



VNB35NV04 / VNP35NV04 VNV35NV04 / VNW35NV04

“OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFET

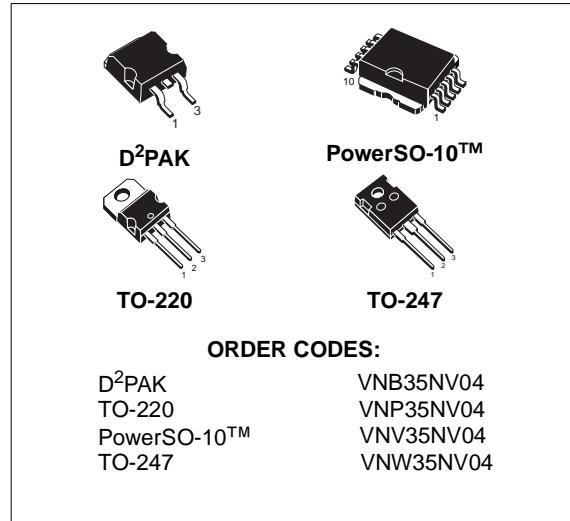
PRELIMINARY DATA

TYPE	R _{DS(on)}	I _{lim}	V _{clamp}
VNB35NV04			
VNP35NV04	10 mΩ	30 A	40 V
VNV35NV04			
VNW35NV04			

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

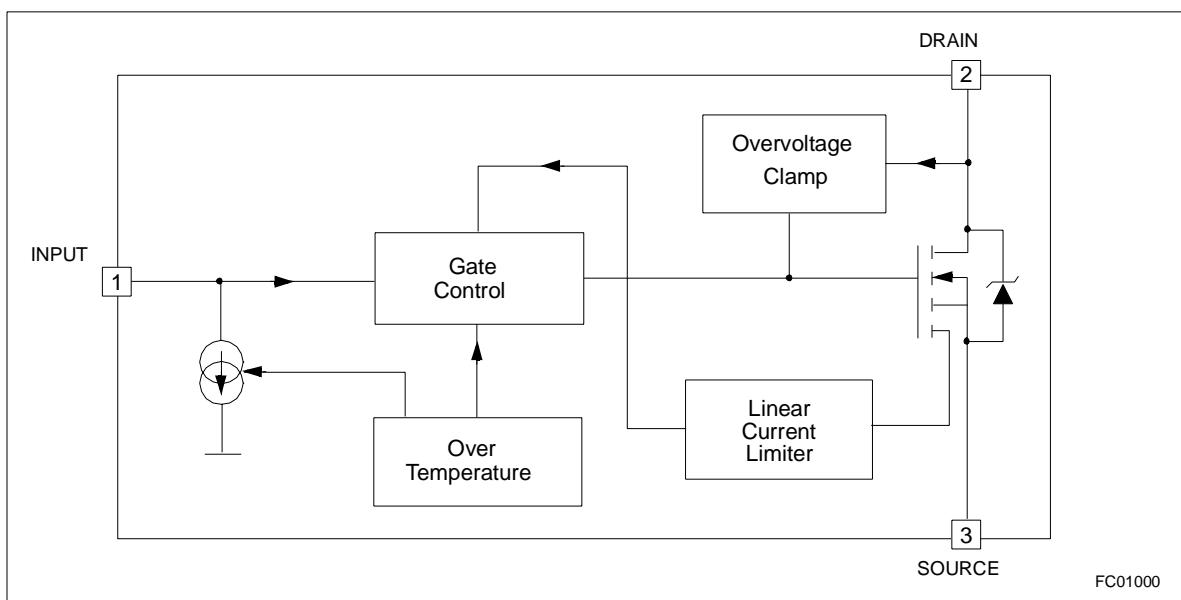
The VNB35NV04, VNP35NV04, VNV35NV04, VNW35NV04 are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power



MOSFETS from DC up to 25KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

BLOCK DIAGRAM

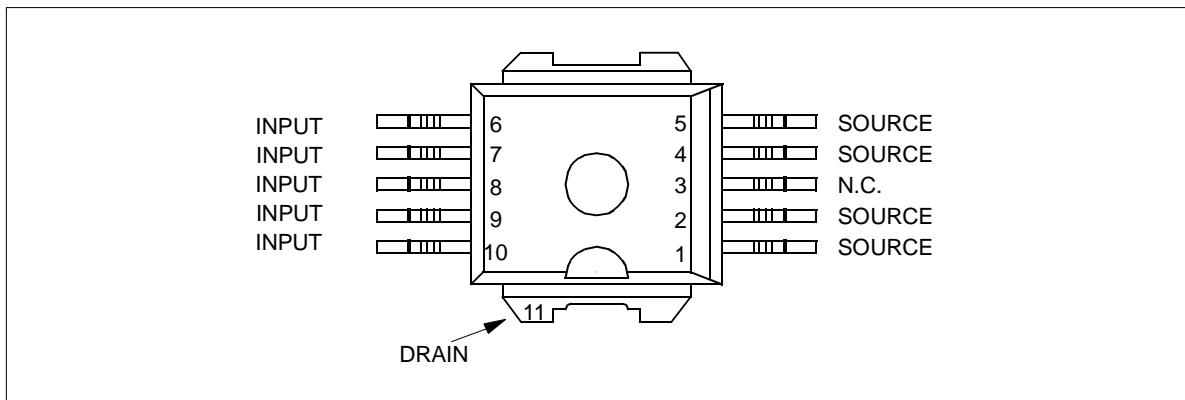


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ABSOLUTE MAXIMUM RATING

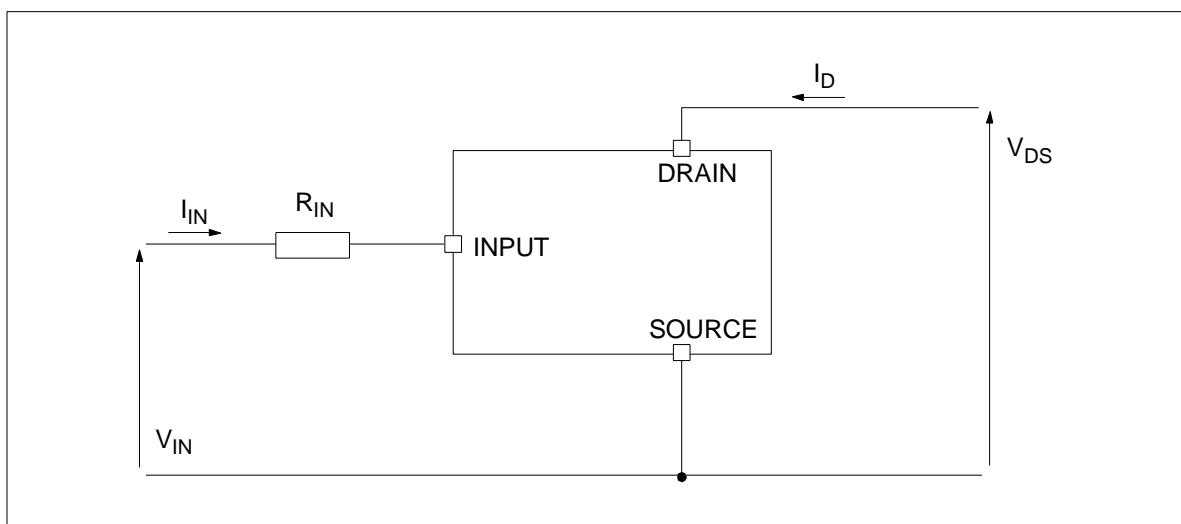
Symbol	Parameter	Value				Unit
		PowerSO-10™	D ² PAK	TO-220	TO-247	
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)		Internally Clamped			V
V_{IN}	Input Voltage		Internally Clamped			V
I_{IN}	Input Current		+/-20			mA
$R_{IN\ MIN}$	Minimum Input Series Impedance		4.7			Ω
I_D	Drain Current		Internally Limited			A
I_R	Reverse DC Output Current		-30			A
V_{ESD1}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)		4000			V
V_{ESD2}	Electrostatic Discharge on output pin only ($R=330\Omega$, $C=150pF$)		16500			V
P_{tot}	Total Dissipation at $T_c=25^\circ C$	125	125	125	208	W
T_j	Operating Junction Temperature		Internally limited			$^\circ C$
T_c	Case Operating Temperature		Internally limited			$^\circ C$
T_{stg}	Storage Temperature		-55 to 150			$^\circ C$

CONNECTION DIAGRAM (TOP VIEW)



(*) For the pins configuration related to TO-220, TO-247, D²PAK, see outlines at page 1.

CURRENT AND VOLTAGE CONVENTIONS



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THERMAL DATA

Symbol	Parameter	Value				Unit
		PowerSO-10™	D2PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal Resistance Junction-case MAX	1	1	1	0.6	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient MAX	50(*)	50(*)	50	30	°C/W

(*) When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 µm thick) connected to all DRAIN pins.

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 150°C, unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source Clamp Voltage	$V_{IN}=0V$; $I_D=15A$	40	45	55	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	$V_{IN}=0V$; $I_D=2mA$	36			V
V_{INTH}	Input Threshold Voltage	$V_{DS}=V_{IN}$; $I_D=1mA$	0.5		2.5	V
I_{ISS}	Supply Current from Input Pin	$V_{DS}=0V$; $V_{IN}=5V$		100	150	µA
V_{INCL}	Input-Source Clamp Voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero Input Voltage Drain Current ($V_{IN}=0V$)	$V_{DS}=13V$; $V_{IN}=0V$; $T_j=25^\circ C$ $V_{DS}=25V$; $V_{IN}=0V$			30 75	µA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{IN}=5V$; $I_D=15A$; $T_j=25^\circ C$ $V_{IN}=5V$; $I_D=15A$			10 20	mΩ

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ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^\circ\text{C}$, unless otherwise specified)

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs} (*)	Forward Transconductance	$V_{DD}=13\text{V}$; $I_D=15\text{A}$		35		s
C_{OSS}	Output Capacitance	$V_{DS}=13\text{V}$; $f=1\text{MHz}$; $V_{IN}=0\text{V}$		1300		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=15\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN \text{ MIN}}=4.7\Omega$ (see figure 1)		150	500	ns
t_r	Rise Time			750	2500	ns
$t_{d(off)}$	Turn-off Delay Time			900	3000	ns
t_f	Fall Time			500	1500	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=15\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=2.2\text{K}\Omega$ (see figure 1)		4	12	μs
t_r	Rise Time			32	100	μs
$t_{d(off)}$	Turn-off Delay Time			50	150	μs
t_f	Fall Time			40	120	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}$; $I_D=15\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=R_{IN \text{ MIN}}=4.7\Omega$		18		$\text{A}/\mu\text{s}$
Q_i	Total Input Charge	$V_{DD}=12\text{V}$; $I_D=15\text{A}$; $V_{IN}=5\text{V}$ $I_{gen}=2.13\text{mA}$ (see figure 5)		60		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD} (*)	Forward On Voltage	$I_{SD}=15\text{A}$; $V_{IN}=0\text{V}$ $I_{SD}=15\text{A}$; $di/dt=100\text{A}/\mu\text{s}$ $V_{DD}=30\text{V}$; $L=200\mu\text{H}$ (see test circuit, figure 2)		0.8		V
t_{rr}	Reverse Recovery Time			400		ns
Q_{rr}	Reverse Recovery Charge			1.4		μC
I_{RRM}	Reverse Recovery Current			7		A

PROTECTIONS (-40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=6\text{V}$; $V_{DS}=13\text{V}$	30	45	60	A
t_{dlim}	Step Response Current Limit	$V_{IN}=6\text{V}$; $V_{DS}=13\text{V}$		50		μs
T_{jsh}	Overtemperature Shutdown		150	175		$^\circ\text{C}$
T_{jrs}	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf}	Fault Sink Current	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$; $T_j=T_{jsh}$	10	15	20	mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j=25^\circ\text{C}$; $V_{DD}=24\text{V}$ $V_{IN}=5\text{V}$; $R_{gen}=R_{IN \text{ MIN}}=4.7\Omega$; $L=24\text{mH}$ (see figures 3 & 4)	1.7			J

(*) Pulsed: Pulse duration = 300μs, duty cycle 1.5%

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 25KHz. The only difference from the user's standpoint is that a small DC current I_{iss} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION:

internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current I_D to I_{lim} whatever the INPUT pin voltages is. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- STATUS FEEDBACK:

in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{iss} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

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Fig.1: Switching Time Test Circuit for Resistive Load

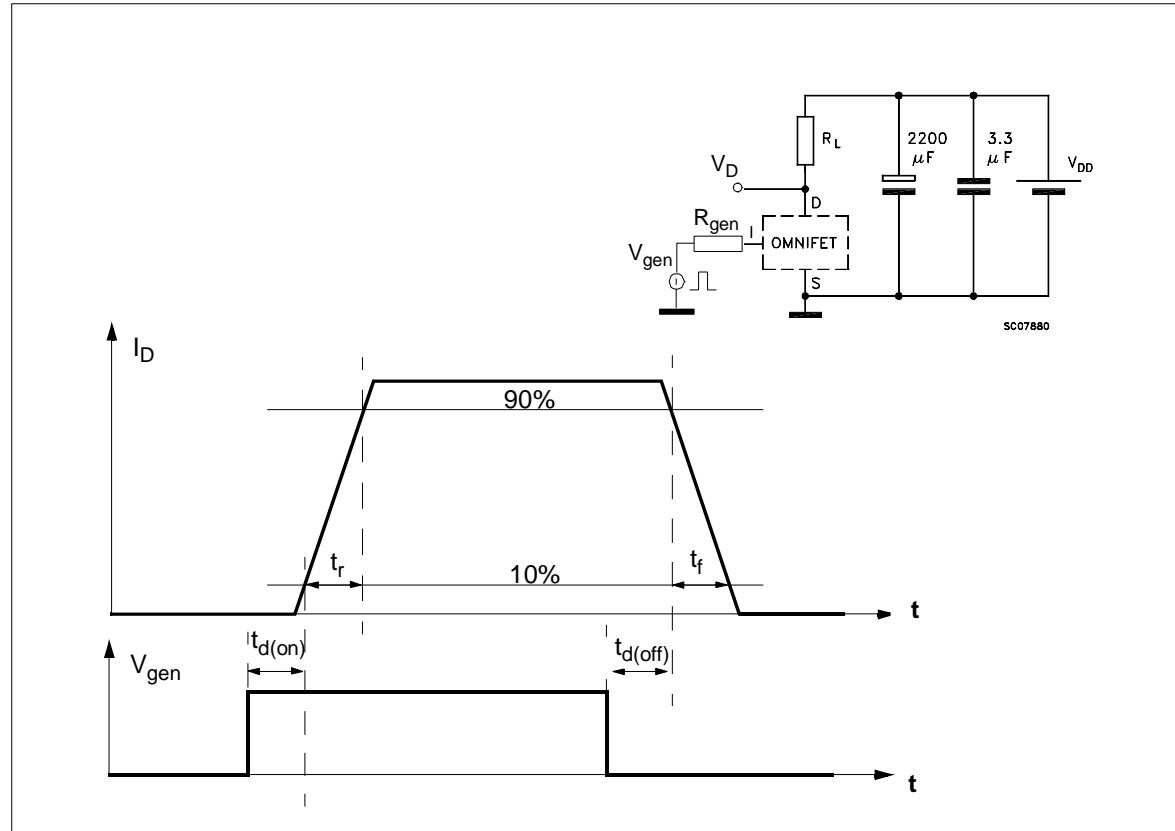
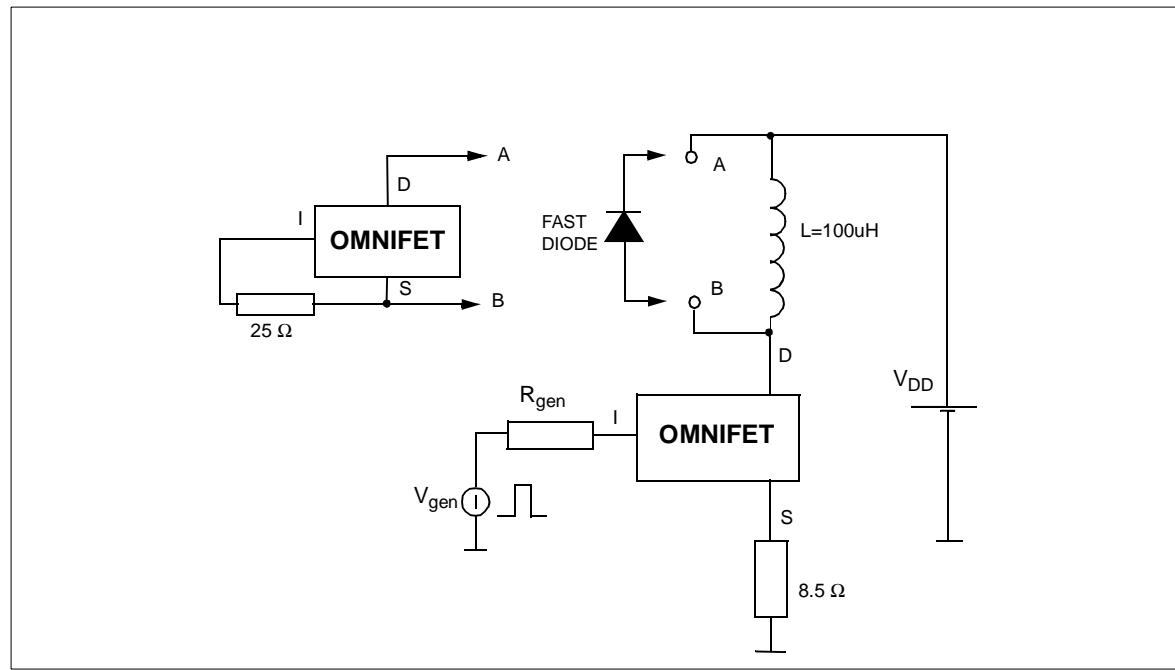


Fig.2: Test Circuit for Diode Recovery Times



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Fig. 3: Unclamped Inductive Load Test Circuits

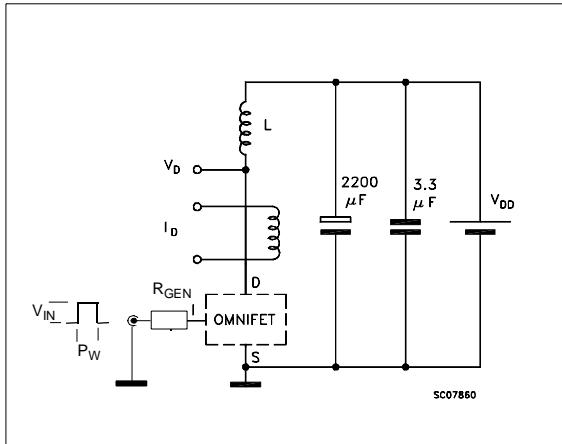


Fig. 4: Unclamped Inductive Waveforms

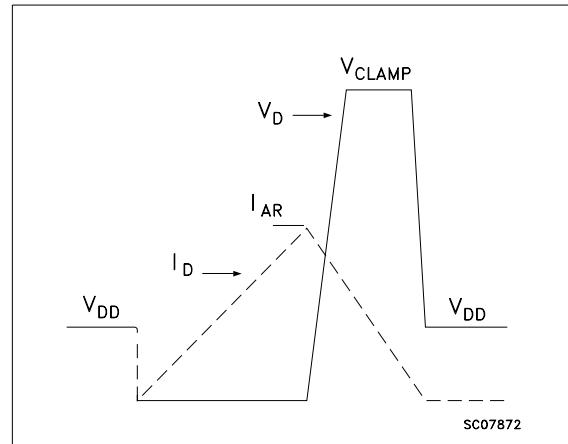


Fig. 5: Input Charge Test Circuit

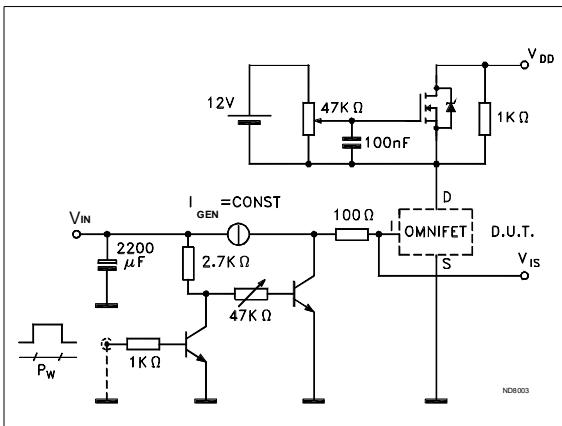


Fig 6 : Thermal Impedance for TO-220

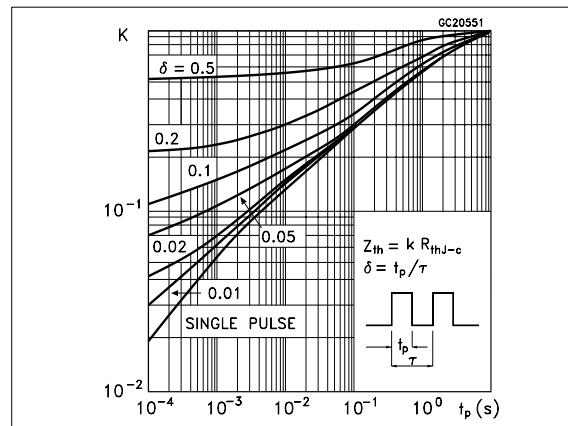
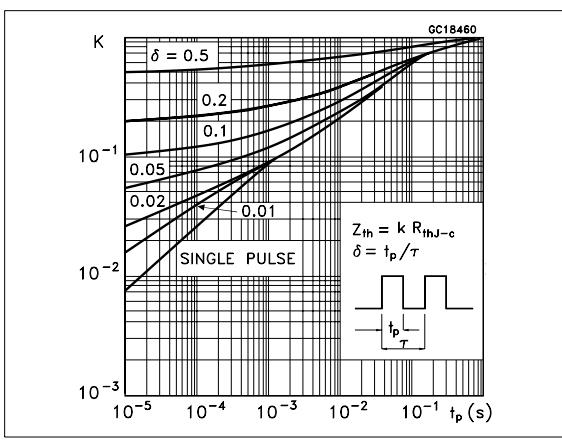


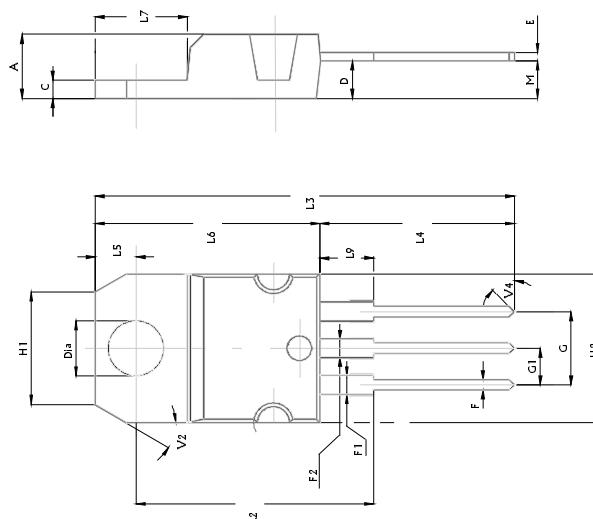
Fig. 7:Thermal Impedance for TO-247



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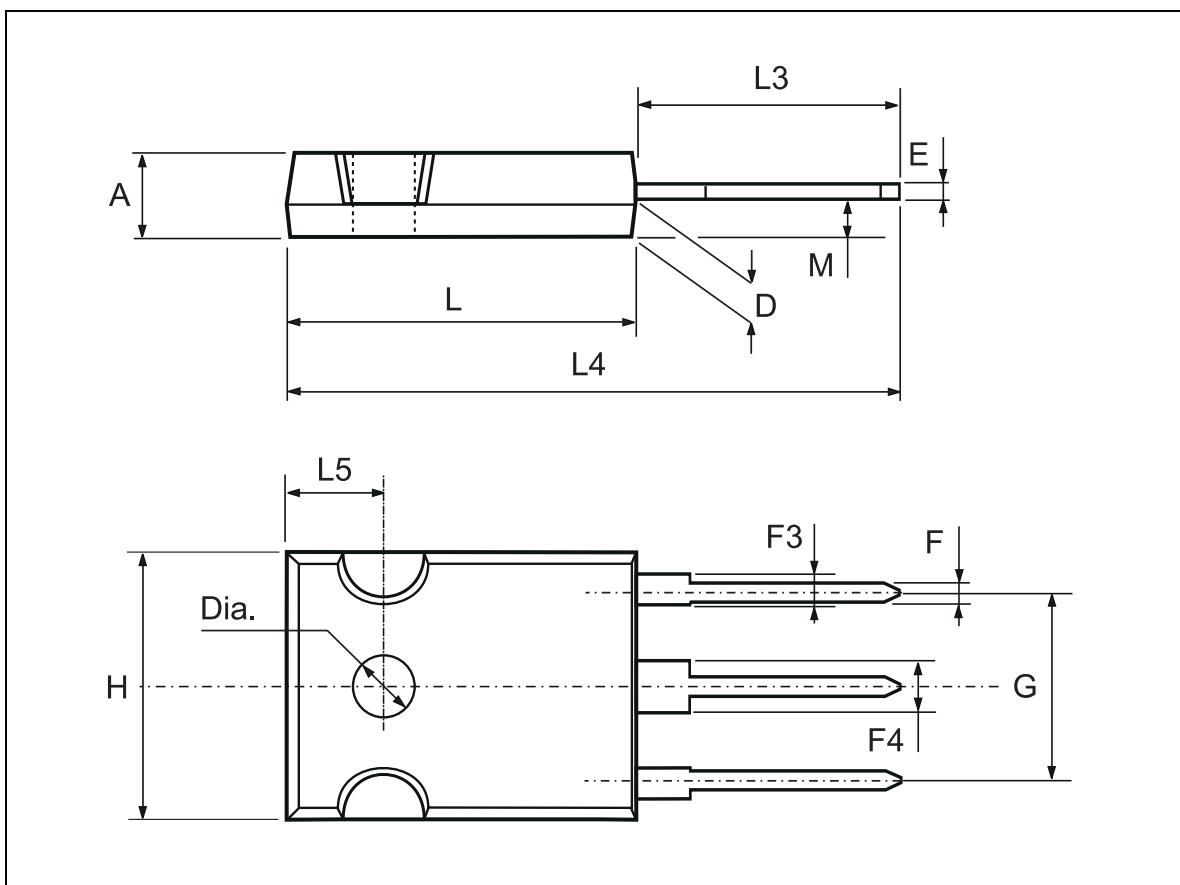
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137	0.154	
M		2.6			0.102	
DIA.	3.75		3.85	0.147		0.151



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118
Dia.	3.55		3.65	0.140		0.144

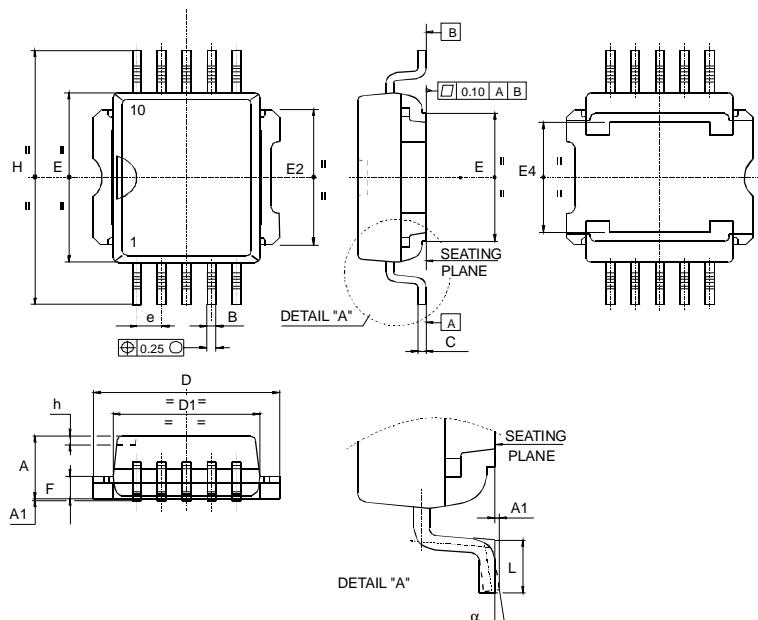


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PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
$\alpha (*)$	2°		8°	2°		8°

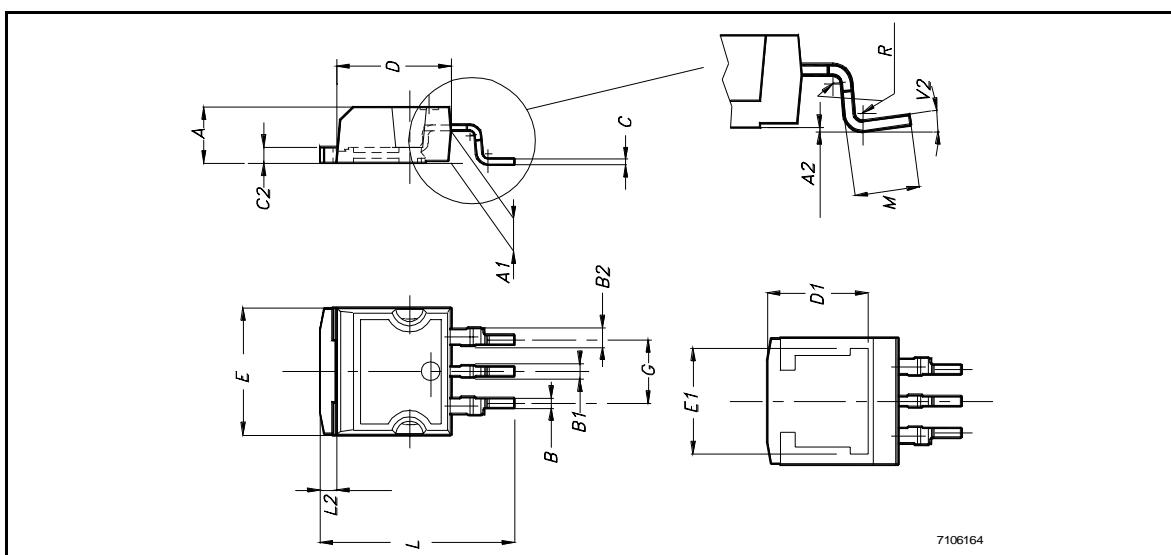
(*) Muar only POA P013P



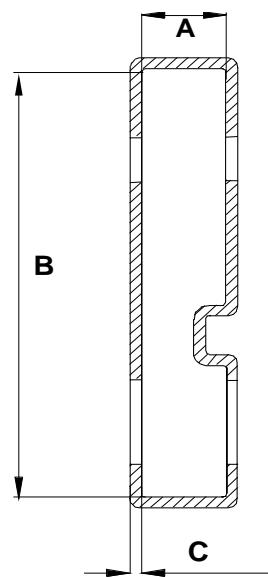
P095A

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B1	0.8		1.3	0.031		0.051
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



TO-220 TUBE SHIPMENT (no suffix)

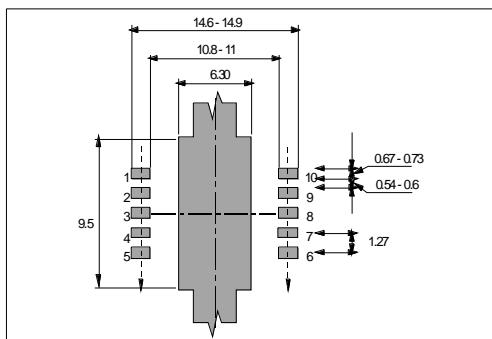


Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	5.5
B	31.4
C (± 0.1)	0.75

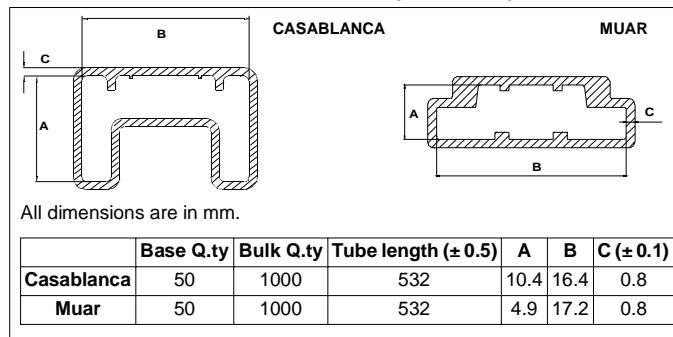
All dimensions are in mm.

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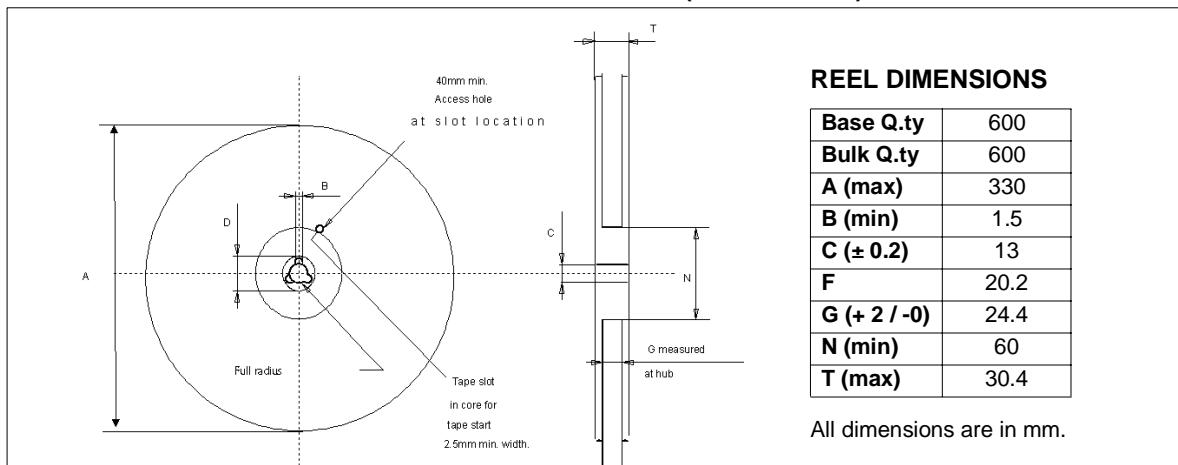
PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

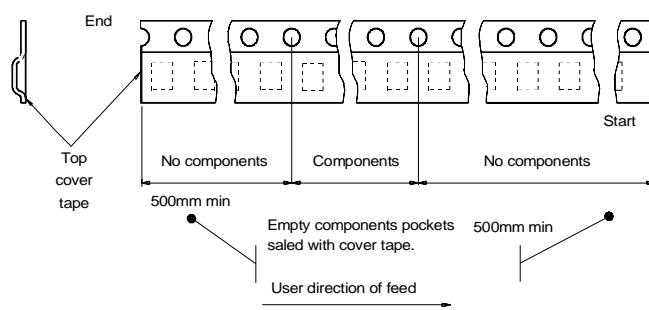
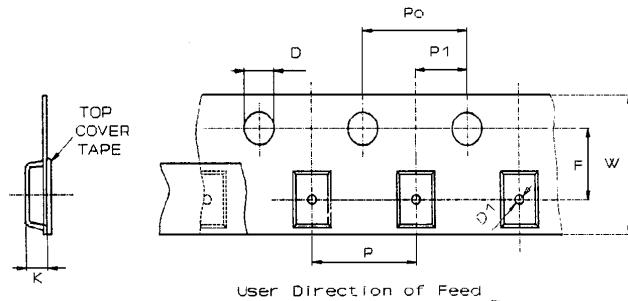


TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

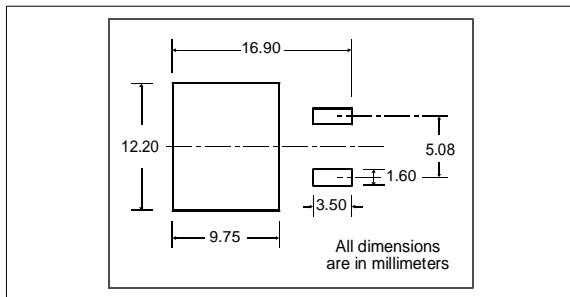
Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

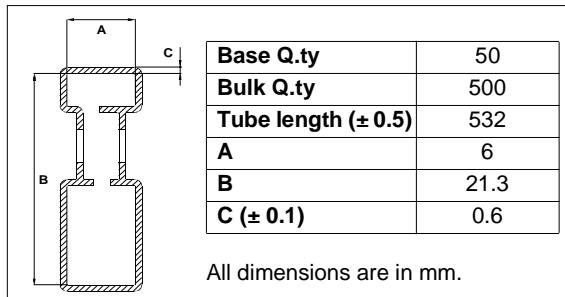


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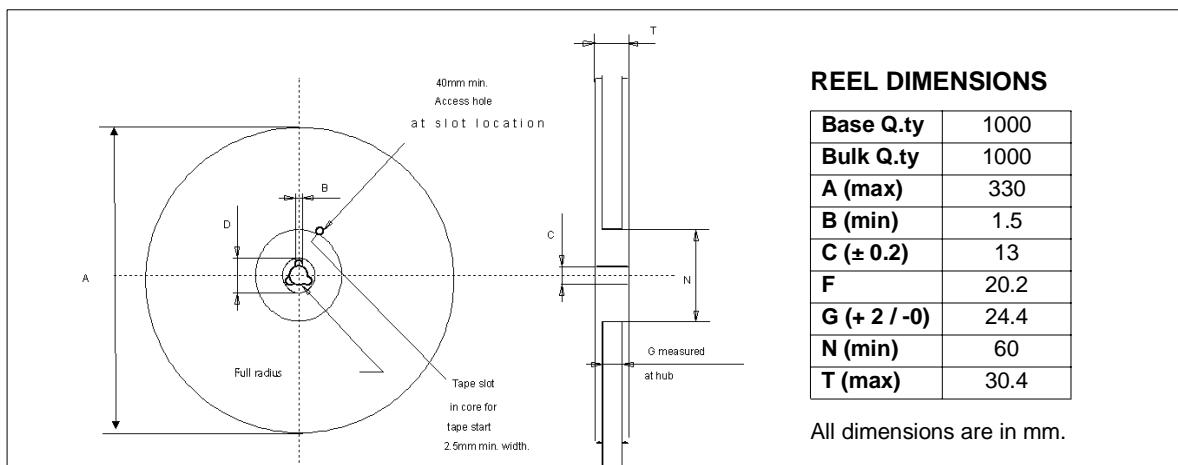
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

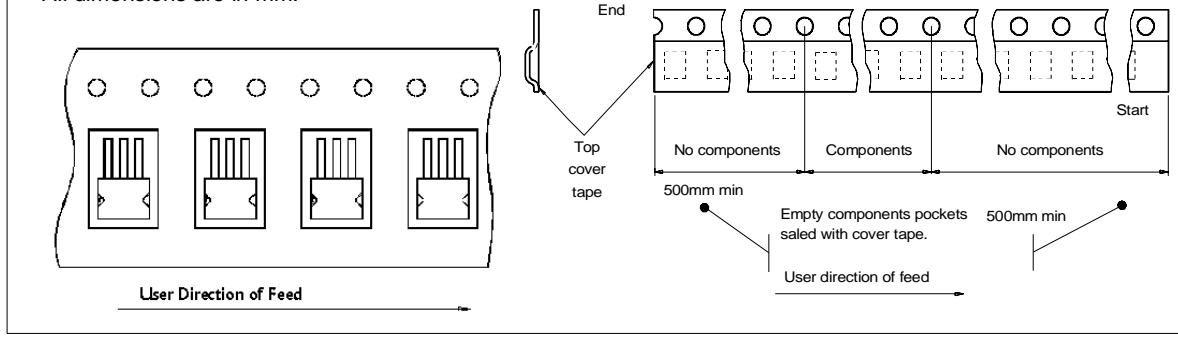
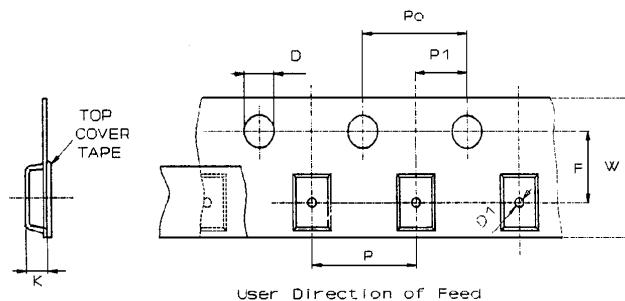


TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	16
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



VNB35NV04 / VNP35NV04 / VNV35NV04 / VNW35NV04

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