V.22 bis Modem

GENERAL DESCRIPTION

The XR-2400 Chip Set is designed to provide the complete modem function for V.22 bis (2400 BPS) type modems. The chip set consists of the XR-2401 DSP Modem Signal Processor and the XR-2402A Analog Front End (AFE) with microcontroller interface. The XR-2400 set also supports Bell 212A (1200/300 BPS) and CCITT V.22 (1200 BPS) modes for a Bell/CCITT compatible system.

The XR-2401 is the heart of the system. It is a digital signal processor (DSP) based chip providing 300 BPS FSK, 1200 BPS DPSK, and 2400 QAM modulation and demodulation for the system. Other functions included are scrambler/descrambler, adaptive equalizer, carrier detection, DTMF tone generator, and AGC control.

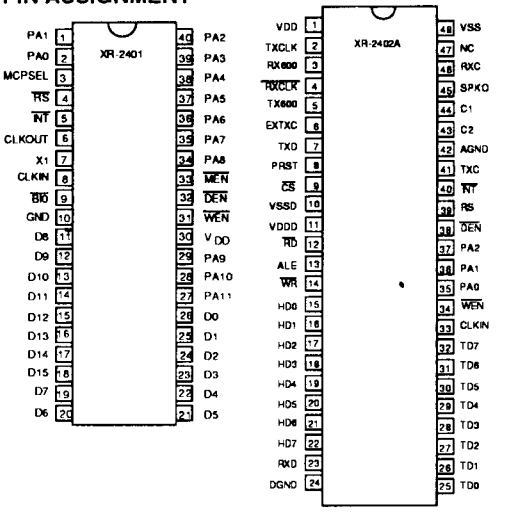
The XR-2402A provides the interface functions for the XR-2401, such as A/D and D/A converters for accessing the DSP chip inputs and outputs. Also provided are band splitting filters (SCF type), a programmable gain amplifier (PGA), asynchronous to synchronous and synchronous to asynchronous conversion, guard tone generation for CCITT applications, and a timing recovery.

Both the XR-2401 and XR-2402A are constructed with the Si-gate CMOS technology for low power operation. The XR-2401 is available in a 40 pin and the XR-2402A in a 48 pin package. The XR-2401 operates from a single +5 volt and XR-2402A from ±5 volt power supply.

FEATURES

2400 BPS (QAM), 1200 BPS (DPSK), 300 BPS (FSK) Operation
V.22 bis, V.22, 212A, 103 Compatible
DSP Based (XR-2401)
Bus Structured Control
No Adjustments
DTMF Dialing
Low Power CMOS (450 mw max.)
Adaptive Equalization
Asynchronous/Synchronous Operation
550 Hz/1800 Hz Guard Generation
Automatic Call Progress Monitoring
Upgradeable to MNP 5 Operation With the XR-2403B 5 microcontroller or V.42bis with the XR-2443 microcontroller

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2401CP	Plastic	0°C to 70°C
XR-2402ACP	Plastic	0°C to 70°C
XR-2401CJ	PLCC	0°C to 70°C
XR-2402ACJ	PLCC	0°C to 70°C
XR-2401CQ	QFP	0°C to 70°C
XR-2402ACQ	QFP	0°C to 70°C

For other pin assignments, refer to the end of this datasheet

APPLICATIONS

Stand Alone Modems
Internal Modems
Smart Modems
Laptop Applications

ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-2401	-0.3 to +7 V
XR-2402A	-7 to +7 V
Input Voltage	-0.7 to VDD + 0.3 V
DC Input Current (Any Input)	± 10mA
Power Dissipation (package limitation)	1 Watt
Storage Temperature Range	-65°C to +125°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
XR-2401 $f_{CLKIN} = 19.6608$ MHz ± 0.01%						
I_{DD}	Positive Supply Current	33	50	mA		
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	High Level Input Voltage	2.0			V	Except CLKIN
V_{IHC}	CLK High Level Input Voltage	0.56 V_{DD}			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			20	µA	$V_{OH} = V_{DD} - .4V$
				300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High Level Output Voltage	$V_{DD} - .4$			V	$I_{OH} = 20$ µA
		2.4			V	$I_{OH} = 300$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
XR-2402A $f_{CLKIN} = 4.9152$ MHz ± 0.01%						
V_{DD}	Positive Supply Voltage	4.5	5.0	5.5	V	
VSS	Negative Supply Voltage	-5.5	-5.0	-4.5	V	
I_{DD}	Positive Supply Current		15	20	mA	
I_{DDS}	Positive Supply Current, Standby Mode		3	5	mA	
I_{SS}	Negative Supply Current			20	mA	
I_{SSS}	Negative Supply Current, Standby Mode			5	mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4V$
I_{OL}	Low Level Output Current			2	mA	
V_{OH}	High level Output Voltage	2.4			V	$I_{OH} = 700$ µA
I_I	Input Current			50	µA	$V_I = 0$ to V_{DD}
R_{XC}	Receive Carrier Range	-6		-45	dBm	(Using 6/16 dB RCVG feature)

SYSTEM DESCRIPTION

The XR-2401 / XR-2402A Modem Chip Set is designed to interface directly to popular microcontrollers, such as 8031. The microcontroller provides such functions as handshake control, smart functions such as "AT" commands, and dialing control. Exar provides a complete "AT" command set which can be used as is or modified.

The only other circuitry necessary is a line interface circuit (DAA) and RS-232 interface.

TRANSMITTER SPECIFICATIONS

All values are measured at TXC (Pin 41) of the XR-2402A with Bit 0-2 = 1 of CNTRL 0.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER POWER						
T_{XC} QAM	QAM/PSK Transmitter Power	-.6		+3.4	dBm	
T_{XC}550	CCITT Guard Tone Power	-1.7		-.4	dBm	
T_{XC}1800		-5.2		-3.4	dBm	
T_{XC} QAM/PSK 550	QAM/PSK Transmitter Power With Guard Tone	1.9			dBm	
T_{XC} QAM/PSK 1800		.8			dBm	
T_{XC} FSK	FSK Transmitter Power	-.16		+2.5	dBm	
T_{XC} AT	Answer Tone Power	1.6		2.9	dBm	
T_{XC} DTMF C	DTMF Tone Power Column	-4.9		-3.1	dBm	
T_{XC} DTMF R	DTMF Tone Power Row	-6.2		-4.4	dBm	
ΔT_{XC} DTMF	DTMF Amplitude Difference	-2		+2	dB	
SPEAKER						
AV SPKR	Gain - RXC to SPKO	4	6	8	dB	AV SPKR = 20 Log $\frac{V_{SPKO}}{V_{RXC}}$

SYSTEM PERFORMANCE

V_{RXC} = -40dBm 40, Originate Mode, 3002 Line Conditions, T_{XC} = -10dBm.

SYSTEM	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
S/N	Signal-to-Noise Ratio		16		dB	2400 BPS
			9		dB	1200 BPS
			12		dB	300 BPS
F_{OFF}	Frequency Offset		±10		Hz	2400/1200 BPS

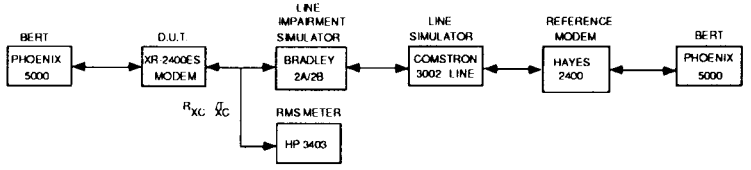
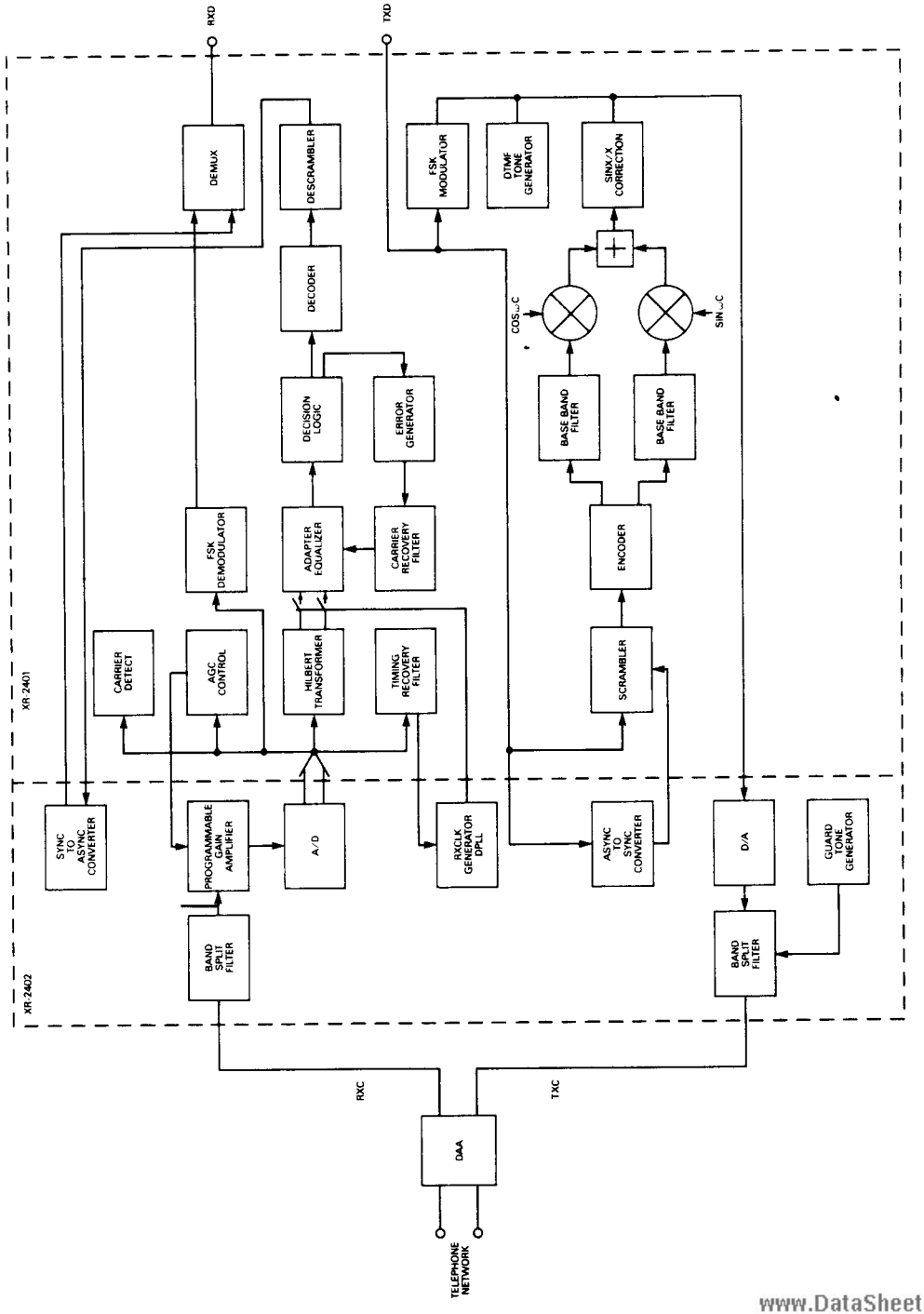
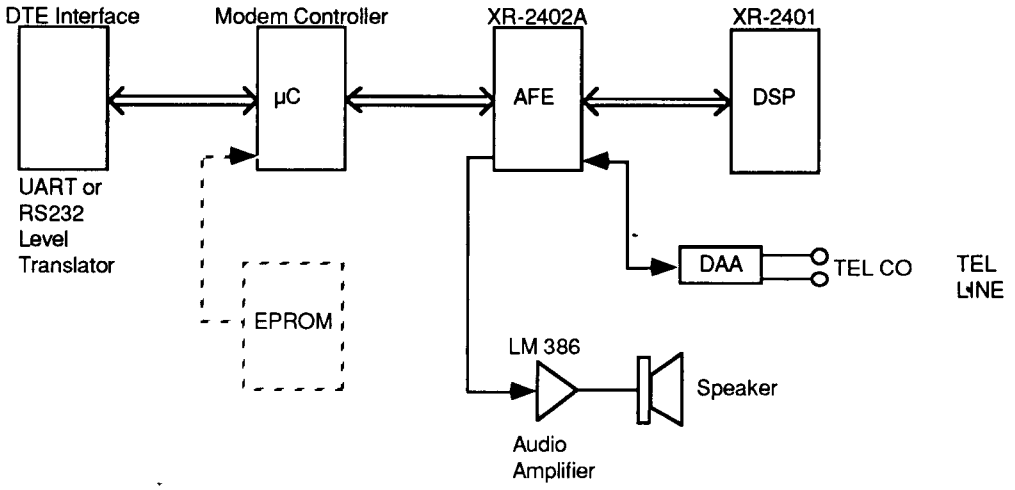


Figure 1. Performance Test Set-Up



XR-2400 Functional Block Diagram



XR-2400 Typical System Connection

PIN DESCRIPTIONS/FUNCTIONS

The XR-2401 and XR-2402A provide the heart of a V.22 bis modem system and when connected to a microcontroller such as the 8031 type, a complete system is formed. The XR-2402A provides the analog front end (AFE) function as well as the bridge, or interface, between the XR-2401 digital signal processor (DSP) and microcontroller.

The pin functions of the XR-2401 are as follows:

Symbol	I/O	Pin#	Description
V_{DD}	I	30	Positive supply Voltage +5V ±5%
GND	I	10	Ground connection - digital
$\overline{RS}$	I	4	Reset to initialize chip
X1	I	7	Crystal input 19.6608 MHz ±0.01%
CLK IN	I	8	Crystal input or external clock
CLK OUT	O	6	1/4 crystal/CLK IN frequency
PA0-PA11	O	1,2 27,29, 34-40	External address bus. I/O port address multiplexed over PA0-PA2
$\overline{BIO}$	I	9	External polling input for bit test and jump operations.
D0-D15	I/O	11-26	16 bit data bus
$\overline{DEN}$	O	32	Data enable indicates the XR-2401 accepting input data on D0-D15.
$\overline{INT}$	I	5	Interrupt input
MCPSEL	I	3	Mode select. 1 = microcomputer mode, 0 = microprocessor mode.
$\overline{MEN}$	O	33	Memory enable indicates that D0-D15 will accept memory instruction.
$\overline{WEN}$	O	31	Write enable indicates valid data on D0-D15.

The pin functions of the XR-2402A are as follows:

Symbol	I/O	Pin#	Description
VDD	I	1	Positive analog supply +5V ±5%
VSS	I	48	Negative analog supply -5V ±5%
VDDD	I	11	Logic positive supply +5V ±5%
VSSD	I	10	Logic negative supply -5V ±5%
DGND	I	24	Logic ground
AGND	I	42	Analog ground
PRST	I	8	Power on reset input
Microprocessor Interface			
ALE	I	13	Address latch enable
HD0	I/O	15	Address/data bus bit 0
HD1	I/O	16	Address/data bus bit 1
HD2	I/O	17	Address/data bus bit 2
HD3	I/O	18	Address/data bus bit 3
HD4	I/O	19	Address/data bus bit 4
HD5	I/O	20	Address/data bus bit 5
HD6	I/O	21	Address/data bus bit 6
HD7	I/O	22	Address/data bus bit 7
$\overline{CS}$	I	9	Chip select
$\overline{WR}$	I	14	Write strobe
$\overline{RD}$	I	12	Read strobe

XR-2401 Interface

Symbol	I/O	Pin#	Description
CLK IN	I	33	4.9152MHz input from XR-2401
$\overline{INT}$	O	40	Interrupt flag for XR-2401
$\overline{RS}$	O	39	Reset output for XR-2401
PA0	I	35	I/O port address bus bit 0
PA1	I	36	I/O port address bus bit 1
PA2	I	37	I/O port address bus bit 2
$\overline{DEN}$	I	38	Read enable strobe
$\overline{WEN}$	I	34	Write enable strobe
TD0	I/O	25	Data bus bit 0
TD1	I/O	26	Data bus bit 1
TD2	I/O	27	Data bus bit 2
TD3	I/O	28	Data bus bit 3
TD4	I/O	29	Data bus bit 4
TD5	I/O	30	Data bus bit 5
TD6	I/O	31	Data bus bit 6
TD7	I/O	32	Data bus bit 7
RS232C Interface			
EXTXC	I	6	External transmit clock
TXCLK	O	2	Transmit clock output
TXD	I	7	Transmit data input
$\overline{RXCLK}$	O	4	Receive clock output
RXD	O	23	Receive data output, with pullup resistor

Special Functions

TX600	O	5	Transmit 600 Hz output
RX600	O	3	Receive 600 Hz output
SPKO	O	45	Audio output to speaker

Analog Interface

TXC	O	41	Transmit carrier output
RXC	I	46	Receive carrier input
C1	O	44	Programmable gain stage output
C2	I	43	A/D input

SYSTEM OPERATION

The XR-2400 (XR-2401/2402A) is designed to interface with a host controller by both hardware and software. The XR-2400 looks like a memory mapped peripheral to the host controller. The XR-2402A acts as a bridge or interface between the XR-2401 DSP and host controller and thus, all control/status information will pass through it. Figure 2 shows the general data/address bus connection of the XR-2400 to the host controller.

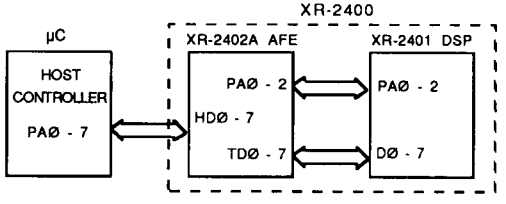


Figure 2. General Data/Address Bus Connection

The XR-2401 DSP performs all of the modem signal processing functions. While, the controller functions are left to the host microcontroller for system flexibility.

There are two kinds of control/status registers for the host microcontroller to access; one in the XR-2402A and one in the XR-2401 via the XR-2402A interface buffer. To the µc, the XR-2402A register looks just like an external data memory. The XR-2401 data memory must be accessed through the XR-2402A. The handshake procedure to access the memory map is shown in Table I.

Read	Write	XR-2402A
	0	Address register (8 bit latch)
	1	Write data register (8 bit latch)
2		Read data register (8 bit latch)
3		Status register in XR-2402A
	3	Control register in XR-2402A

Table 1. Memory Map for Host

GENERAL MODE SETTING READING INFORMATION FROM XR-2400

A handshake procedure is necessary for communication between the host microcontroller and XR-2400. All data (address, write data, read data) passes through a register in the XR-2402A with the procedure for controlling this register as follows:

Read Cycle

First, the host microcontroller will write a target address to the XR-2402A address register. Simultaneously, the XR-2402A will generate an interrupt for the XR-2401, which will branch to interrupt service routine and send data out to the XR-2402A reading register. This procedure takes 3 microseconds, thus, the host microcontroller needs to ensure it waits at least 3 microseconds from target address and reading data. (Refer to Figure 12)

Write Cycle

The write cycle is used for the host microcontroller to write to the XR-2400. Data is written first to the XR-2402A then the target address to the address register. It will generate interrupt for the XR-2401 and after a 6 microseconds delay, the XR-2401 will take the data from the write register. (Refer to Figure 12)

Read/Write Data Directly From the XR-2402A

There are two data memory locations which the host microcontroller can access immediately.

1. Status Register - Address 3

   Bit 3 - Bit 0 are copied from Control Register 7 in the XR-2401. Bit 6 - bit 4 are generated in the XR-2402A.

   Bit 0 R_{XDATA}
   Bit 1 Unscrambled R_{XDATA}
   Bit 2 Energy Detect
   Bit 3 Signal Quality Indicator
   Bit 4 S1 Signal Detector. With and S1 pattern coming in, Bit 4 will be continuously high allowing the user to access the coming S1 signal information.
   Bit 5 Dotting Pattern Detect Indicator. With an incoming dotting pattern (alternating etc.), this indicator will be high allowing the user to detect digital loopback.
   Bit 6 R_{XD} after Buffer. The user may access parallel R_{XD} through the data bus.

The following is an instruction example for the status register:

```
MOV     RO,#3 ;     Put #03 in RO
MOVX    A, @ RO;    Move external memory #03 to ACC.
```

2. Control Register

   Bit 0 Parallel TXD Input - This allows the user to input TXD through the parallel data bus.

   Bit 1 Software Reset for XR-2401 - Reset = "0" ; Normal Operation = "1". For prop er reset operation, a low must be present for at least 2 µs.

The following is an example of writing to the control register:

```
MOV     RO, #3   ; Put #03 in RO
MOVX @ RO, A     ; Move data from ACC
                   to external memory.
```

Modem Mode Selection Control

The XR-2401 data memory location #69 is used for mode selection as follows:

0	Idle Mode
1	FSK Mode
2	PSK Mode
3	DTMF Mode

Handshake Sequences

The XR-2400 chip set provides operating modes of 2400 BPS, 1200 BPS and 300 BPS to cover CCITT standards of V.22 bis and V.22 as well as Bell 212A and 103. The following figures illustrated the handshake sequences for automatic rate speed selection. Figure 3 shows the sequence for 2400 BPS (V.22 bis) with V.25 automatic answering. The following figures, 4 through 7, show the remaining handshake sequences needed to support other CCITT/Bell operating modes.

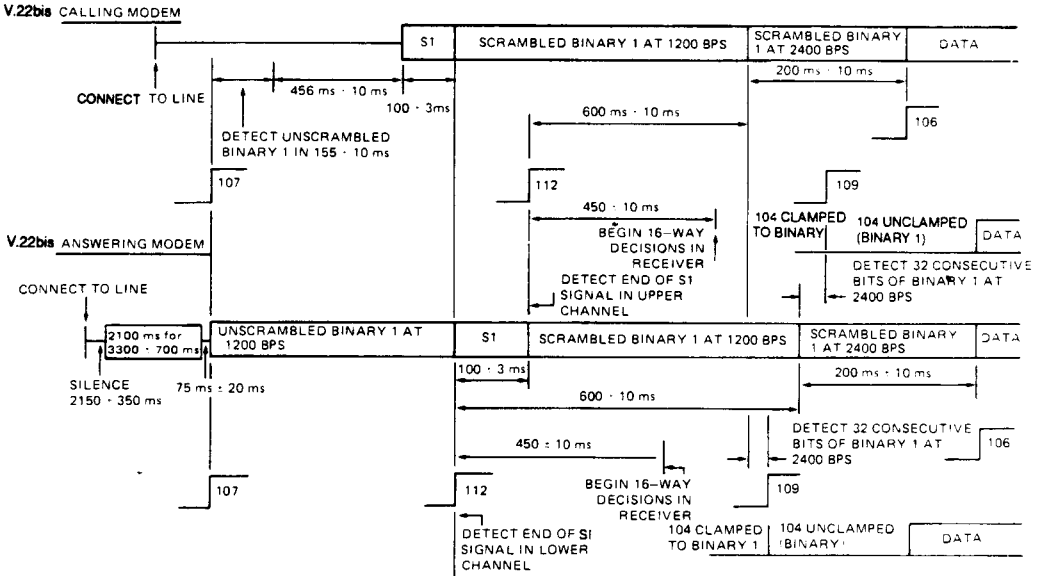


Figure 3. V.22 bis Handshake Sequence at 2400 BPS (with V.25 Auto Ans.)

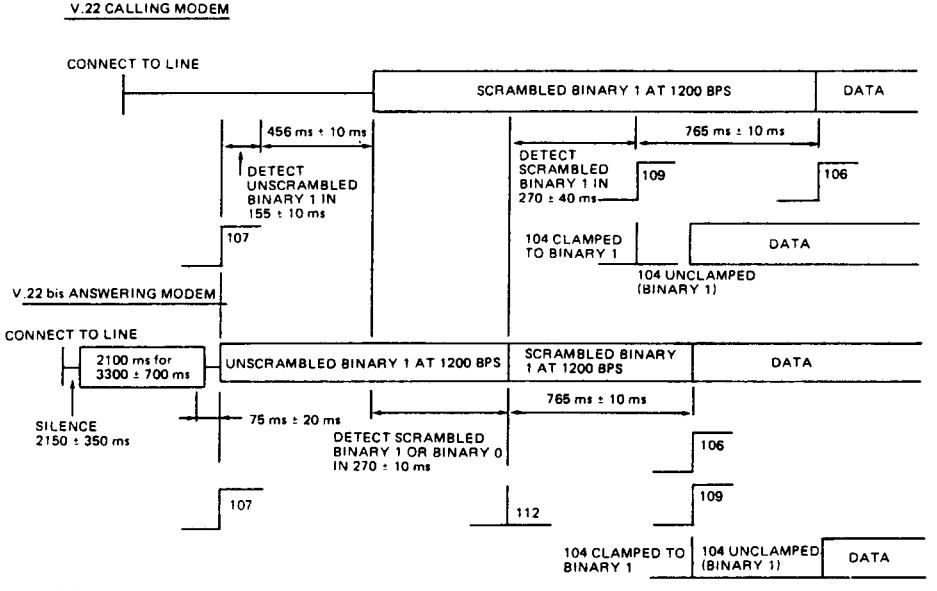


Figure 4. V.22 bis Handshake Sequence at 1200 BPS with V.22 Calling Modem (with V.25 Auto Ans.)

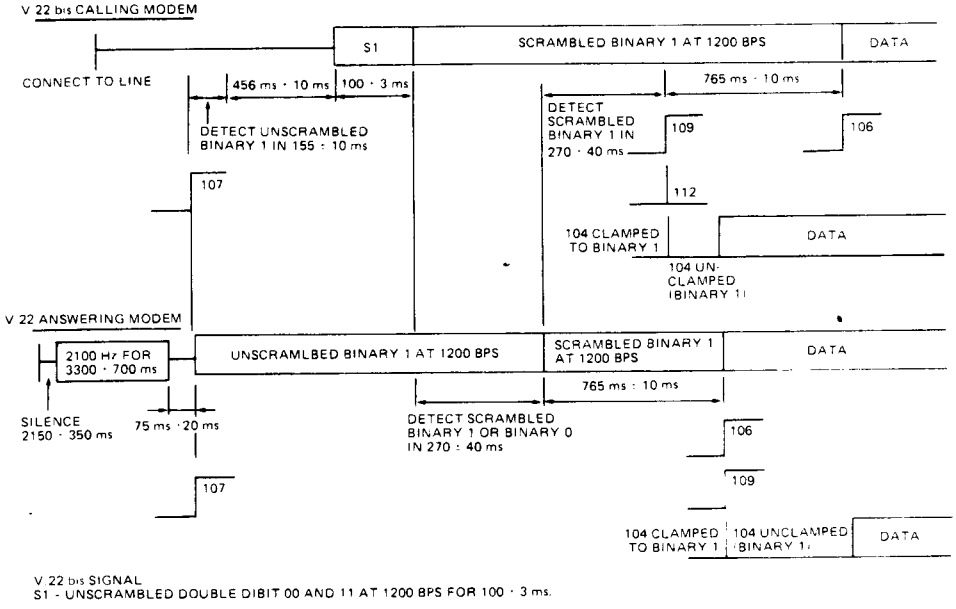


Figure 5. V.22 bis Handshake Sequence at 1200 BPS with V.22 Answering Modem (with V.25 Auto Ans.)

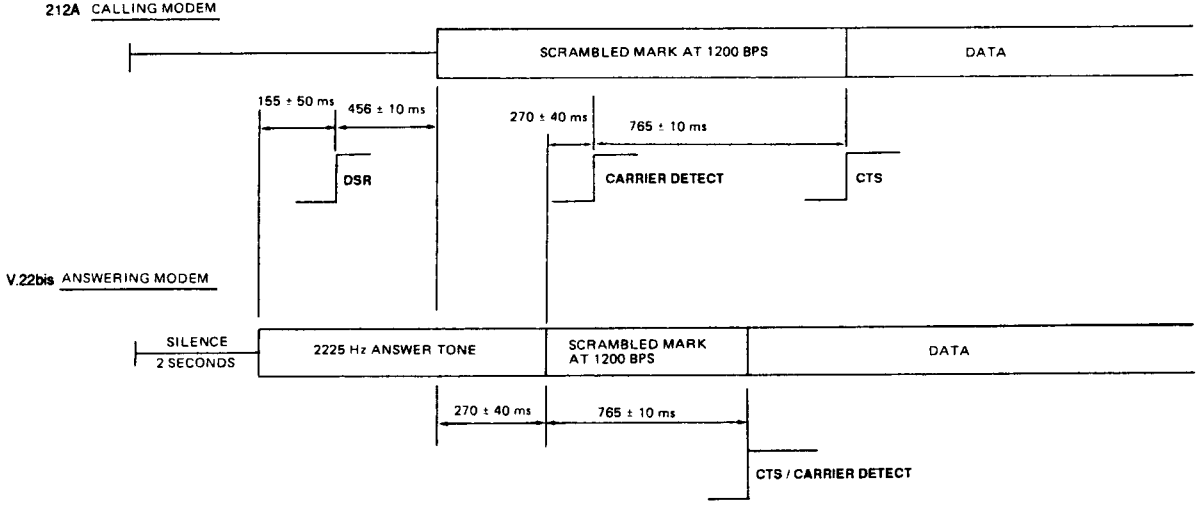


Figure 6. 212A Handshake Sequence at 1200 BPS with 212A Modem

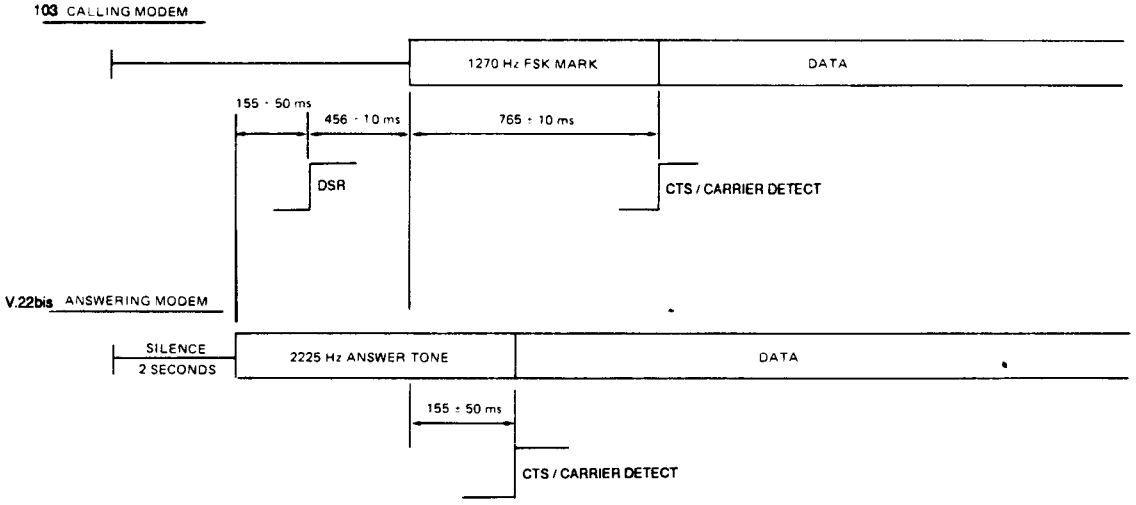
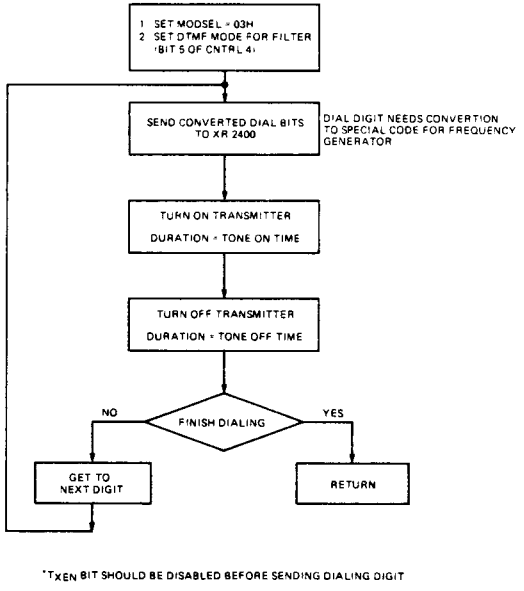


Figure 7. 103 Handshake Sequence at 300 BPS with 103 Modem

DTMF Generation

The XR-2400 provides an onboard DTMF generator which is controlled by the host microcontroller. The flow chart in Figure 8 illustrates the procedure for DTMF tone generation.



*T_{XEN} BIT SHOULD BE DISABLED BEFORE SENDING DIALING DIGIT

Figure 8. DTMF Generation Flow

Table 2 shows the digit/tone pairs for the DTMF generator.

Dial Digit	Encode D4	D3	D2	D1	Tone Pairs (Hz) Tone 1	Tone 2
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	770	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477
(B)	1	1	0	0	697	1633
(C)	1	1	0	1	770	1633
(D)	1	1	1	0	852	1633
(F)	1	1	1	1	941	1633

Table 2. DTMF Tone Pairs / Dial Digits

Call Progress Tone Monitor Operation

The host microcontroller uses the XR-2402A as a filter for call progress detection mode. When CPM = HIGH (enabled), the XR-2402A low band will be scaled down by a factor of 2.5 or 300-660 Hz. The ALB control bit provides the input for band connection to the carrier detect as shown in Table 3.

CPM = 1

ALB	Carrier Detect (CD) Connected to
0	High Band (2400 Hz)
1	Low Band (Scaled low band 300-660 Hz)

Table 3. CPM Frequency Band Assignments

The output of the CD circuit is monitored by the host microcontroller for duration and repetition rate to determine line status. The CD information is available by reading Bit 2 of CNTRL 7. The CD status is as follows:

CD = Energy Detect (direct access locations)
1 = Energy Detected
0 = No Energy

The MODSEL is set to FSK mode. After CPM mode, the microcontroller needs to send a reset signal to the XR-2401.
Table 4 indicates the various CD selections.

CPM	ALB	A/O	CD
1	0	0	Received high band; monitor answer tone.
1	1	0	Received low band filter scaled down by 2.5; monitoring dial tone, busy tone, and ring back tone.
0	0	0	Normal high band energy detect.
0	0	1	Normal low band energy detect.

Table 4. CD Frequency Band Assignments

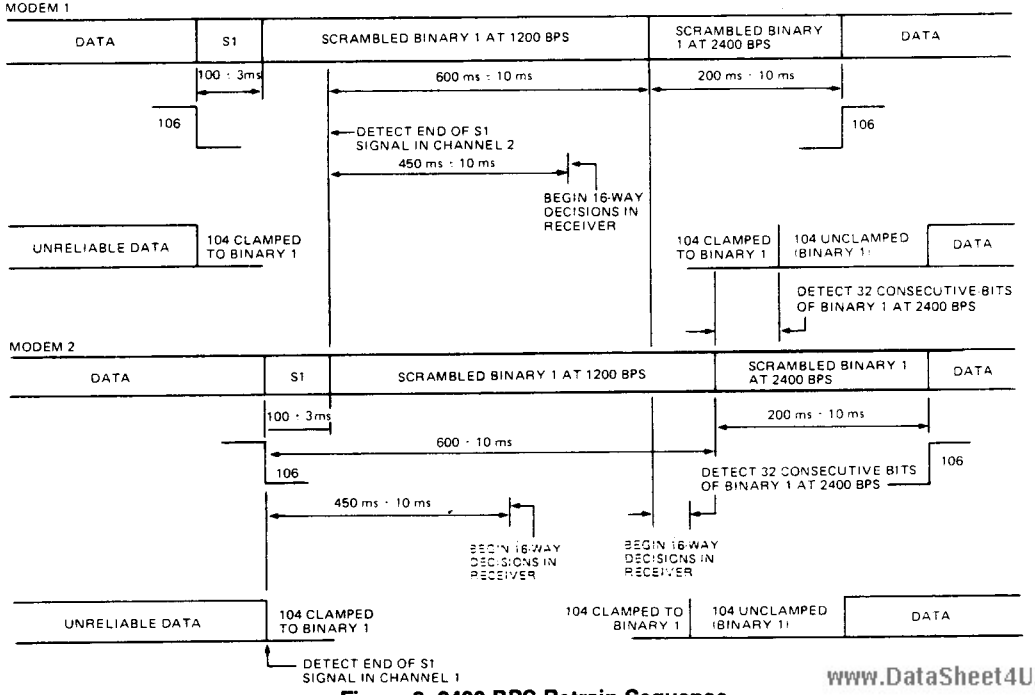


Figure 9. 2400 BPS Retrain Sequence

Signal Quality Indicator

The XR-2400 provides a signal quality indicator, SGQ, to indicate the quality of the received demodulated data. The state of this output is as follows:

SGQ Output:	
0	Good Signal
1	Bad Signal

The XR-2401 signal quality detector utilizes least mean square error method for error detection.

The XR-2400 provides the SGQ indicator for the host microcontroller. A counter is set up in the microcontroller, and if the value in it exceeds a preset value in a predetermined time, a request for retrain requirement will be given. The retrain sequence is shown in Figure 9.

Test Modes

ALB, Analog Loopback, is a test mode which is used for complete testing of the local modem. Figure 10 illustrates the basic signal flow.

The transmit carrier is looped back to the demodulator input, bypassing the receive filter. The demodulator is set to the transmit carrier frequency. Table 5 illustrates ALB selection for answer and originate.

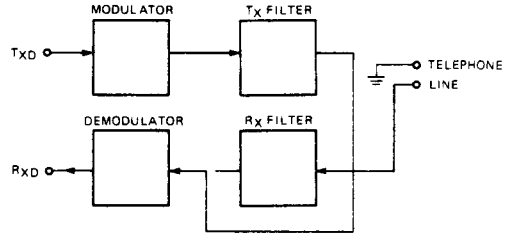


Figure 10. ALB Signal Flow

ALB = 1

MODE	T_X	R_X
ANS	Low Band	Low Band
ORIG	High Band	High Band

Table 5. ALB Frequency Assignments

RDLT, Remote Digital Loopback, is used to test the far-end or remote modem. The start of this type of loopback is automatically initiated by sending an unscrambled mark pattern, as seen in Figure 11. Also shown in Figure 11 is the carrier pattern for termination of RDLB.

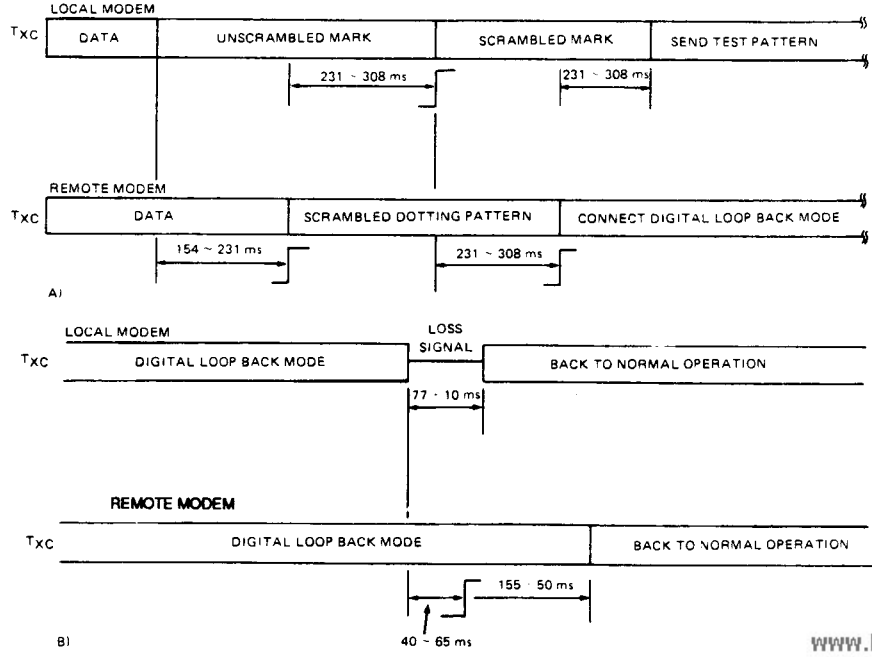


Figure 11. RDLB Initiation (A) and Termination (B)

XR-2400 / MICROCONTROLLER INTERFACING

The XR-2400 looks as a memory peripheral to a host microcontroller. The following indicates the address locations with bit functions of XR-2401 registers.

Location 60H - CNTRL 0

Bit	Description
0	TXL1
1	TXL2
2	TXL3
3	SPKR On / Off (O = Off)
4	TST1 (EXAR Special Test Mode)
5	TST2 (EXAR Special Test Mode)
6	SPKR1 Speaker Control LSB
7	SPKR2 Speaker Control MSB

Location 61H - CNTRL 1

0	OPTD
1	SP1
2	SP2
3	ETE
4	DLB
5	BC1
6	BC2
7	ASY

Bit 2	Bit 1	Bit 0	Transmit Level (±1 dB)
0	0	0	-10.5 dB
0	0	1	-9.0 dB
0	1	0	-7.5 dB
0	1	1	-6.0 dB
1	0	0	-4.5 dB
1	0	1	-3.0 dB
1	1	0	-1.5 dB
1	1	1	0

Bit 3	Speaker
0	OFF
1	ON

Bit 0	Async Data Rate
0	+1% to -2.5%
1	+2.3% to -2.5%

Bit 2	Bit 1	Receiver Speed
1	1	2400 BPS
0	1	1200 BPS
1	0	300 BPS

Bit 3	Transmit Clock
0	Internal
1	External

Bit 4	Bit Status	
0	Normal Data Mode	
1	Digital Loopback	TXCLK connect to RXCLK TXDATA connect to TXDATA

Bit 6	Bit 5	ASY Character Length
0	0	8 bit
1	0	9 bit
0	1	10 bit
1	1	11 bit

Bit 7	Mode
0	Synchronous
1	Asynchronous

Location 62H - CNTRL 2

0	TEN	Transmitter Enable (EN = 1)
1	SCR	Scrambler Enable (EN = 1)
2	64B	64 Bit Mark Sensor (EN = 1)
3	EQO	Adaptive Equalizer ON/OFF Control (ON @ 1)
4	EQT	Adaptive Equalizer T or T/2 Select (T/2 = 1)
5	VBS	Transmitter Shaping Select. 1 = CCITT 75% square root raised cosine 0 = Bell shaping
6	ANT	Answer Tone Selection (0=2225 Hz / 1 = 2100 Hz)
7	REQ	Equalizer Reset Control (BS = 0)

Location 63H - CNTRL 3

0	FL	Fast Locking Control (FL = 1). At the beginning of communication FL is set to 1 for fast DPLL response to the incoming signal.
1	CRD	RXD Clamp Control (RXD = 1 when CRD = 1)
2	TSP	Transmit Clock Select (2400 BPS = 1 / 1200 BPS = 0)
3	TST4	EXAR SPECIAL TEST MODE, set to 0 for normal operation.
4	PTD	Parallel TXD Input Selection (Parallel = 1). TXD will be taken from the µc data bus.
5	NTD	Normal Data Mode TXD from RS232 when (NTD = 1). 0: TXDATA will be taken from the selection of TC1, TC2.
6	TC1	
7	TC2	

Bit 7	Bit 6	TXC (NTD = 0)
1	1	Dotting Pattern used for DLB/Self Test
0	1	300 Hz, used to Generate S1 Pattern
1	0	Mark (ones)
0	0	Space (zeros)

Location 64H - CNTRL 4

0	PDM	Power Down Mode (PD=1). During power down mode, only the analog portion of the XR-2402A is disabled. The digital portion will still be active waiting for a control signal from the µc.
1	MOD	Answer/Originate Mode (Ans = 1)
2	GTE	Guard Tone Enable (GT=1)
3	GTS	Guard Tone Selection (1800 Hz = 1 / 550 Hz = 0)
4	RCVG	Receive Filter Gain (6dB = 1, 16 dB = 0)
5	DMFM	DTMF Mode Control (DTMF=1)
6	CPD	Call Progress Tone Detect Mode (CPT = 1)
7	ALB	Analog Loopback Enable (ALB = 1)

Location 65H - CNTRL 5

0	D1	Dial Digit 1
1	D2	Dial Digit 2
2	D3	Dial Digit 3
3	D4	Dial Digit 4
4	-	
5	-	
6	--	
7	-	

Location 66H - CNTRL 6 AGC Word

0	AG0	7 bits AGC control, each step is 0.375 dB
1	AG1	
2	AG2	
3	AG3	
4	AG4	
5	AG5	
6	AG6	
7	-	

Location 67H - CNTRL 7 Status Word

0	RXD	Receive Data
1	USD	Unscrambled Received Data
2	CD	Energy Detect
3	SGQ	Signal Quality Indicator

Location 69H - MODSEL

0	IDLE MODE
1	FSK MODE
2	PSK MODE
3	DTMF TONE MODE

A summary of control locations is given below in Table 6.

CNTRL	BIT 7	BIT 6	BIT5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CNTRL 0	-	TST3	TST2	TST1	SPC	TXL3	TLX2	TLX1
CNTRL 1	ASY	BC2	BC1	DLB	ETE	SP2	SP1	OPTD
CNTRL 2	REQ	ANT	VBS	EQT	EQO	64B	SCR	TEN
CNTRL 3	TC2	TC1	NTD	PTD	TST4	TSP	CRD	FL
CNTRL 4	ALB	CPDQ	DMFM	RCVG	GTS	GTE	MOD	PDM
CNTRL 5	-	-	-	-	DIAL DIGIT	DIAL DIGIT	DIAL DIGIT	DIAL DIGIT
CNTRL 6	-	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0
CNTRL 7	-	-	-	-	SGQ	CD	URXD	RXD

Table 6. Control / Status Locations

The following describes the read/write ports of the XR-2401 which is selected by PA0 ~PA2

Write Ports (WEN)

Port 0 — Write to XR-2402A DAC D0-D7

Port 3 — Write RXD to XR-2402A D0-RXD
D1 - Underscrambled RXD
D2 - CD
D3 - Equalizer Crash Indicator

Port 4 — Write AGC Gain to XR-2402A/
Reset RX600 FLAG 6 D0 - D6

Port 5 — Write PLL Information to XR 2402
D0 -Late/Early (L/E) Information

Port 6 — Write Eye Pattern Information D0 - D15

Port 7 — Write Data to XR-2402A D0 - D7

Read Ports (DEN)

Port 0 — Read Status from XR-2401 and XR-2402A
D0 - RX9600 Hz Ready
D1 - TX9600 Hz Ready
D2 - RX600 Hz Ready
D3 - TXD Ready
D4 - RXD Ready
D5 - TX600 Hz Ready
D6 -
D7 - Write Register Ready

Port 1 — Read Serial TXD from XR-2402A

Port 3 — Read Converted Signal from A/D on XR-2402A D0 - D7

Port 4 — Read Address Information from XR-2402A D0 - D7

Port 5 — Read "Write Register" Data from XR-2402A D0 - D7

Port 6 — Output Dummy to Reset TX600 Flag

The following illustrates the 8031 type microcontroller read/write of the XR-2401.

1. Read Target Address #60H in XR-2401:

```
MOV  A,#60H  ; Set up target address for XR-2401
MOV RO,#00   ; Set up RO for external memory
                 read
MOVX@RO,A ;  Move target address to address
                 register
           ;  After this instruction will poll the
           ;  interrupt for XR-2401
NOP        ;  These NOP ensure there is 3 µs
NOP        ;  for data setting
MOV RO,#02 ;  Put #02 in RO
MOVX A,@RO;  Move data read data register
```

2. Write Data #AA to target Address #60H in XR-2401:

```
MOV A,#AA    ; Put desired data in accumulator
MOV RO,#01   ; Put #01 in RO
MOVX @RO,A ; Move #AA to write data register
MOV A,#60H   ; Move target address #60 to
               accumulator
MOV RO,#00   ; Put #00 in RO
MOVX @RO,A ; Move target address to address
               register
```

After 6 microseconds, the XR-2401 will take data from the XR-2402A to finish the write cycle.

Note: In order to maintain proper operation, there are some limitations on read/write access for the XR-2401. In normal operation (excluding idle mode), more than one access within 100 microseconds is not allowed.

Figure 12 illustrates the read/write data timing to the XR-2400.

APPLICATIONS INFORMATION

Figure 17 shows the XR-2401/XR-2402A in a complete stand alone V.22 bis modem. In this system, an 8031 type µC is used for providing the handshake and command set control. The 2764 EPROM would hold the command set, with the 373 necessary to interface the 8031 to the 2764.

Special attention should be followed in system grounding. The analog and digital grounds should be single point connected at the power supply.

Figure 18 shows XR-2401/XR-2402A in a complete internal V.22bis modem.

Signal Constellation Monitor Circuit

For system testing and evaluation, it is often instructive to evaluate the signal constellation of the modem. During design and testing, the constellation provides useful information on demodulation quality. The circuit in Figure 13 provides an output which can be displayed on an oscilliscope. The general characteristics of the signal constellation is illustrated in Figure 14.

SYSTEM PERFORMANCE

Test set-up conditions shown on page 3, Figure 1.

Data quality is illustrated in figures 15 and 16 for 2400 BPS and 1200 BPS operation.

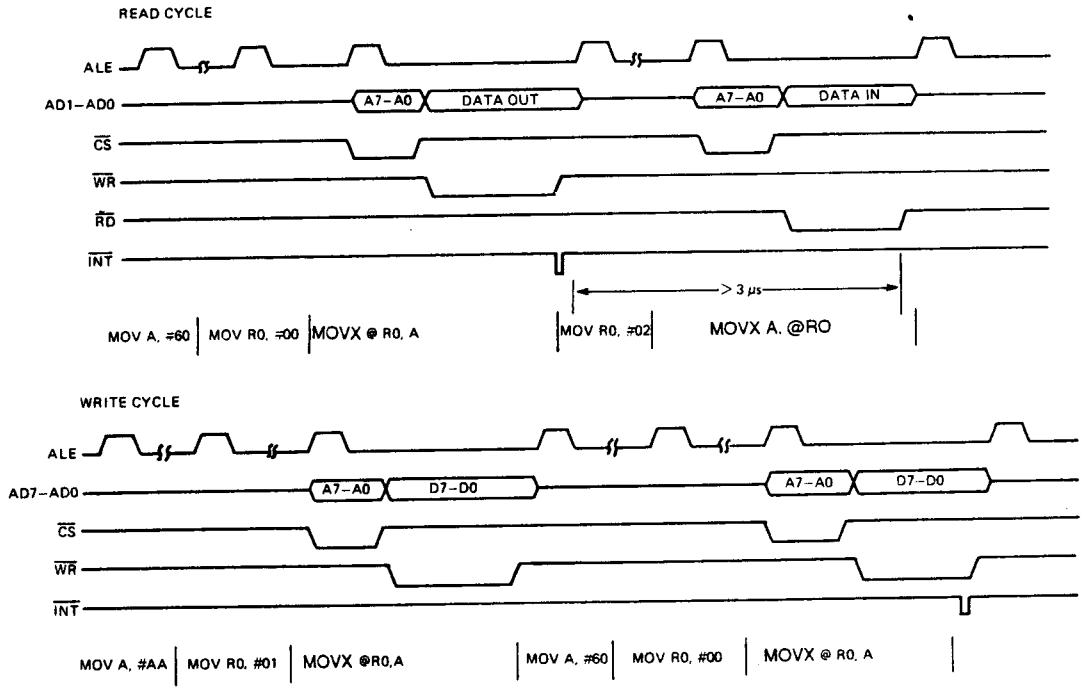


Figure 12. Timing for XR-2400 Read/Write Data

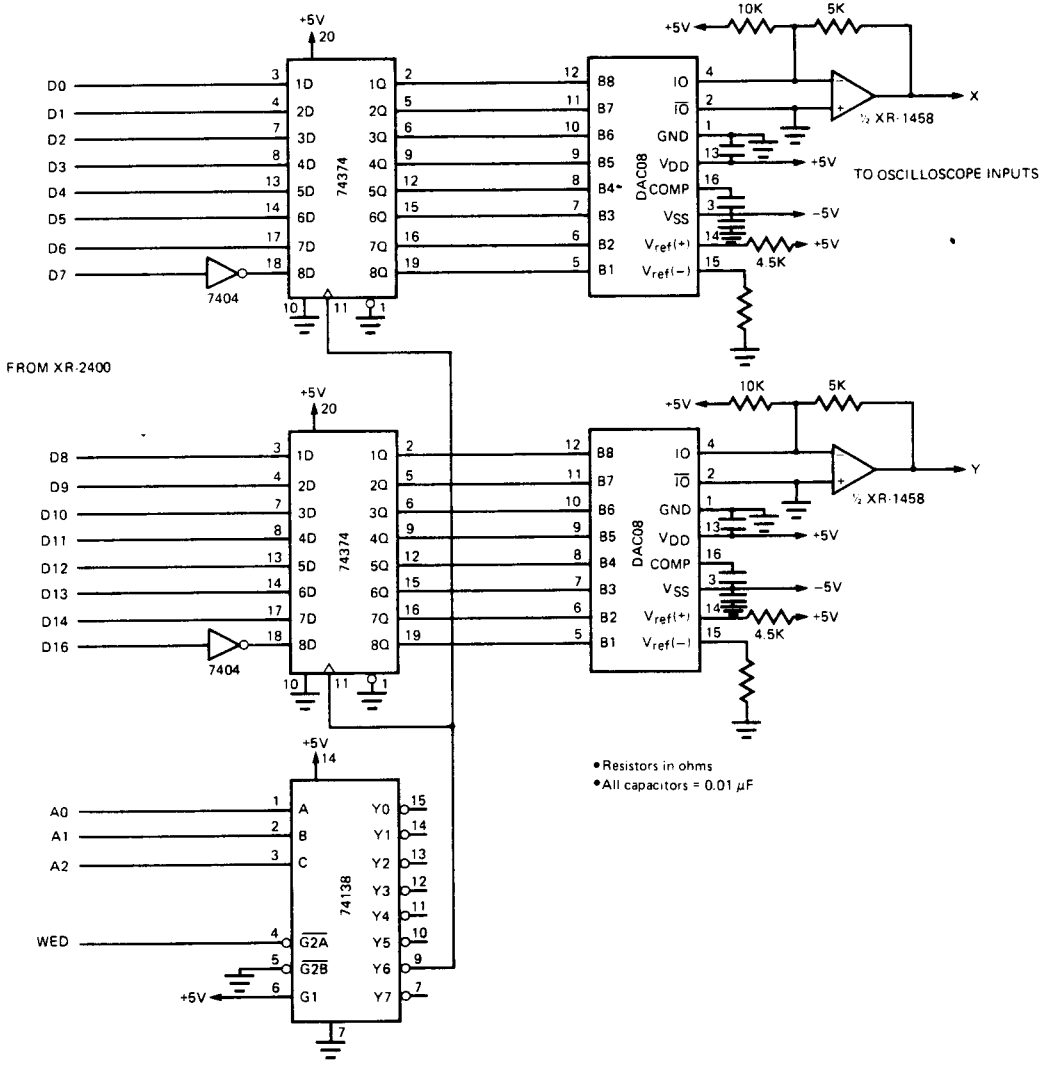


Figure 13. Signal Constellation Monitor

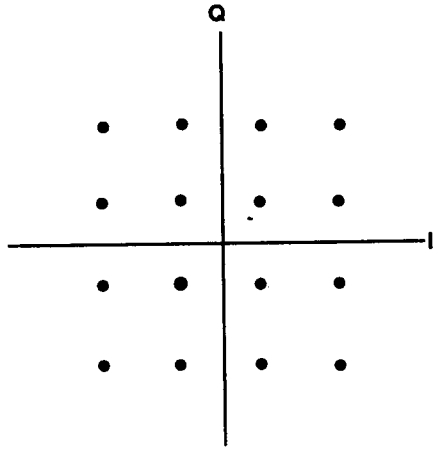


Figure 14. General Characteristics of 16 Point Constellation at 2400 BPS Q I

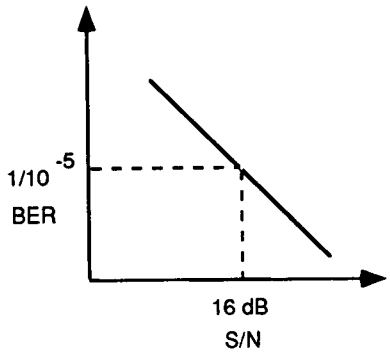


Figure 15. 2400 BPS BER vs. S/N

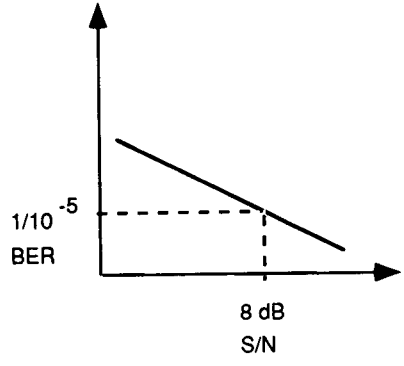


Figure 16. 1200 BPS BER vs. S/N