Octal transceiver with parity generator/checker (3-State)

54ABT657

FEATURES

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +48mA/–24mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 54ABT657 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT657 is an octal transceiver featuring non–inverting buffers with 3–State outputs and an 8–bit parity generator/checker, and is intended for bus–oriented applications. The buffers have a guaranteed current sinking capability of 48mA. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active–High) enables data from A ports to B ports; Receive (active–Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$ = High) and an input when receiving from port B to A port (T/$\overline{R}$ = Low). When transmitting (T/$\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$ = Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

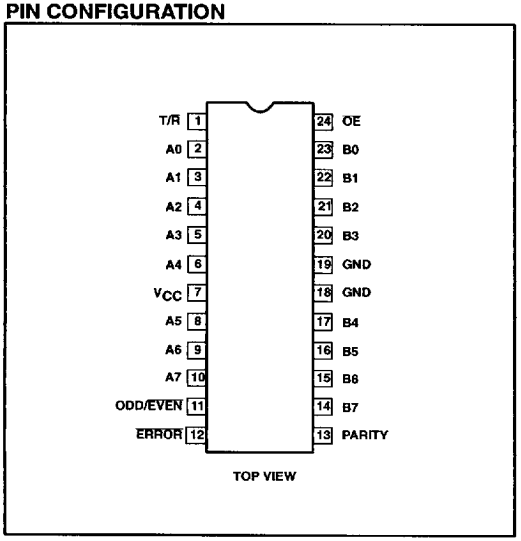
(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

ORDERING INFORMATION

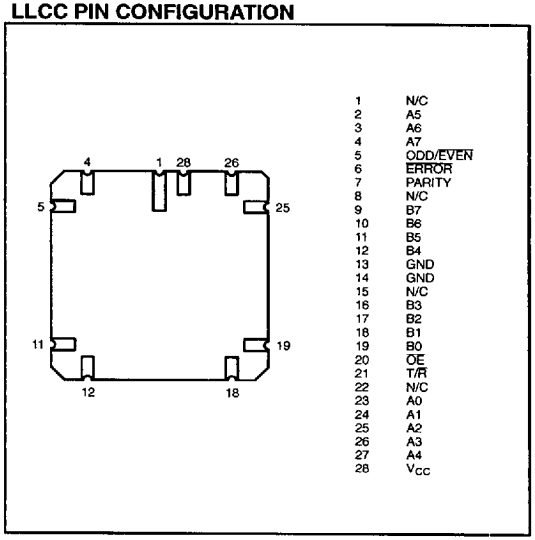
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24–pin Ceramic DIP	54ABT657/BLA	GDIP3-T24
28–pin Ceramic LLCC	54ABT657/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

PIN CONFIGURATION



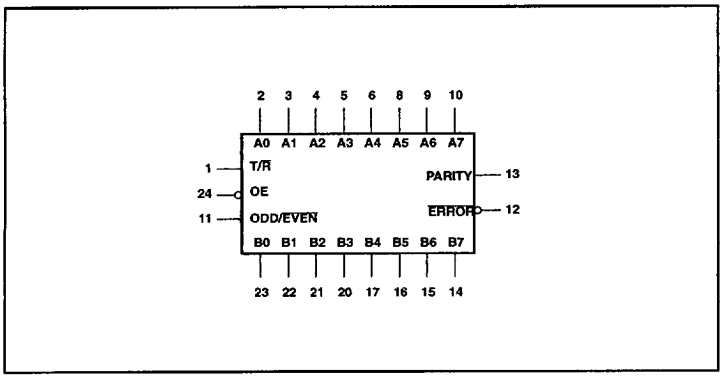
LLCC PIN CONFIGURATION



Octal transceiver with parity generator/checker (3-State)

54ABT657

LOGIC SYMBOL



PIN DESCRIPTION

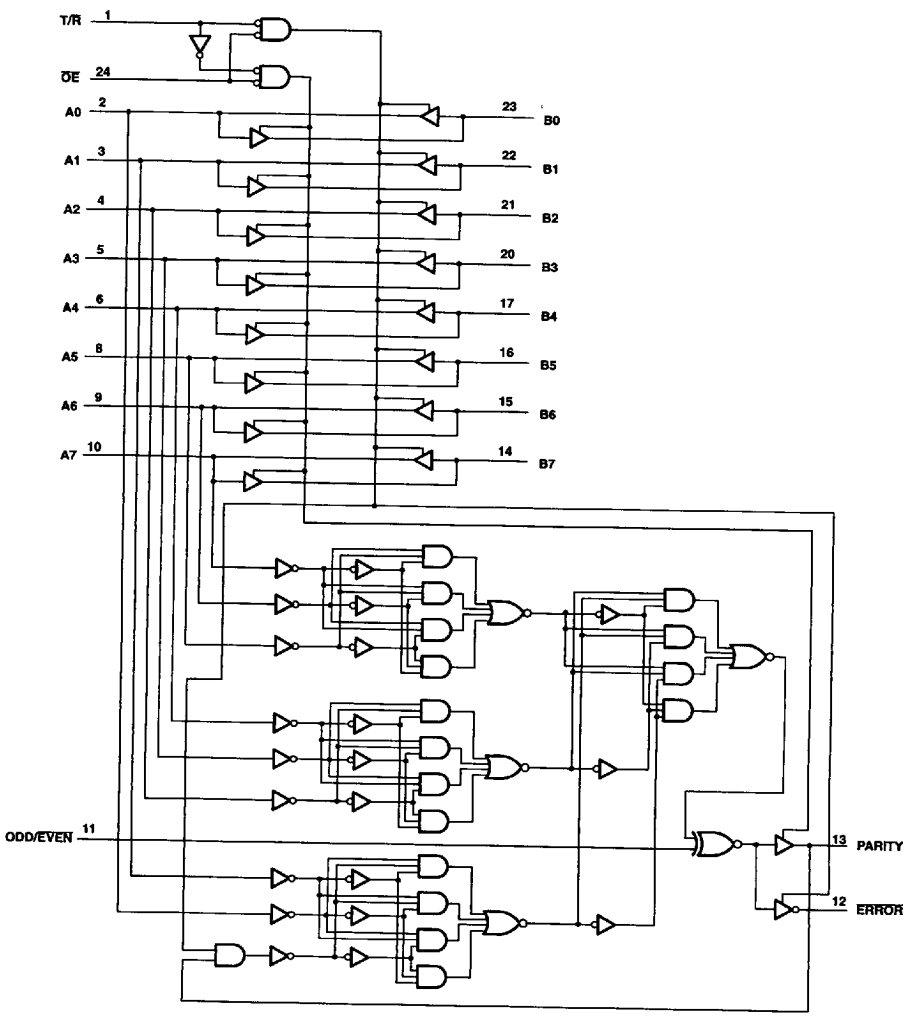
SYMBOL	PIN NUMBER	NAME AND FUNCTION
13	PARITY	Parity output
11	ODD/$\overline{\text{EVEN}}$	Parity select input
12	$\overline{\text{ERROR}}$	Error output
1	T/$\overline{\text{R}}$	Transmit/receive input
2, 3, 4, 5, 6, 8, 9, 10	A0 – A7	A port 3–State outputs
23, 22, 21, 20, 17, 16, 15, 14	B0 – B7	B port 3–State outputs
24	$\overline{\text{OE}}$	Output enable input (active–Low)
18, 19	GND	Ground (0V)
7	V_{CC}	Positive supply voltage

FUNCTION TABLE

NUMBER OF HIGH INPUTS	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{\text{OE}}$	T/$\overline{\text{R}}$	ODD/$\overline{\text{EVEN}}$	PARITY	$\overline{\text{ERROR}}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3–State

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	96	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High–level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High–level output current		–24	mA
I_{OL}	Low–level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free–air temperature range	–55	+125	°C

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: V_{CC} = MAX, $V_I = V_{IL}$ or V_{IH}, T_{amb} = –55 to +125°C)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA	2.5	3.5		V
			V_{CC} = 4.5V; I_{OH} = –24mA	2.0	2.6		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 48mA		0.42	0.55	V
I_I	Input leakage current	Control pins	V_I = GND or 5.5V		±0.01	±1.0	µA
		Data pins[3]	V_I = GND or 5.5V		±5	±100	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_O = 2.7V; $V_I = V_{IL}$ or 3.0V		5.0	50	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_O = 0.5V; $V_I = V_{IL}$ or 3.0V		–5.0	–50	µA
I_O	Output current[1]		V_O = 2.5V, V_I = GND or V_{CC}	–50	–80	–180	mA
I_{CCH}	Quiescent supply current		Outputs High, V_I = GND or V_{CC}		50	250	µA
I_{CCL}			Outputs Low, V_I = GND or V_{CC}		20	30	mA
I_{CCZ}			Outputs 3–State; V_I = GND or V_{CC}		50	250	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.

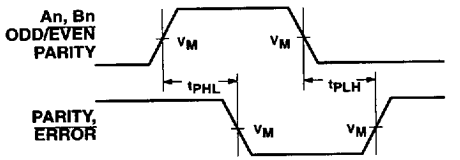
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

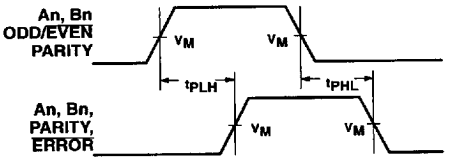
SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –55 to +125°C, V_{CC} = +5.0V +10%		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.1 1.2	3.3 3.0	5.0 4.3	0.8 0.8	5.5 4.8	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1, 2	2.5 2.8	6.5 7.0	8.7 9.1	2.2 2.7	10.1 10.6	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	1, 2	1.7 1.9	5.0 5.0	6.6 6.6	1.7 1.8	7.3 7.3	ns
t_{PLH} t_{PHL}	Propagation delay Bn to $\overline{\text{ERROR}}$	1, 2	3.9 4.0	9.2 9.6	11.7 12.1	3.9 4.0	13.8 14.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	1, 2	2.7 3.2	6.0 6.4	7.6 8.0	2.7 3.2	9.4 9.4	ns
t_{PZH} t_{PZL}	Output enable time[1] to High or Low level	3 4	1.3 1.9	3.8 4 4	5.6 7.0	0.9 1.5	6.6 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	3 4	2.4 2.7	5.1 5.4	7.0 7.6	2.0 2.5	7.7 8.2	ns

NOTES:
1. These delay times reflect the 3–State recovery time only and do not include the delay through the buffers and the parity check circuitry which affect the $\overline{\text{ERROR}}$ output. To assure *valid* information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output. *Valid* data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY).

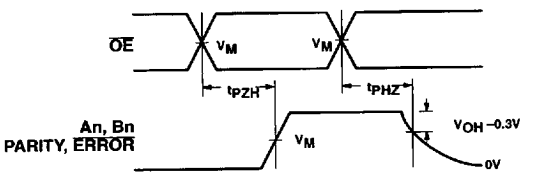
AC WAVEFORMS



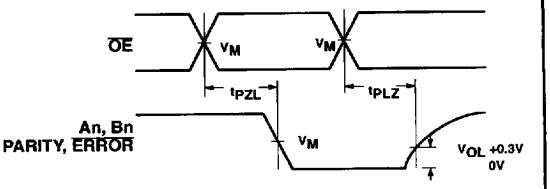
Waveform 1. Propagation Delay For Inverting Output



Waveform 2. Propagation Delay for Non-inverting Output



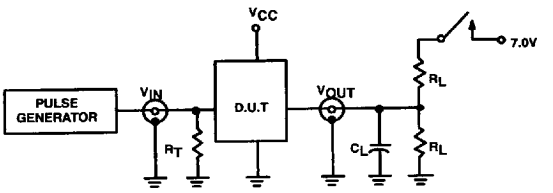
Waveform 3. 3–State Output Enable Time to High Level and Output Disable Time from High Level



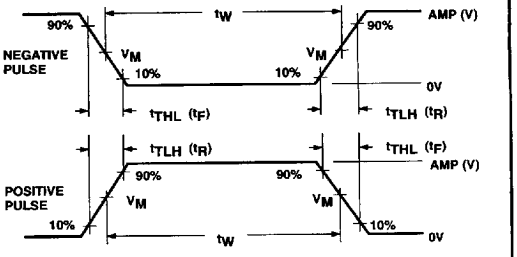
Waveform 4. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3–State Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.