REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	26	27						
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
02-04-04

REVISION LEVEL

MICROCIRCUIT, DIGITAL, ASIC, SINGLE POINT TO POINT IEEE 1355 HIGH SPEED CONTROLLER, MONOLITHIC SILICON

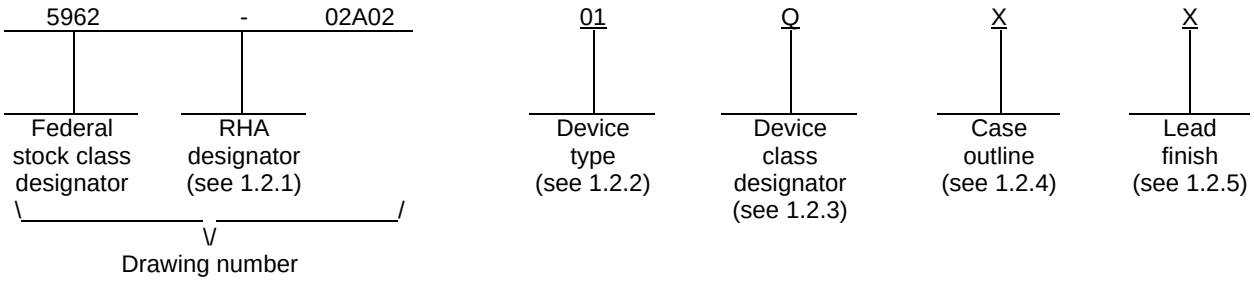
SIZE	CAGE CODE	
A	**67268**	**5962-02A02**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	T7906E	IEEE1355 high speed controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	100	Square Quad Flat Package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings 1/ 2/

Supply voltage range (V_{DD}) ..... -0.5 V to 7.0 V
Input voltage range (V_{IN}) ..... -0.5 V to V_{DD} + 0.5 V 3/
Input current (I_{IN})
Signal pin ..... -10 mA to 10 mA
Power pin ..... -50 mA to 50 mA
Output short circuit current 4/
V_{OUT} = V_{DD} ..... 160 mA
V_{OUT} = V_{SS} ..... -130 mA
Lead temperature (soldering, 10 sec) ..... 300°C 5/
Storage temperature ..... -65°C to 150°C
Maximum junction temperature (T_J) ..... 175°C

1.4 Recommended operating conditions.

Supply voltage range ..... 4.5 V to 5.5 V
Case operating temperature (T_C) ..... -55°C to 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to ground unless otherwise specified
3/ V_{DD} + 0.5 V shall not exceed 7.0 V
4/ The maximum output current of any single output in a shorted condition for a maximum duration of 1 second.
5/ Duration 10 s max at a distance not less than 1.6 mm.

2.2 Non Government Publications. The following document(s) form a part of this document to the extent specified herin. Unless otherwise specified, the issues of the documents(s) which are DOD adopted are those listed in the DODISS cited in the solicitation

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1355 - IEEE Standard for Heterogeneous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction.

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronic Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be specified in figure 4.

3.2.5 JTAG timing waveforms. The JTAG timing waveforms shall be as specified on figure 5.

3.2.6 Boundary Scan Instruction Codes. The boundary scan instruction codes shall be maintained and available from the device manufacturer upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. All device types shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10 % unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input clamp voltage to GND 1/	V_{IC}	I_{OH} = -300 µA	1, 2, 3	-1.2	-0.2	V
Low level input current 2/	I_{IL}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	-10		µA
Low level input current, pull-up 2/	I_{ILPU}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	-250		µA
Low level input current, pull-down 2/	I_{LLPD}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	-10		µA
High level input current 2/	I_{IH}	V_{IN} = V_{DD} = 5.5 V	1, 2, 3		10	µA
High level input current, pull-up 2/	I_{IHPU}	V_{IN} = V_{DD} = 5.5 V	1, 2, 3		10	µA
High level input current, pull-down 2/	I_{IHPD}	V_{IN} = V_{DD} = 5.5 V	1, 2, 3		450	µA
Output leakage low current 2/	I_{OZL}	Outputs disabled, V_{OUT} = GND	1, 2, 3	-10		µA
Output leakage high current pull-down output 2/	I_{OZHPD}	Outputs disabled, V_{OUT} = V_{DD}	1, 2, 3		450	µA
Output leakage low current pull-up output 2/	I_{OZLPU}	Outputs disabled, V_{OUT} =GND	1, 2, 3	-250		µA
Output leakage high current 2	I_{OZH}	Outputs disabled, V_{OUT} = V_{DD}	1, 2, 3		10	µA
Low level input voltage 1/	V_{IL}	Functional verification	1, 2, 3		0.8	V
High level input voltage 1/	V_{IH}	Functional verification	1, 2, 3	2.2		V
Low level output voltage 2/ 4/	V_{OL}	V_{DD} = 4.5 V, I_{OL} = + 3, + 6, + 12 mA	1, 2, 3		0.4	V
High level output voltage 2/ 4/	V_{OH}	V_{DD} = 4.5 V, I_{OH} = - 3, - 6, - 12 mA	1, 2, 3	3.9		V
Supply current at reset 3/	ICCRST	VCC=5.5V	1, 2, 3		15	mA
Supply current in idle 3/	ICCIDLE	VCC=5.5V	1, 2, 3		50	mA
Supply current at reset 2/	ICCOP	VCC=5.5V	1, 2, 3		80	mA
Input capacitance 3/	C_I	V_{DD} = 0 V	4		15	pF
Output capacitance 3/	C_{IO}	V_{DD} = 0 V	4		15	pF

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{DD} = 5.0\ V \pm 10\ \%$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
CLK period 3/	t_{CLK}	Nominal 5Mhz : 200ns	9,10,11			ns
CLK width high 3/	t_{CLKH}	See figure 4	9,10,11	80	120	ns
CLK width low 3/	t_{CLKL}	See figure 4	9,10,11	80	120	ns
$\overline{\text{RESET}}$ setup before CLK high 3/	t_{RSTS}	See figure 4	9,10,11	10		ns
$\overline{\text{RESET}}$ low pulse width 3/	t_{RSTW}	See figure 4	9,10,11	$2*t_{CLK}$		ns
Output disable after CLK high 3/	t_{OUTD}	See figure 4	9,10,11		38	ns
$\overline{\text{HSEL}}$ active low pulse width 3/	t_{HSL}	See figure 4	9,10,11	150		ns
$\overline{\text{HSEL}}$ inactive high pulse width 3/	t_{HSH}	See figure 4	9,10,11	60		ns
HWRnRD setup before $\overline{\text{HSEL}}$ active low 3/	t_{HWnRS}	See figure 4	9,10,11	5		ns
HDATnADR setup before $\overline{\text{HSEL}}$ active low 3/	t_{HWnRH}	See figure 4	9,10,11	5		ns
HWRnRD hold after $\overline{\text{HSEL}}$ inactive high 3/	t_{HWnRH}	See figure 4	9,10,11	0		ns
HDATnADR hold after $\overline{\text{HSEL}}$ inactive high 3/	t_{HDnAH}	See figure 4	9,10,11	0		ns
HDATA valid after HSEL active low and HWRnRD high 3/	t_{HDWV}	See figure 4	9,10,11		25	ns
HDATA hold after HSEL inactive high 3/	t_{HDWH}	See figure 4	9,10,11	0		ns
$\overline{\text{HSEL}}$ active low pulse width 3/	t_{HSL}	See figure 4	9,10,11	150		ns
$\overline{\text{HSEL}}$ inactive high pulse width 3/	t_{HSH}	See figure 4	9,10,11	60		ns
HWRnRD setup before $\overline{\text{HSEL}}$ active low 3/	t_{HWnRS}	See figure 4	9,10,11	5		ns
HDATnADR setup before $\overline{\text{HSEL}}$ active low 3/	t_{HWnRL}	See figure 4	9,10,11	5		ns
HWRnRD hold after $\overline{\text{HSEL}}$ inactive high 3/	t_{HWnRH}	See figure 4	9,10,11	0		ns
HDATnADR hold after $\overline{\text{HSEL}}$ inactive high 3/	t_{HDnAH}	See figure 4	9,10,11	0		ns
HDATA enable after $\overline{\text{HSEL}}$ active low and HWRnRD low 3/	t_{HDE}	See figure 4	9,10,11	4	18	ns

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10 % unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
HDATA valid after $\overline{\text{HSEL}}$ active low and HWRnRD low 3/	t_{HDV}	See figure 4	9,10,11		125	ns
HDATA hold after $\overline{\text{HSEL}}$ inactive high 3/	t_{HDH}	See figure 4	9,10,11	4	18	ns
$\overline{\text{HSEL}}$ active low pulse width 3/	t_{HSL}	See figure 4	9,10,11	150		ns
RAM I/F write access time 3/	t_{RWA}	See figure 4	9,10,11	120	120+(ws*40)	ns
$\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$ active low pulse width 3/	t_{RWL}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
Address ADDR0-15 valid before $\overline{\text{CSO}}$, $\overline{\text{WR}}$ active low 3/	t_{RWAS}	See figure 4	9,10,11	38	42	ns
Address ADDR0-15 hold after $\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$ inactive high 3/	t_{RWAH}	See figure 4	9,10,11	38	42	ns
DATA0-15 enable after $\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$ active low 3/	t_{RWDE}	See figure 4	9,10,11	0	6	ns
DATA0-15 valid before $\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$ inactive high 3/	t_{RWDV}	See figure 4	9,10,11	32		ns
DATA0-15 hold after $\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$ inactive high 3/	t_{RWDH}	See figure 4	9,10,11	20	26	ns
$\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and ADDR valid active low pulse width 3/	t_{RRL}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
$\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and ADDR valid inactive high pulse width 3/	t_{RRH}	See figure 4	9,10,11	38	40	ns
ADDRESS change 3/ 6/	t_{RRA}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
DATA0-15 setup before $\overline{\text{CSO}}$ -3, $\overline{\text{RD}}$ high or new address on ADDR0-15 valid 3/	t_{RDS}	See figure 4	9,10,11	14		ns
DATA hold after $\overline{\text{CSO}}$ -3, $\overline{\text{RD}}$ high or new address on ADDR0-15 3/	t_{RDH}	See figure 4	9,10,11	0	40	ns
$\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$, $\overline{\text{RD}}$, ADDR0-15 and DATA0-15 disable after $\overline{\text{BUS\_REQ}}$ active low 3/	t_{RBRS}	See figure 4	9,10,11	40	160	ns
$\overline{\text{CSO}}$ -3, $\overline{\text{WR}}$, $\overline{\text{RD}}$, ADDR0-15 and DATA0-15 enable after BUS_REQ inactive high 3/	t_{RBRA}	See figure 4	9,10,11	20	65	ns

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10 % unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
START_TRM high active pulse width 3/	t_{RETH}	See figure 4	9,10,11	47		ns
START_TRM low inactive pulse width 3/	t_{RETL}	See figure 4	9,10,11	47		ns
first read access ($\overline{CSO}$ -3/ $\overline{RD}$ low active) after START_TRM high 3/	t_{RETC}	See figure 4	9,10,11	120	7/	ns
TRM_RDY (transmit ready) high active after the last read from memory 3/	t_{RETR}	See figure 4	9,10,11	160	7/	ns
time between the rising edge of TRM_RDY and the next start (rising edge from START_TRM) 3/	t_{RETS}	See figure 4	9,10,11	0		ns
TRM_RDY hold after START_TRM high 3/	t_{RETD}	See figure 4	9,10,11		170	ns
START_RCV high active pulse width 3/	t_{RERH}	See figure 4	9,10,11	47		ns
START_RCV low inactive pulse width 3/	t_{RERL}	See figure 4	9,10,11	47		ns
first write access ($\overline{CSO}$ -3/ $\overline{WR}$ low active) after START_RCV high 3/	t_{RERC}	See figure 4	9,10,11	120		ns
RCV_RDY (receive ready) high inactive after the last write to memory 3/	t_{RERR}	See figure 4	9,10,11	160	170	ns
time between the rising edge of RCV_RDY and the next start (rising edge from START_RCV) 3/	t_{RERS}	See figure 4	9,10,11	0		ns
RCV_RDY hold after START_RCV high 3/	t_{RERD}	See figure 4	9,10,11		170	ns
$\overline{WR}$ active low pulse width 3/	t_{FWL}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
$\overline{WR}$ inactive high pulse width 3/	t_{FWH}	See figure 4	9,10,11	38	40	ns

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10 % unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{WR}$ active low after RCV_EOP_ACK high 3/	t_{FWACK}	See figure 4	9,10,11	120		ns
$\overline{FIFO\_FULL}$ setup before $\overline{WR}$ high 3/	t_{FFS}	See figure 4	9,10,11	8		ns
RCVEOP1, RCVEOP2 high after last write and $\overline{WR}$ high 3/	t_{FWEOP}	See figure 4	9,10,11	40	7/	ns
RCV_EOP_ACK active high pulse width 3/	t_{FWEOPA}	See figure 4	9,10,11	49		ns
RCVEOP1, RCVEOP2 low after RCV_EOP_ACK high 3/	t_{FWEOPH}	See figure 4	9,10,11		128	ns
DATA0-7 enable after $\overline{WR}$ 、low 3/	t_{FWDE}	See figure 4	9,10,11	0	6	ns
DATA0-7 valid before $\overline{WR}$ high 3/	t_{FWDV}	See figure 4	9,10,11	32		ns
DATA0-7 hold after $\overline{WR}$ high 3/	t_{FWDH}	See figure 4	9,10,11	2		ns
$\overline{RD}$ active low pulse width 3/	t_{FRL}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
$\overline{RD}$ inactive high pulse width 3/	t_{FRH}	See figure 4	9,10,11	38	40	ns
$\overline{FIFO\_EMPTY}$ setup before $\overline{RD}$ high 3/	t_{FES}	See figure 4	9,10,11	8		ns
TRM_EOP_ACKnowledge active high after TRMEOP1, TRMEOP2 high AND FIFO_EMPTY active low 3/	t_{FREOPA}	See figure 4	9,10,11	160	7/	ns
TRMEOP1, TRMEOP2 hold after TRM_EOP_ACK high 3/	t_{FREOPH}	See figure 4	9,10,11	0		ns
TRM_EOP_ACK hold after TRMEOP1, TRMEOP2 low 3/	t_{FRACKH}	See figure 4	9,10,11	122	128	ns
DATA0-7 setup before $\overline{RD}$ inactive high 3/	t_{FRDV}	See figure 4	9,10,11	9		ns
DATA0-7 hold after $\overline{RD}$ inactive high 3/	t_{FRDH}	See figure 4	9,10,11	0		ns
$\overline{ADC\_CS}$ low pulse width 3/	t_{ADCCS}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
ADC_RDY high pulse width 3/	t_{ADCRDY}	See figure 4	9,10,11	45		ns

See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10 % unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
ADC_RDY high to ADC_$\overline{R/C}$ high 3/	t_{ADCR}	See figure 4	9,10,11	200		ns
ADC_$\overline{R/C}$ setup before ADC_$\overline{CS}$ low 3/	t_{ADCS}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
ADC_TRIG high pulse width 3/	$t_{ADCTRIG}$	See figure 4	9,10,11	45		ns
ADC_TRIG high to ADC_$\overline{CS}$ low 3/	t_{ADCTCS}	See figure 4	9,10,11	200+(ws*40) 5/		ns
DATA 0-15 setup to ADC_$\overline{CS}$ high 3/	t_{ADCDS}	See figure 4	9,10,11	19		ns
DATA 0-15 hold after ADC_$\overline{CS}$ high 3/	t_{ADCDH}	See figure 4	9,10,11	0		ns
DAC_ADDR 0-2 and DATA 0-15 setup before DAC_$\overline{WR}$ low 3/	t_{DACS}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
DAC_$\overline{WR}$ low pulse width 3/	t_{DACWR}	See figure 4	9,10,11	40+(ws*40) 5/	42+(ws*40) 5/	ns
DATA 0-15 hold after DAC_$\overline{WR}$ high 3/	t_{DACH}	See figure 4	9,10,11	38	42	ns
TMRx_CLK period 3/	t_{TCLK}	See figure 4	9,10,11	80		ns
TMRx_CLK width high 3/	t_{TCLKH}	See figure 4	9,10,11	35	45	ns
TMRx_CLK width low 3/	t_{TCLKL}	See figure 4	9,10,11	35	45	ns
TMRx_EXP low / high after TMRx_CLK high 3/	t_{TEXP}	See figure 4	9,10,11	9	24	ns
EXT_IREQx low pulse width 3/	t_{EXINT}	See figure 4	9,10,11	10		ns
Bit Period 3/	t_{LBITP}	See figure 4	9,10,11	4		ns
LDOx, LSOx output skew 3/ 8/	t_{LOUTS}	See figure 4	9,10,11		0.5	ns
Data/Strobe edge separation 3/	t_{LDSI}	See figure 4	9,10,11	1		ns
TCK period 3/	t_{TCK}	See figure 5	9,10,11	100		ns
TCK width high 3/	t_{TCKH}	See figure 5	9,10,11	40		ns
TCK width low 3/	t_{TCKL}	See figure 5	9,10,11	40		ns
TMS, TDI setup before TCK high 3/	t_{TIS}	See figure 5	9,10,11	8		ns
TMS, TDI hold after TCK high 3/	t_{TIH}	See figure 5	9,10,11	8		ns
TDO delay after TCK low 3/	t_{TDO}	See figure 5	9,10,11		17	ns

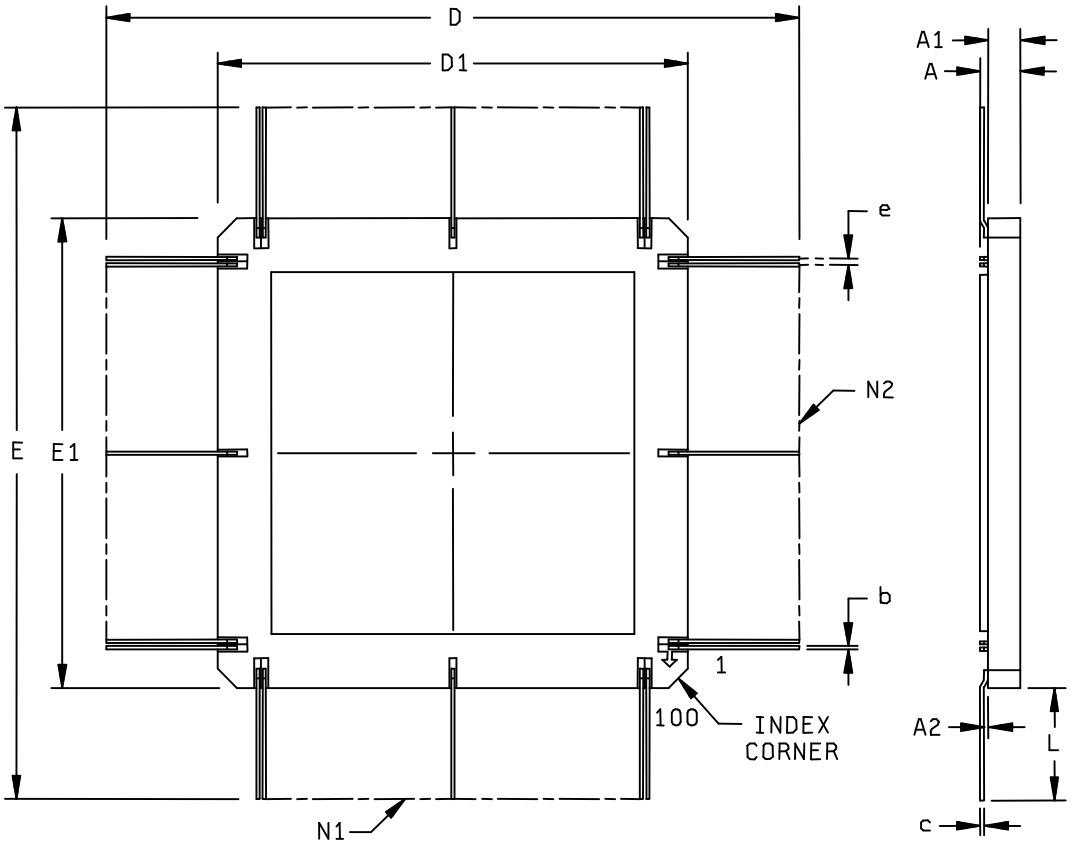
See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10 % unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
SMCS Inputs setup before TCK high 3/	t_{SYSS}	See figure 5	4	8		ns
SMCS Inputs hold after TCK high 3/	t_{SYSM}	See figure 5	4	8		ns
SMCS Outputs delay after TCK low 3/	t_{SYSO}	See figure 5	4		27	ns
TDO disable after $\overline{\text{TRST}}$ active low 3/	t_{TDOZ}	See figure 5	4		5	ns
$\overline{\text{TRST}}$ pulse width 3/	t_{TRST}	See figure 5	4	2 * t_{TCK}		ns

1/ Forcing conditions of the functional test, assure that these limits are met, but they will not be individually recorded.
2/ Read & record measurements in accordance with MIL-PRF-38535.
3/ Tested at initial design and after major process changes, otherwise guaranteed.
4/ I_{OL} and I_{OH} are based on buffer size.
5/ ws = wait state number. Wait state is defined in one register (called RAM_WS_REG) located at address OX42.
6/ Internal clock runs at 25MHz, t_{iclk} = 40 ns.
7/ Data bandwidth over the IEEE-1355 link. Simultaneous read from the memory with wait states.
8/ Output skew includes jitter.

Case X



Symbol	Milimeters		Inches	
	Min	Max	Min	Max
A	2.21	2.67	.087	.105
c	0.15	0.20	.006	.008
D/E	31.80	32.80	1.252	1.291
D1/E1	18.80	19.30	.740	.760
e	0.635 BSC		.025 BSC	
b	0.254 REF		.010 REF	
A1	1.83	2.24	.072	.088
A2	0.203 REF		.008 REF	
L	6.50	6.75	.256	.266
N1/N2	25		25	

Figure1. Case outline.

Pin Number	Name
1	V_{CC}
2	GND
3	GND
4	V_{CC}
5	LD0
6	LS0
7	LDI
8	LSI
9	GND
10	TCK
11	TMS
12	TDI
13	$\overline{\text{TRST}}$
14	TD0
15	GND
16	V_{CC}
17	IOB0
18	IOB1
19	IOB2
20	IOB3
21	IOB4
22	IOB5
23	IOB6
24	IOB7
25	IOB8
26	IOB9
27	V_{CC}
28	GND
29	IOB10
30	IOB11
31	IOB12
32	IOB13
33	IOB14
34	IOB15

Pin Number	Name
35	IOB16
36	IOB17
37	IOB18
38	IOB19
39	IOB20
40	IOB21
41	IOB22
42	IOB23
43	IOB24
44	IOB25
45	IOB26
46	IOB27
47	DATA0
48	DATA1
49	DATA2
50	DATA3
51	DATA4
52	DATA5
53	DATA6
54	DATA7
55	DATA8
56	V_{CC}
57	GND
58	DATA9
59	DATA10
60	DATA11
61	V_{CC}
62	GND
63	DATA12
64	DATA13
65	DATA14
66	DATA15
67	GPIO0
68	GPIO1

Pin Number	Name
69	GPIO2
70	GPIO3
71	GPIO4
72	GPIO5
73	GPIO6
74	GPIO7
75	TMR1_CLK
76	TMR2_CLK
77	RxD1
78	TMR1_EXP
79	TMR2_EXP
80	TxD1
81	HDATA0
82	HDATA1
83	HDATA2
84	HDATA3
85	HDATA4
86	HDATA5
87	HDATA6
88	V_{CC}
89	GND
90	HDATA7
91	HDATNADR
92	$\overline{\text{HSEL}}$
93	HWRNRD
94	$\overline{\text{HINTR}}$
95	$\overline{\text{RESET}}$
96	CLK
97	GND
98	GND
99	V_{CC}
100	PLLOUT

Figure 2. Terminal connections.

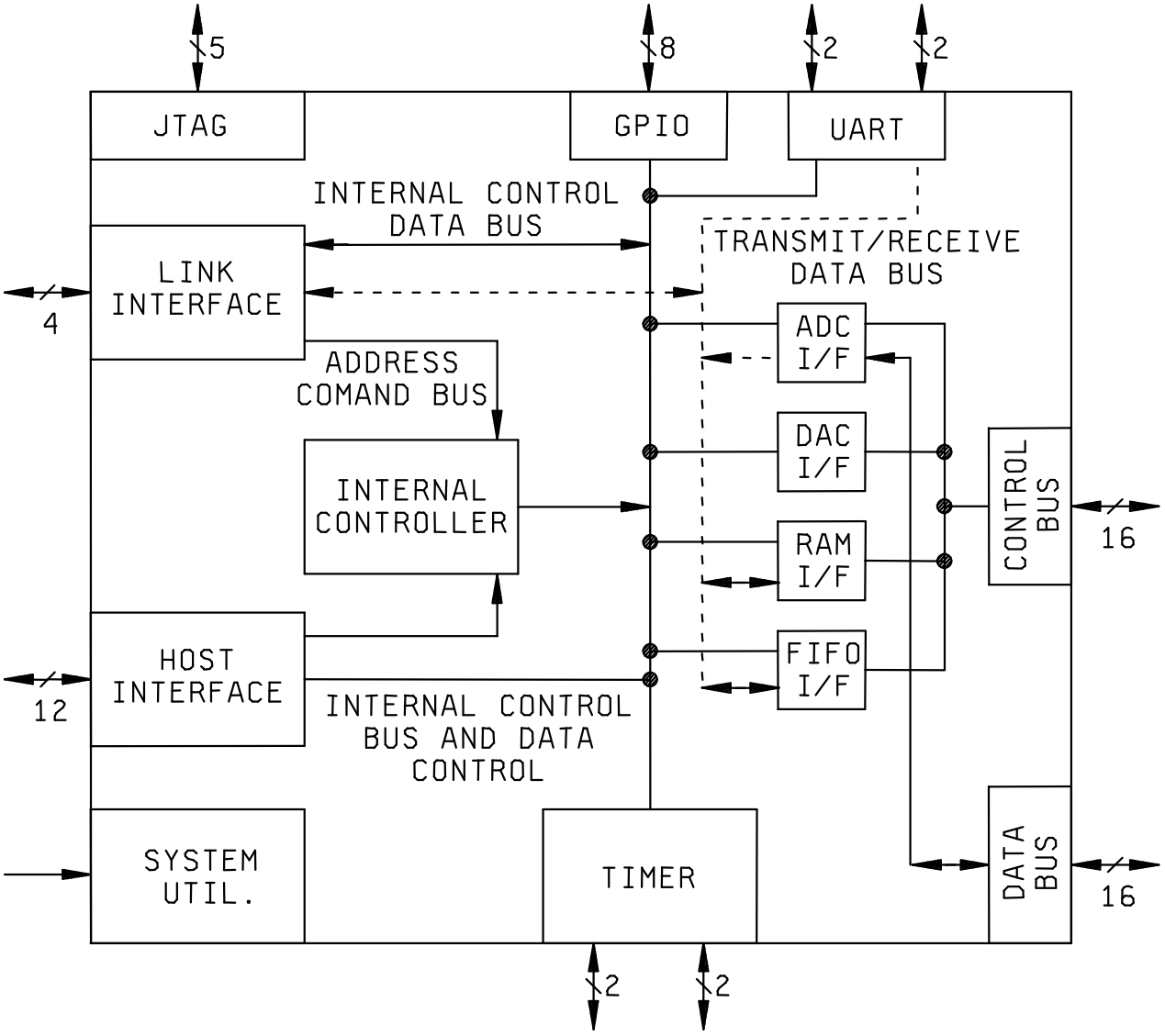


Figure 3. Block diagram.

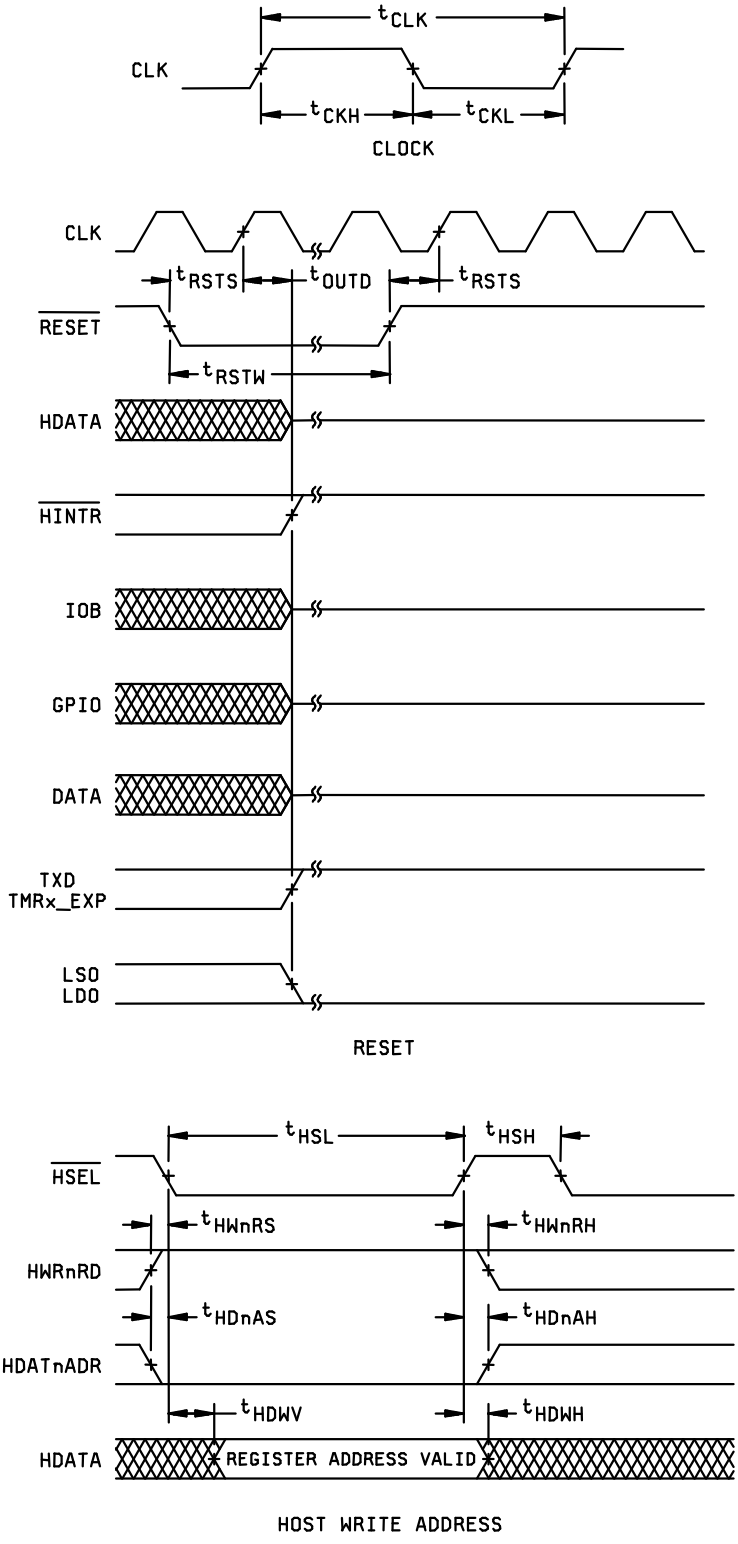
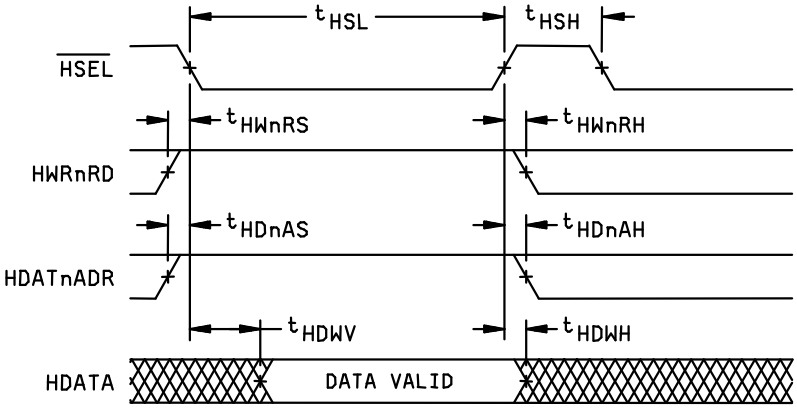
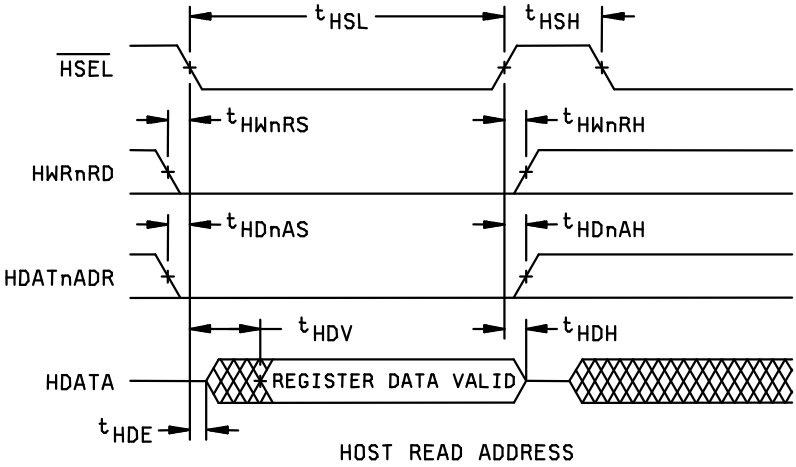


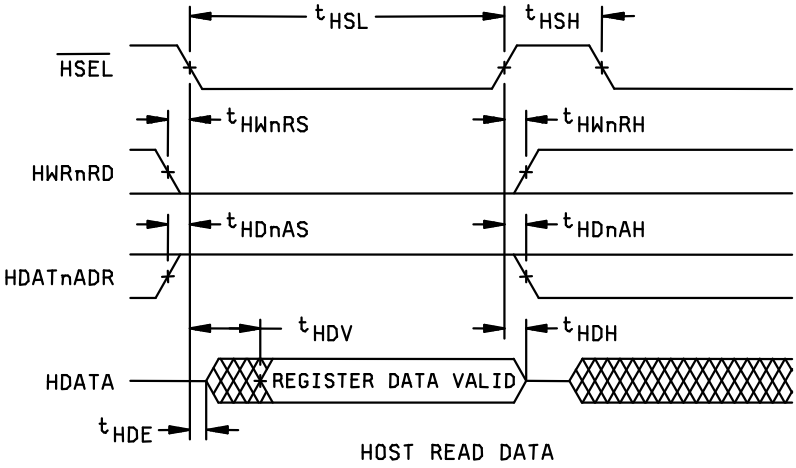
Figure 4. Timing waveforms.



HOST WRITE DATA

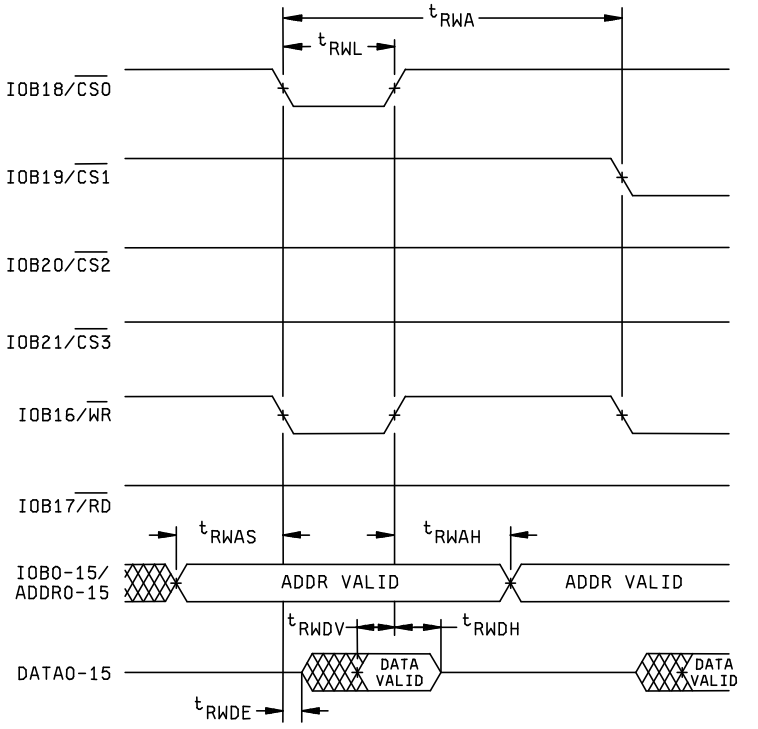


HOST READ ADDRESS

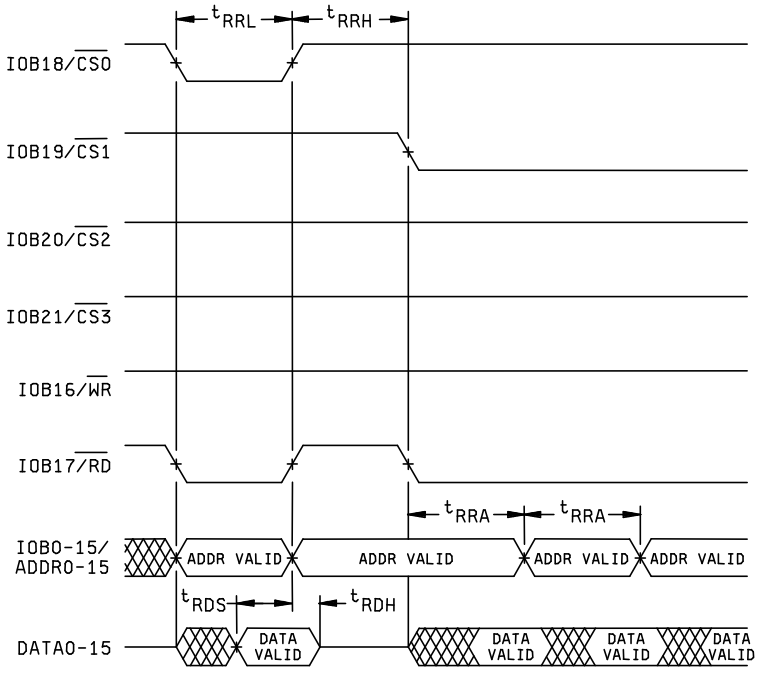


HOST READ DATA

Figure 4. Timing waveforms - Continued.

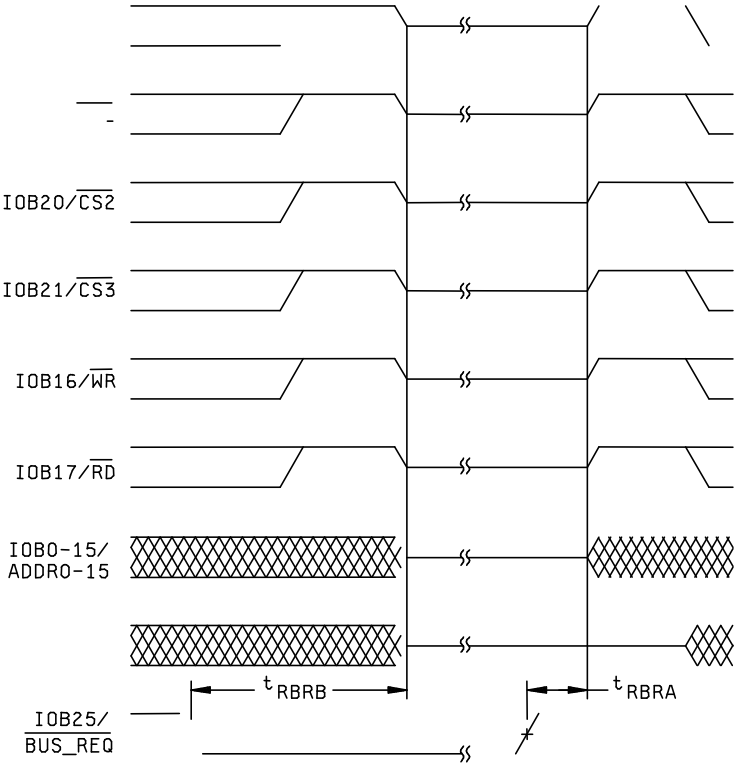


RAM INTERFACE WRITE

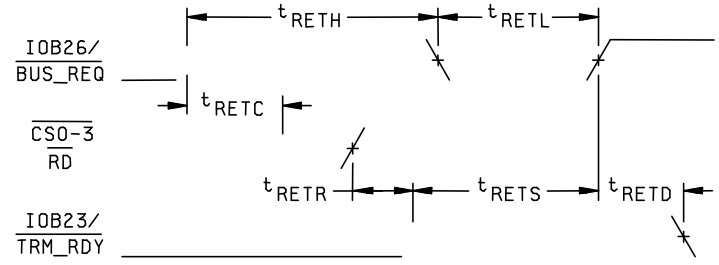


RAM INTERFACE READ

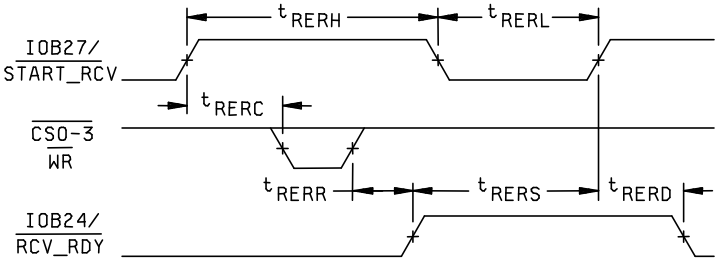
Figure 4. Timing waveforms - Continued.



RAM INTERFACE EXTERNAL BUS REQUEST



RAM INTERFACE EXTERNAL CONTROL READ



RAM EXTERNAL CONTROL WRITE

Figure 4. Timing waveforms - Continued.

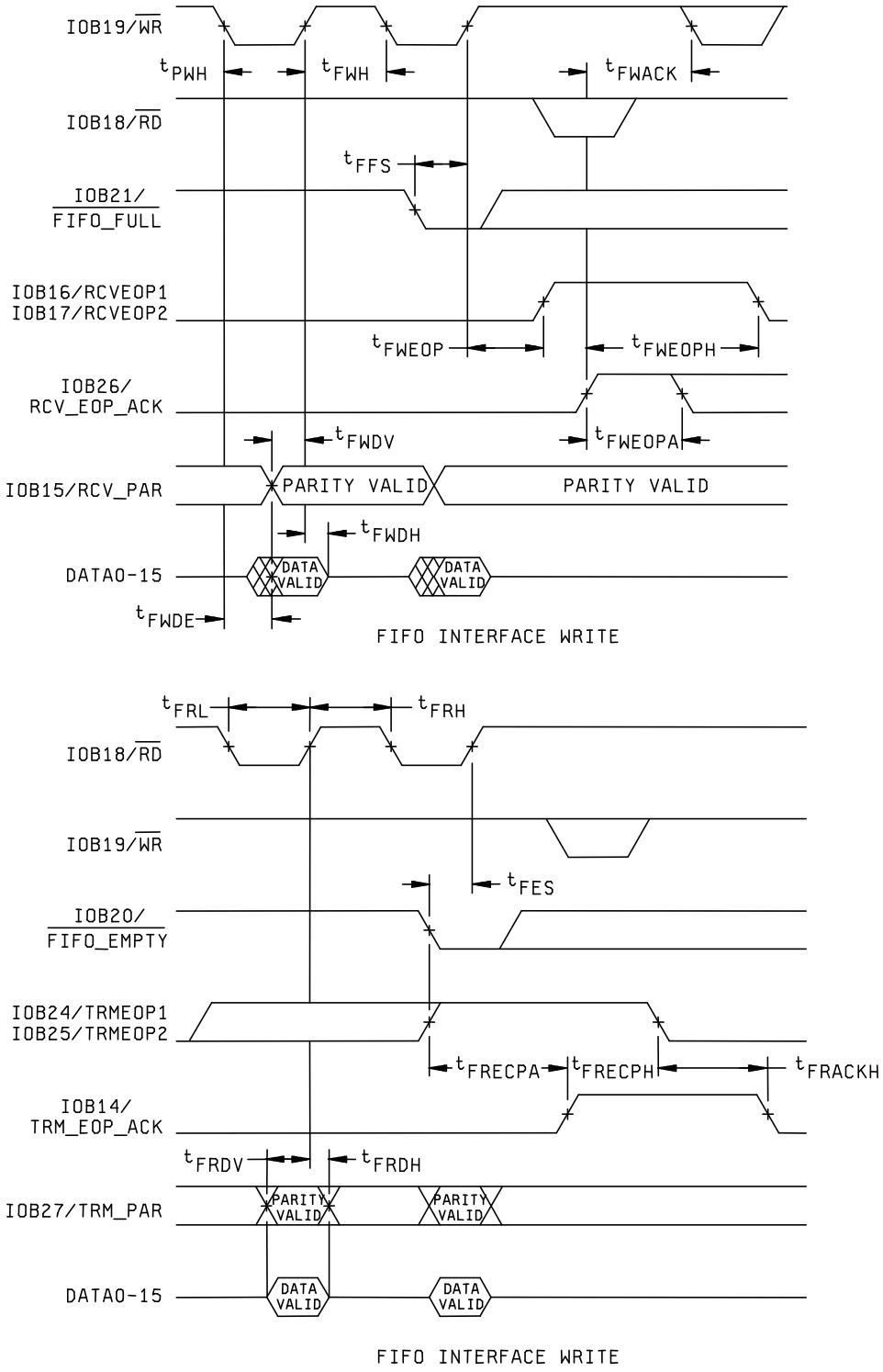
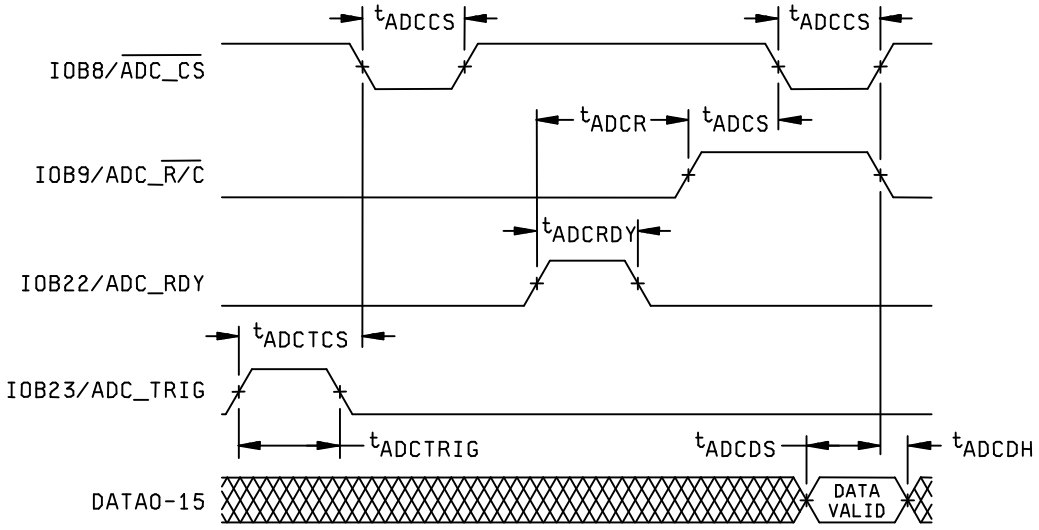
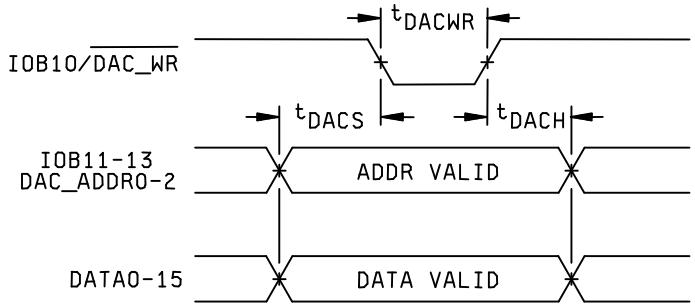


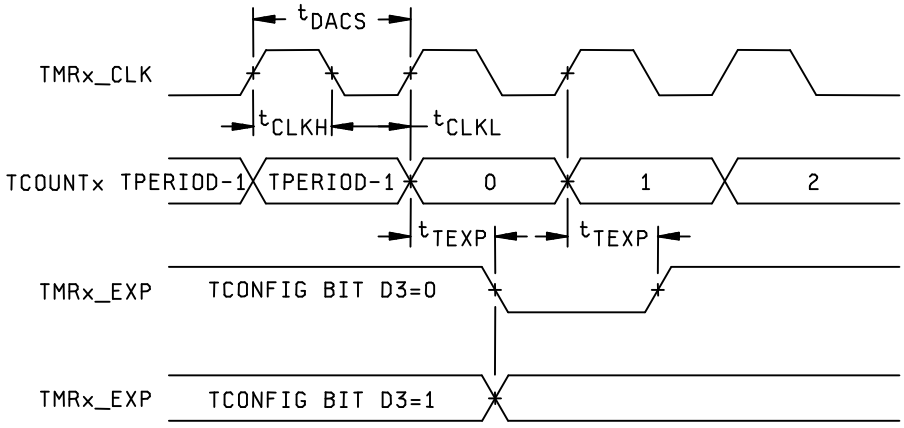
Figure 4. Timing waveforms - Continued.



ADC INTERFACE

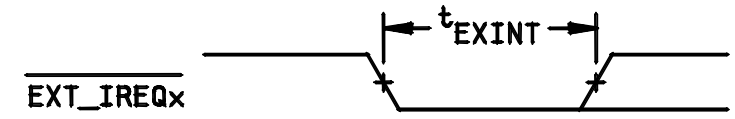


DAC INTERFACE

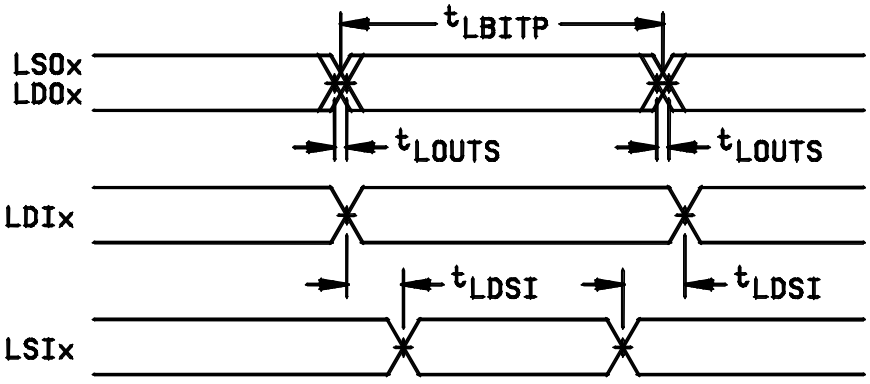


TIMER

Figure 4. Timing waveforms - Continued.



EXTERNAL INTERRUPT



LINKS

Figure 4. Timing waveforms - Continued.

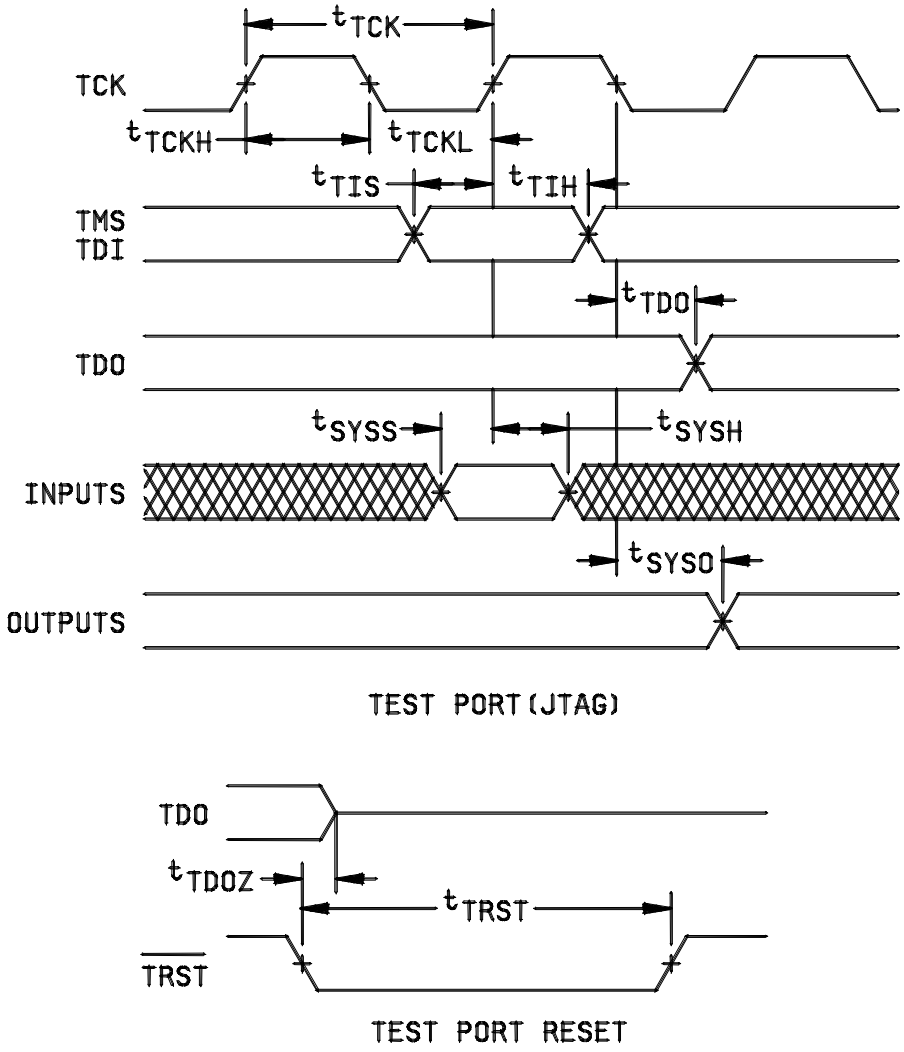


Figure 5. JTAG timing waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10, 11 1/	1,2,3,7,8,9,10, 11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11 1/	1,2,3,4,7,8,9, 10,11 1/	1,2,3,4,7,8,9,10, 11 2/
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits are as specified in table IIB herein and shall be required where specified in table I.

TABLE IIB. Delta limits

Parameter 1/	Symbol	Test Method	Test Conditions	Change limits	Unit
Low Level input current 2/	I_{IL}	As per Table I		± 0.1	µA
High level input current 2/	I_{IH}			± 0.1	µA
Output leakage low current 2/	I_{OZL}			± 0.1	µA
Output leakage high current 2/	I_{OZH}			± 0.1	µA
Low level output voltage	V_{OL}			± 100	mV
High level output voltage	V_{OH}			± 100	mV

1/ The parameters shall be recorded before and after the required burn-in and life test to determine the delta limits.
2/ Only for inputs and I/O without pull up or pull down.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Table III. Pin descriptions.

TDI-TEST DATA INPUT. Provides serial data for the boundary scan logic.

TDO-TEST DATA OUTPUT. Serial scan output of the scan path.

TCK-TEST CLOCK. Provides an asynchronous clock for JTAG boundary scan.

TMS-TEST MODE SELECT. Used to control the test state machine. This input should be left unconnected or tied to ground during normal operation.

TRST-TEST RESET. Resets the test state machine.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-04-04

Approved sources of supply for SMD 5962-02A02 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-02A0201QXC	F7400	T7906EKTMQ
5962-02A0201VXC	F7400	T7906EKTSV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes SA BP 70602 44306 Nantes Cedex 3 France