

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Inactive device 01 for new design. Add device 03. Upgrade to full military temperature range. Change drawing CAGE code. Editorial changes throughout.	88-04-15	W. Heckman
B	Add case outline Y. Editorial changes throughout.	89-09-08	W. Heckman
C	Add device types 02 and 03 for CAGE code 48257. Changed thermal resistance value in section 1.3. Changes to figure 1. Editorial changes throughout.	90-10-07	W. Heckman
D	Updated drawing to reference MIL-STD-1835. Made changes to table I. Modified figure 1, case outline Y. Editorial changes throughout.	93-03-10	Monica L. Poelking
E	Changes in accordance with NOR 5962-R222-93.	93-03-10	Monica L. Poelking
F	Add device 04. Editorial changes throughout.	94-08-05	Monica L. Poelking

CURRENT CAGE CODE 67268  
 THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS OF SHEETS	REV			F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Christopher A. Rauch	<b>DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>																	
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY William J. Johnson	<b>MICROCIRCUIT, DIGITAL, HCMOS, 32-BIT MICROPROCESSOR, MONOLITHIC SILICON</b>																	
	APPROVED BY William K. Heckman																		
	DRAWING APPROVAL DATE 25 February 1987	SIZE <b>A</b>	CAGE CODE 14933	<b>5962-86032</b>															
	REVISION LEVEL F	SHEET	1	OF	28														

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5962-E364-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	68020-12	HCMOS, 32-bit microprocessor
02	68020-16	HCMOS, 32-bit microprocessor
03	68020-20	HCMOS, 32-bit microprocessor
04	68020-25	HCMOS, 32-bit microprocessor

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CMGA5-P114	114	Pin grid array
Y	See figure 1	132	Square leaded chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.3 V dc to +7.0 V dc
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P <sub>D</sub> ) - - - - -	1.75 W
Lead temperature (soldering, 5 seconds) - - - - -	+270°C
Junction temperature (T <sub>J</sub> ) - - - - -	+150°C
Thermal resistance, junction to case (θ <sub>JC</sub> ):	
Case X - - - - -	See MIL-STD-1835
Case Y - - - - -	10 °C

1.4 Recommended operating conditions.

Supply voltage range (V <sub>DD</sub> ) - - - - -	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage (V <sub>IH</sub> ) - - - - -	2.0 V dc to V <sub>CC</sub> V dc
Low level input voltage range (V <sub>IL</sub> ) - - - - -	GND or -0.5 V dc to +0.8 V dc
Minimum high level output voltage (V <sub>OH</sub> ) - - - - -	2.4 V dc
Maximum low level output voltage (V <sub>OL</sub> ) - - - - -	0.5 V dc
Maximum low level output voltage (RESET only) - - - - -	0.8 V dc
Case operating temperature range (T <sub>C</sub> ) - - - - -	-55°C to +125°C
Frequency of operation:	
Device type 01 - - - - -	8.0 MHz to 12.5 MHz
Device type 02 - - - - -	8.0 MHz to 16.7 MHz
Device type 03 - - - - -	12.5 MHz to 20.0 MHz
Device type 04 - - - - -	12.5 MHz to 25.0 MHz

1/ Must withstand the added P<sub>D</sub> due to short circuit test; e.g., I<sub>OS</sub>.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-86032</b>
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
 MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be as specified on figure 1 and in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> 4.50 V ≤ V <sub>CC</sub> ≤ 5.50 V -55°C ≤ T <sub>C</sub> ≤ +125°C	Wave- form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
Output high voltage A0-A31, AS, BG, D0-D31, DBEN, DS, ECS, R/W, IPEND, OCS, RMC, SIZ0-SIZ1, FCO-FC2	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA		1, 2, 3	All	2.4		V
Output low voltage A0-A31, FCO-FC2, SIZ0-SIZ1, BG, D0-D31	V <sub>OL1</sub>	I <sub>OL</sub> = 3.2 mA		1, 2, 3	All		0.5	V
Output low voltage AS, DS, R/W, RMC, DBEN, IPEND	V <sub>OL2</sub>	I <sub>OL</sub> = 5.3 mA		1, 2, 3	All		0.5	V
Output low voltage ECS, OCS	V <sub>OL3</sub>	I <sub>OL</sub> = 2.0 mA		1, 2, 3	All		0.5	V
Output low voltage HALT	V <sub>OL4</sub>	I <sub>OL</sub> = 10.7 mA		1, 2, 3	All		0.5	V
Output low voltage RESET	V <sub>OL5</sub>	I <sub>OL</sub> = 10.7 mA		1, 2, 3	All		0.8	V
Input high voltage	V <sub>IH</sub>			1, 2, 3	All	2.0	V <sub>CC</sub>	V
Input low voltage	V <sub>IL</sub>			1, 2, 3	All	GND -0.5	0.8	V
Input leakage current, BERR, BR, BGACK, CLK, IPL0-IPL2, AVEC, CDIS, DSACK0, DSACK1	I <sub>IN1</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		1, 2, 3	All	-1.0	1.0	μA
Input leakage current HALT, RESET	I <sub>IN2</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		1, 2, 3	All	-2.5	2.5	μA
HI-Z (off-state) leakage current A0-A31, AS, DBEN, DS, D0-D31, FCO-FC2, R/W, RMC, SIZ0-SIZ1	I <sub>TSI</sub>	2.4 V or 0.5 V		1, 2, 3	All	-2.5	2.5	μA
Supply current <sup>2/</sup>	I <sub>CC</sub>	V <sub>CC</sub> = 5.50 V		1, 3 2	All		333 220	mA
Capacitance	C <sub>IN</sub>	See 4.3.1b, V <sub>IN</sub> = 0, see 4.3.1c, T <sub>C</sub> = +25°C, f <sub>IN</sub> = 1 MHz		4	All		20.0	pF
Functional testing		See 4.3.1d		7, 8	All			

See footnotes at end of table.

STANDARD  
MICROCIRCUIT DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $\frac{1}{4.50 \text{ V} \leq V_{CC} \leq 5.50 \text{ V}}$ $\frac{2}{-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}}$	Wave- form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
Frequency of operation	f	$\frac{3}{V_{CC} = 4.5 \text{ V}}$		9, 10, 11	01 02 03 04	8 8 12.5 12.5	12.5 16.7 20.0 25.0	MHz
Cycle time	t <sub>CYC</sub>		1	9, 10, 11	01 02 03 04	80 60 50 40	125 125 80 80	ns
Clock pulse width	t <sub>CL</sub> , t <sub>CH</sub>		2, 3	9, 10, 11	01 02 03 04	32 24 20 19	87 95 54 61	ns
Clock rise and fall times	t <sub>CR</sub> , t <sub>CF</sub>		4, 5	9, 10, 11	01-03 04		5 4	ns
Clock high to ADDRESS/FC/ SIZE/RMC valid	t <sub>CHAV</sub>		6	9, 10, 11	01 02 03-04	0 0 0	40 30 25	ns
Clock high to $\overline{\text{ECS}}$ , $\overline{\text{OCS}}$ asserted	t <sub>CHEV</sub>		6a	9, 10, 11	01 02 03 04	0 0 0 0	30 20 15 12	ns
Clock HIGH to ADDRESS, DATA, FC, RMC, SIZE, HI-Z	t <sub>CHAZx</sub>		7 5/		01 02 03 04	0 0 0 0	80 60 50 40	ns
Clock high to ADDRESS/FC/ SIZE/RMC invalid	t <sub>CHAZn</sub>		8	9, 10, 11	A11	0		ns
Clock low to $\overline{\text{AS}}$ , $\overline{\text{DS}}$ asserted	t <sub>CLSA</sub>		9	9, 10, 11	01 02 03 04	3 3 3 3	40 30 25 18	ns
$\overline{\text{AS}}$ to $\overline{\text{DS}}$ assertion (READ) (SKEW)	t <sub>STSA</sub>		9a 6/	9, 10, 11	01 02 03-04	-20 -15 -10	20 15 10	ns
$\overline{\text{AS}}$ asserted to $\overline{\text{DS}}$ asserted (WRITE)	t <sub>SASA</sub>		9b 7/	9, 10, 11	01 02 03 04	42 37 32 27		ns
$\overline{\text{ECS}}$ width asserted	t <sub>ECSA</sub>		10	9, 10, 11	01 02 03-04	25 20 15		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4.50 V < V <sub>CC</sub> < 5.50 V -55°C ≤ T <sub>C</sub> ≤ +125°C	Wave- form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
$\overline{OCS}$ width asserted	t <sub>OCSA</sub>	3/ 4/ V <sub>CC</sub> = 4.5 V	10a	9, 10, 11	01 02 03-04	25 20 15		ns
$\overline{ECS}$ , $\overline{OCS}$ width negated	t <sub>CWN</sub>		10b 8/5/		01 02 03 04	20 15 10 5		ns
ADDRESS/FC/SIZE/RMC valid to AS (and DS asserted READ)	t <sub>AVSA</sub>		11	9, 10, 11	01 02 03 04	20 15 10 6		ns
Clock low to $\overline{AS}$ , $\overline{DS}$ negated	t <sub>CLSN</sub>		12	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 15	ns
Clock low to $\overline{ECS}/\overline{OCS}$ negated	t <sub>CLEN</sub>		12a	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 15	ns
AS, $\overline{DS}$ negated to ADDRESS, FC, SIZE, RMC invalid	t <sub>SNAI</sub>		13	9, 10, 11	01 02 03-04	20 15 10		ns
AS (and $\overline{DS}$ READ) width asserted	t <sub>SWA</sub>		14	9, 10, 11	01 02 03 04	120 100 85 70		ns
DS width asserted WRITE	t <sub>SWAW</sub>		14a	9, 10, 11	01 02 03 04	50 40 38 30		ns
AS, $\overline{DS}$ width negated	t <sub>SN</sub>		15	9, 10, 11	01 02 03 04	50 40 38 30		ns
DS negated to $\overline{AS}$ asserted	t <sub>SNSA</sub>		15a 9/5/		01 02 03 04	45 35 30 25		ns
Clock high to $\overline{AS}$ , $\overline{DS}$ , R/W, $\overline{DBEN}$ high impedance	t <sub>CSZ</sub>		16 5/		01 02 03 04		80 60 50 40	ns
AS, $\overline{DS}$ negated to R/W invalid	t <sub>SNRN</sub>		17	9, 10, 11	01 02 03-04	20 15 10		ns

See footnotes at end of table.

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**TABLE. Electrical performance characteristics continued.**

Test	Symbol	Conditions $\frac{1}{4.50\text{ V} \leq V_{CC} \leq 5.50\text{ V}}$ $\frac{2}{-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}}$	Wave-form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
Clock high to R/W high	t <sub>CHRH</sub>	$\frac{3}{V_{CC}} = 4.5\text{ V}$	18	9, 10, 11	01	0	40	ns
					02	0	30	
			03	0	25			
			04	0	20			
Clock high to R/W low	t <sub>CHRL</sub>		20	9, 10, 11	01	0	40	ns
					02	0	30	
			03	0	25			
			04	0	20			
R/W high to AS asserted	t <sub>RAAA</sub>		21	9, 10, 11	01	20		ns
					02	15		
		03	10					
		04	5					
R/W low to DS asserted (WRITE)	t <sub>RASA</sub>	22	9, 10, 11	01	90		ns	
				02	75			
		03	60					
		04	50					
Clock high to data out valid	t <sub>CHDO</sub>	23	9, 10, 11	01		40	ns	
				02		30		
		03-04		25				
DS negated to data out invalid	t <sub>SNDI</sub>	25	9, 10, 11	01	20		ns	
				02	15			
		03	10					
		04	5					
DS negated to DBEN negated (WRITE)	t <sub>SNDN</sub>	25a	10/	01	20		ns	
				02	15			
		03	10					
		04	5					
Data-out valid to DS asserted (WRITE)	t <sub>DVSA</sub>	2611/	9, 10, 11	01	20		ns	
				02	15			
		03	10					
		04	5					
Data-in valid to clock low (data set-up)	t <sub>DICL</sub>	27	9, 10, 11	01	10		ns	
				02	5			
		03-04	5					
Late BERR/HALT asserted to clock low set-up time	t <sub>BELCL</sub>	27a	9, 10, 11	01	25		ns	
				02	20			
		03	15					
		04	10					
AS, DS negated to DSACKx, BERR, HALT, AVEC negated	t <sub>SNDN</sub>	2812/		01	0	110	ns	
				02	0	80		
		03	0	65				
		04	0	50				
DS negated to data-in invalid (data-in hold time)	t <sub>SNDI</sub>	29	9, 10, 11	A11	0		ns	
DS negated to data-in (high impedance)	t <sub>SNDI</sub>	29a	9, 10, 11	01		80	ns	
				02		60		
		03		50				
		04		40				

See footnotes at end of table.

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**TABLE. Electrical performance characteristics continued.**

Test	Symbol	Conditions $\frac{1}{4.50\text{ V} \leq V_{CC} \leq 5.50\text{ V}}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Wave- form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
DSACKx asserted to data-in valid	tDADI	$\frac{3}{4}/$ $V_{CC} = 4.5\text{ V}$	31 13/	9, 10, 11	01 02 03 04		60 50 43 32	ns
DSACKx asserted to DSACKx valid (DSACKx asserted (SKEW))	tDADV		31a 14/	9, 10, 11	01 02 03-04		20 15 10	ns
RESET input transition time	tHRRF		3212/		01 02 03-04		2.5 1.5 1.5	CLKS per.
Clock low to $\overline{\text{BG}}$ asserted	tCLBA		33	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 20	ns
Clock low to $\overline{\text{BG}}$ negated	tCLBN		34	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 20	ns
$\overline{\text{BR}}$ asserted to $\overline{\text{BG}}$ asserted (RMC not asserted)	tBRAGA		35	9, 10, 11	A11	1.5	3.5	CLKS per.
BGACK asserted to $\overline{\text{BG}}$ negated	tGAGN		37		A11	1.5	3.5	CLKS per.
$\overline{\text{BGACK}}$ asserted to $\overline{\text{BR}}$ negated	tGARN		37a 15/	9, 10, 11	A11	0	1.5	CLKS per.
$\overline{\text{BG}}$ width negated	tGN		39	9, 10, 11	01 02 03 04	120 90 75 60		ns
BG width asserted	tGA		39a	9, 10, 11	01 02 03 04	120 90 75 60		ns
Clock high to $\overline{\text{DBEN}}$ asserted (READ)	tCHDAR		40	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 20	ns
Clock low to $\overline{\text{DBEN}}$ negated (READ)	tCLDNR		41	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 20	ns
Clock low to $\overline{\text{DBEN}}$ asserted (WRITE)	tCLDAW		42	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 20	ns
Clock high to $\overline{\text{DBEN}}$ negated (WRITE)	tCHDNW		43	9, 10, 11	01 02 03 04	0 0 0 0	40 30 25 20	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $\frac{1}{4.50 V \leq V_{CC} \leq 5.50 V}$ $-55^\circ C \leq T_C \leq +125^\circ C$	Wave- form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
R/ $\bar{W}$ low to $\overline{DBEN}$ asserted (WRITE)	t <sub>RADA</sub>	$\frac{3}{V_{CC}} = \frac{4}{4.5 V}$	44	9, 10, 11	01 02 03-04	20 15 10		ns
$\overline{DBEN}$ width asserted READ	t <sub>DA</sub>		45 <u>16/</u>	9, 10, 11	01 02 03 04	80 60 50 40		ns
DBEN width asserted WRITE	t <sub>DA</sub>		45a <u>16/</u>	9, 10, 11	01 02 03 04	160 120 100 80		ns
R/ $\bar{W}$ width asserted (WRITE or READ)	t <sub>RWA</sub>		46	9, 10, 11	01 02 03 04	180 150 125 100		ns
Asynchronous input set-up time	t <sub>AI<sub>ST</sub></sub>		47a <u>12/</u>	9, 10, 11	01 02 03-04	10 5 5		ns
Asynchronous input hold time	t <sub>AI<sub>HT</sub></sub>		47b <u>12/</u>		01 02 03 04	20 15 15 10		ns
$\overline{DSACK}_x$ asserted to $\overline{BERR}$ , HALT asserted	t <sub>DABA</sub>		48 <u>17/</u>	9, 10, 11	01 02 03 04		35 30 20 18	ns
Data out hold from clock high	t <sub>DOCH</sub>		53		A11	0		ns
R/ $\bar{W}$ valid to data bus impedance change	t <sub>RADC</sub>		55 <u>5/</u>		01 02 03 04	40 30 25 20		ns
RESET pulse width (RESET instruction)	t <sub>HRPW</sub>		56	9, 10, 11	A11	512		CLKS per.
$\overline{BERR}$ negated to $\overline{HALT}$ negated (RERUN)	t <sub>BNHN</sub>		57	9, 10, 11	A11	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> 4.50 V ≤ V <sub>CC</sub> ≤ 5.50 V -55°C ≤ T <sub>C</sub> ≤ +125°C	Wave- form number	Group A subgroups	Device types	Limits		Unit
						Min	Max	
BGACK negated to bus driven	t <sub>GNBD</sub>	<sup>3/</sup> <sup>4/</sup> V <sub>CC</sub> = 4.5 V	58 <u>12/18/</u>		All	1		CLKS per.
BGACK negated to bus driven	t <sub>BNBD</sub>		59 <u>12/18/</u>		All	1		CLKS per.

- 1/ T<sub>C</sub> = -55°C and +125°C in a power-off condition under thermal soak for 4 minutes, minimum or until thermal equilibrium. Electrical parameters are tested "instant on" 100 ms after power is applied.
- 2/ All outputs unloaded except for load capacitance. Clock should be f<sub>MAX</sub>. High;  $\overline{\text{HALT}}$ ,  $\overline{\text{RESET}}$ ,  $\overline{\text{DSACK0}}$ ,  $\overline{\text{DSACK1}}$ ,  $\overline{\text{CDIS}}$ ,  $\overline{\text{IPL0-IPL2}}$ ,  $\overline{\text{BR}}$ ,  $\overline{\text{BGACK}}$ ,  $\overline{\text{AVEC}}$  and  $\overline{\text{BERR}}$  (part free running).
- 3/ For subgroups 7, 8, 9, 10, and 11; V<sub>IL</sub> = 0.5 V, V<sub>IH</sub> = 2.4 V.
- 4/ See figures 3 and 4.
- 5/ Guaranteed but not tested.
- 6/ This number can be reduced to 5 nanoseconds if strobes have equal loads.
- 7/ This specification allows system designers to qualify the  $\overline{\text{CS}}$  signal of a generic 68881/68882 with AS (allowing 7 ns for gate delay and still meet the CS to DS set-up time requirements (specification 8B)) of the generic 68881/68882.
- 8/ This specification indicates the minimum high time for  $\overline{\text{ECS}}$  and  $\overline{\text{OCS}}$  in the event of an internal cache hit followed immediately by a cache miss or operand cycle.
- 9/ This specification guarantees operation with the coprocessor, generic 68881, which specifies a minimum time for DS negated to AS asserted (specification 13A). Without this specification, incorrect interpretation of specifications 9A and 15 would indicate that the microprocessor does not meet the coprocessor, generic 68881 requirements.
- 10/ This specification allows a system designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with DBEN.
- 11/ Actual value depends on the clock input waveform.
- 12/ Cannot be tested. For system design purposes only.
- 13/ If the asynchronous set-up time (number 47) requirements are satisfied, the DSACKx low to data set-up time (number 31) and DSACKx low to BERR low set-up time (number 48) can be ignored. The data must only satisfy the data-in to clock low set-up time (number 27) for the following clock cycle, BERR must only satisfy the late BERR low to clock low set-up time (number 27A) for the following clock cycle.
- 14/ This parameter specifies the maximum allowable skew between  $\overline{\text{DSACK0}}$  to  $\overline{\text{DSACK1}}$  asserted or  $\overline{\text{DSACK1}}$  to  $\overline{\text{DSACK0}}$  asserted. Specification number 47 must be met by  $\overline{\text{DSACK0}}$  or  $\overline{\text{DSACK1}}$ .
- 15/ The minimum values must be met to guarantee proper operation. If this maximum value is exceeded, BG may be reasserted.
- 16/ DBEN may stay asserted on consecutive WRITE cycles.
- 17/ In the absence of DSACKx, BERR is an asynchronous input using the asynchronous input set-up time (number 47). This specification applies to the first (DSACK0 or DSACK1) DSACKx signal asserted.
- 18/ These specifications allow system designers to guarantee that an alternate bus master has stopped driving the bus when the microprocessor regains control of the bus after an arbitration sequence.

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Case Y

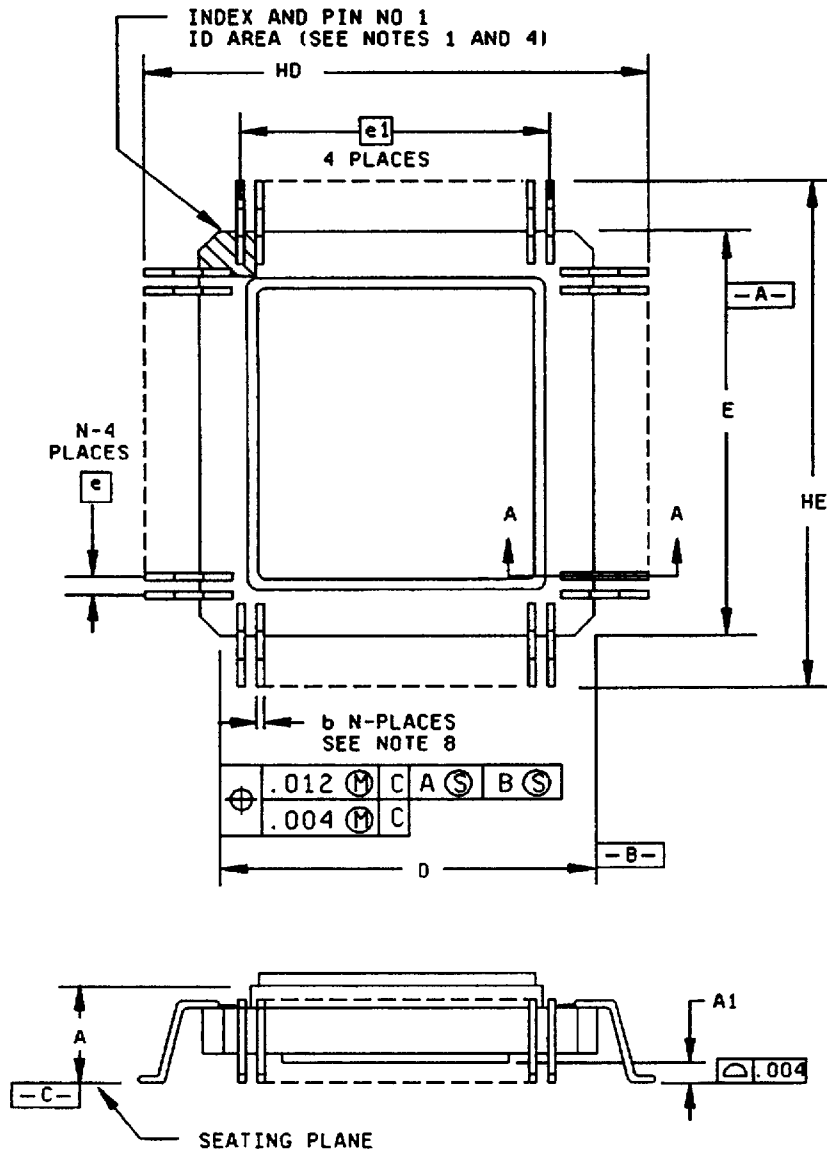
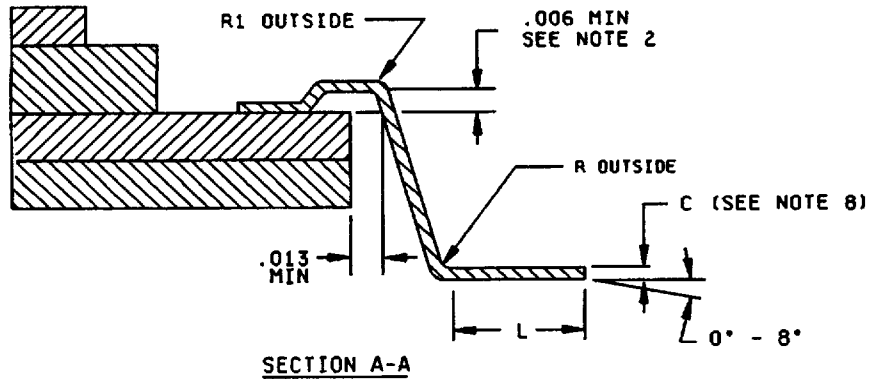


FIGURE 1. Case outlines.

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Case Y				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.125		3.175
A1	.018	.035	0.457	0.889
b	.008	.014	0.457	0.762
c	.005	.010	0.127	0.254
D/E	.940	.960	23.88	24.38
e	.025 BSC		---	
e1	.600 BSC		---	
HD/HE	1.133	1.147	28.78	29.13
L	.024	.040	0.610	1.016
N	52		52	
R	.011	.034	0.279	0.864
R1	.009	---	0.229	---

**NOTES:**

1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimensions b and c include lead finish.

FIGURE 1. Case outlines - Continued.

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Device types 01, 02, 03, and 04

Case X

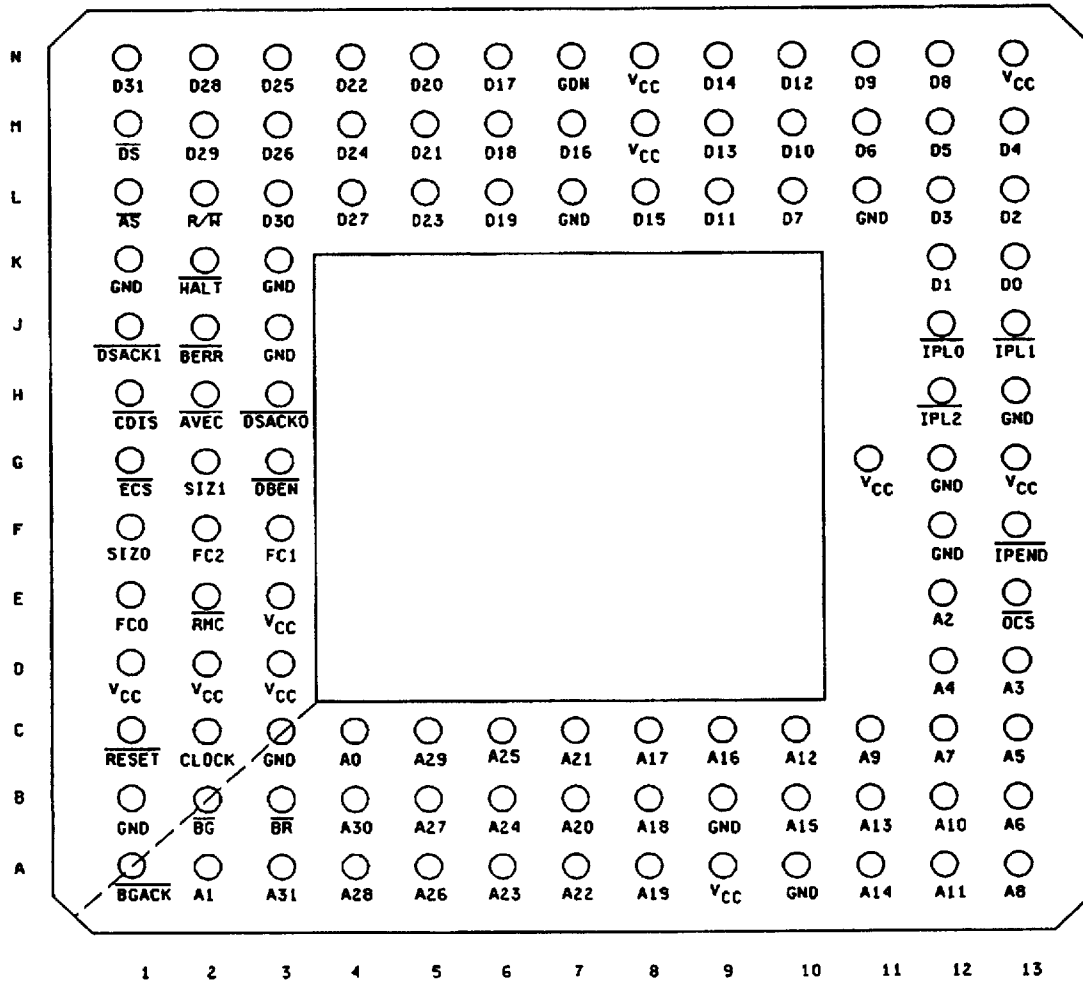


FIGURE 2. Terminal connections.

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Device types 02, 03 and 04  
Case outline Y

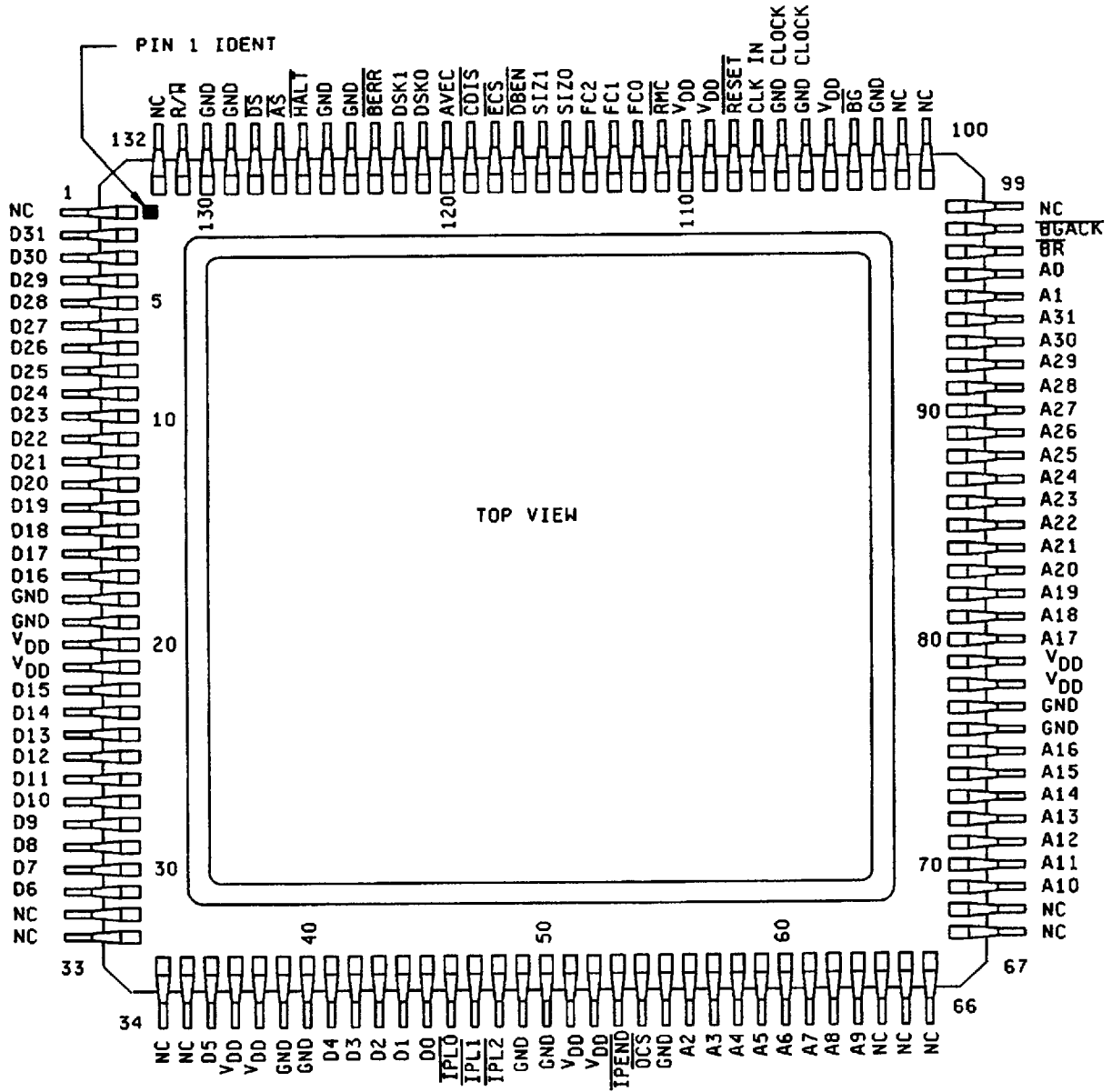


FIGURE 2. Terminal connections - Continued.

<p>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</p>	<p>SIZE A</p>	<p>5962-86032</p>
	<p>REVISION LEVEL F</p>	<p>SHEET 14</p>

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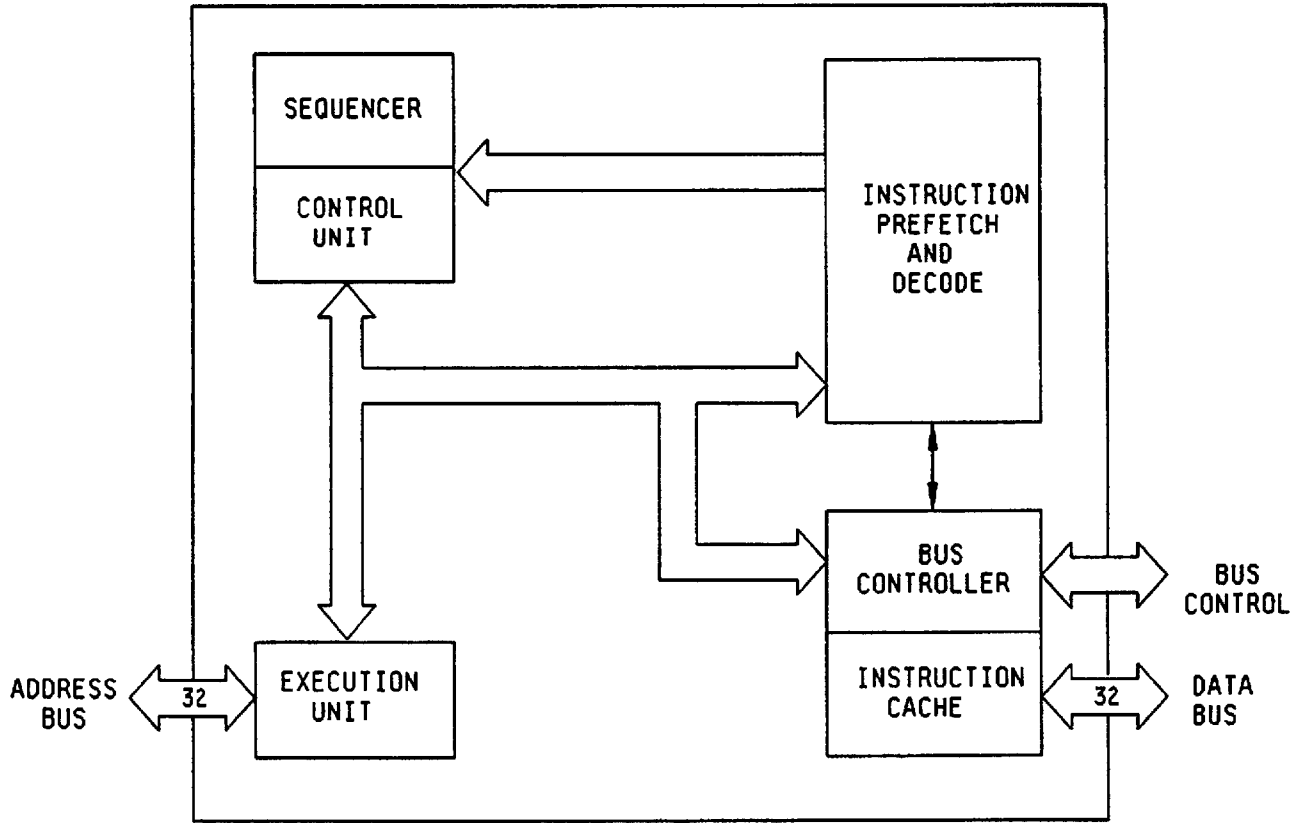
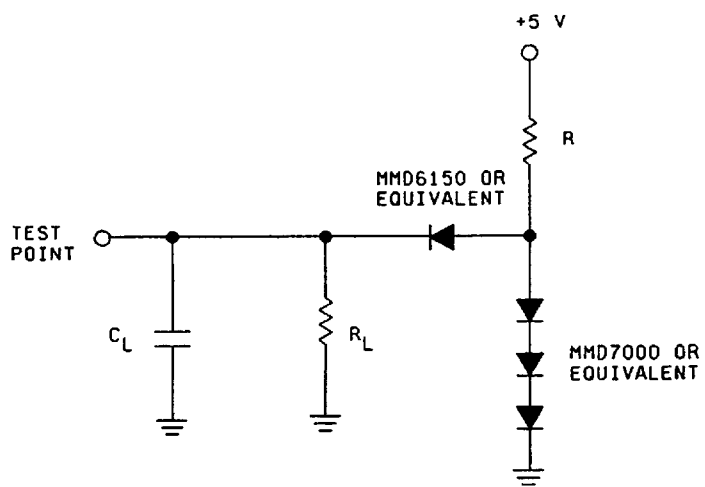
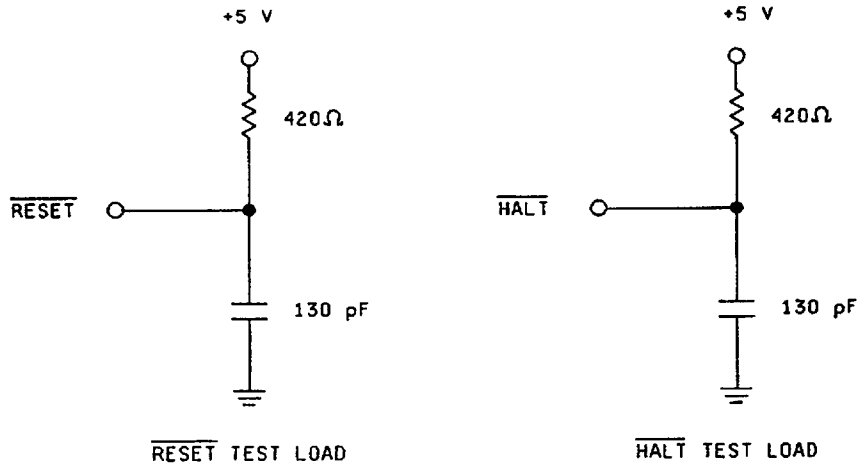


FIGURE 3. Functional block diagram.

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NOTES:

1.  $C_L = 50 \text{ pF}$  for  $\overline{\text{ECS}}$  and  $\overline{\text{OCS}}$ .
2.  $C_L = 130 \text{ pF}$  for all other (includes all parasitics).
3.  $R_L = 6.0 \text{ k}\Omega$ .
4.  $R = 1.22 \text{ k}\Omega$  for  $\overline{\text{A0-A31}}$ ,  $\overline{\text{D0-D31}}$ ,  $\overline{\text{BG}}$ ,  $\overline{\text{FC0-FC2}}$ ,  $\overline{\text{S10-S1Z1}}$ .
5.  $R = 2 \text{ k}\Omega$  for  $\overline{\text{ECS}}$  and  $\overline{\text{OCS}}$ .
6.  $R = 740\Omega$  for  $\overline{\text{AS}}$ ,  $\overline{\text{DS}}$ ,  $\overline{\text{R/W}}$ ,  $\overline{\text{RMC}}$ ,  $\overline{\text{DBEN}}$ ,  $\overline{\text{IPEND}}$ .

FIGURE 4. Switching test circuit and waveforms.

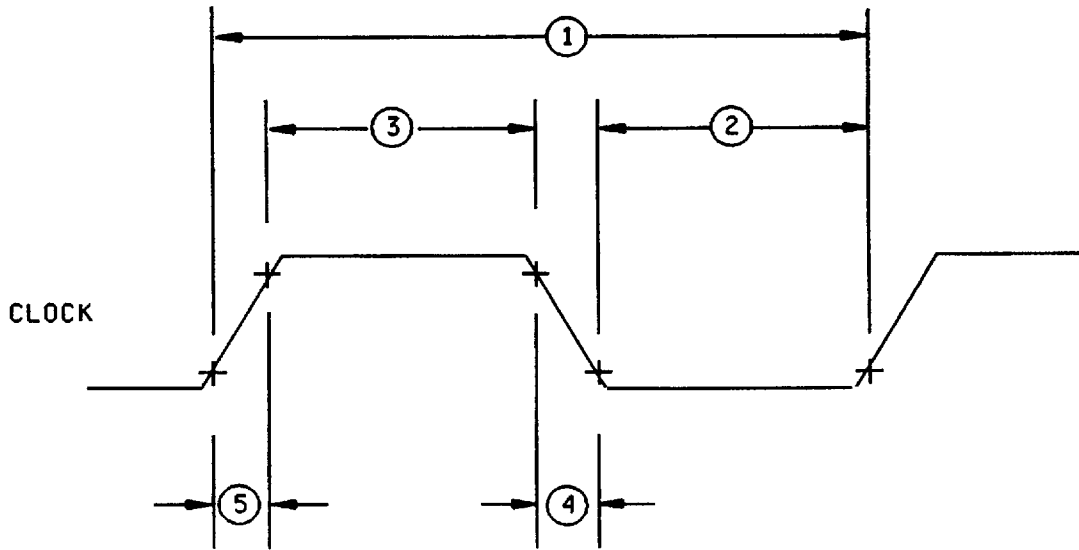
<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>	<b>5962-86032</b>
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Clock input AC timing diagram



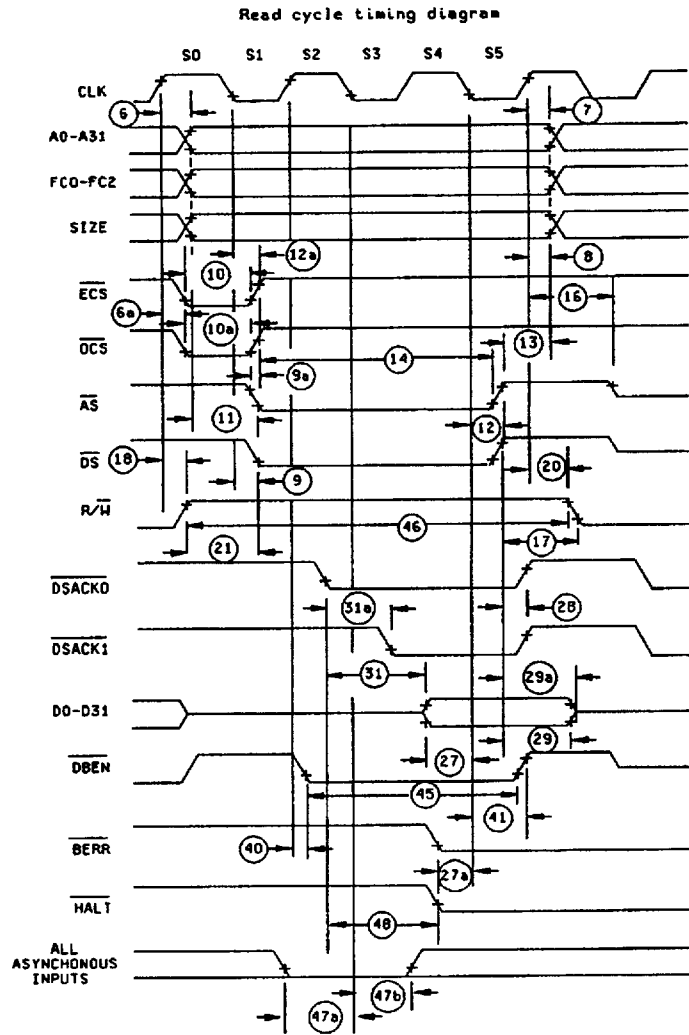
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

FIGURE 4. Switching test circuit and waveforms - Continued.

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NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

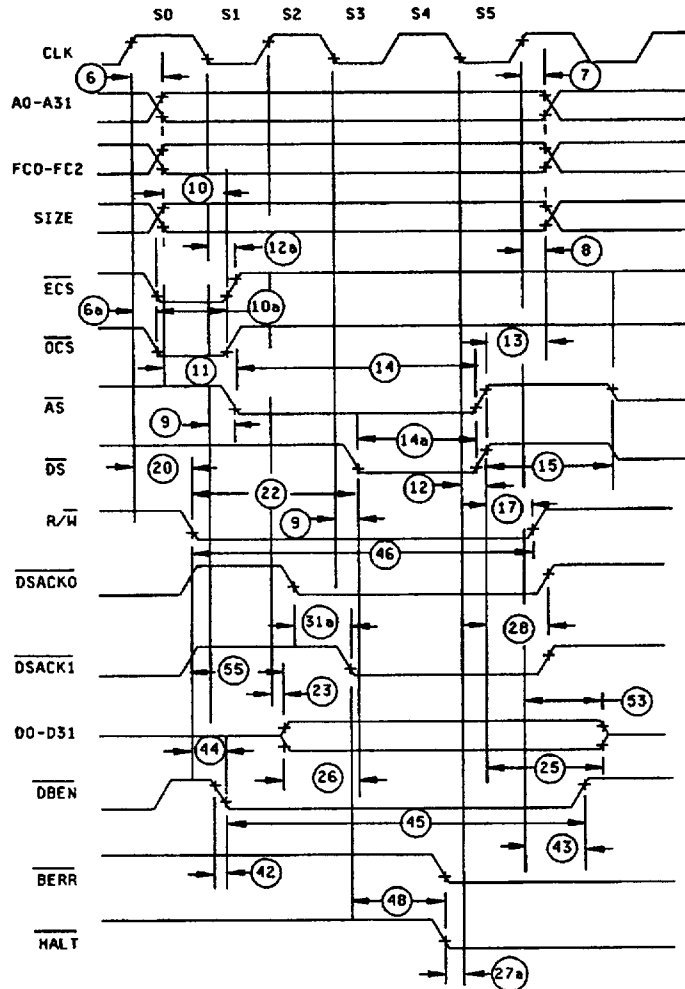
FIGURE 4. Switching test circuit and waveforms - Continued.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>	<b>5962-86032</b>
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Read cycle timing diagram



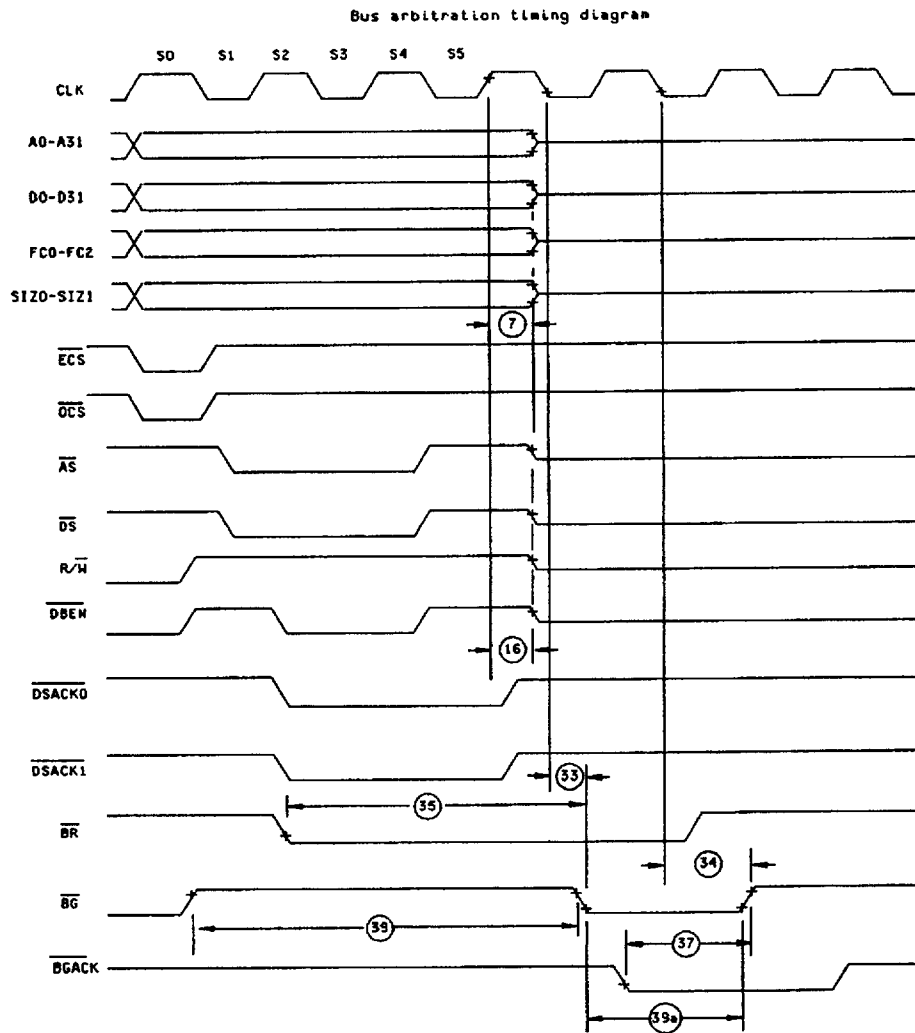
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

FIGURE 4. Switching test circuit and waveforms - Continued.

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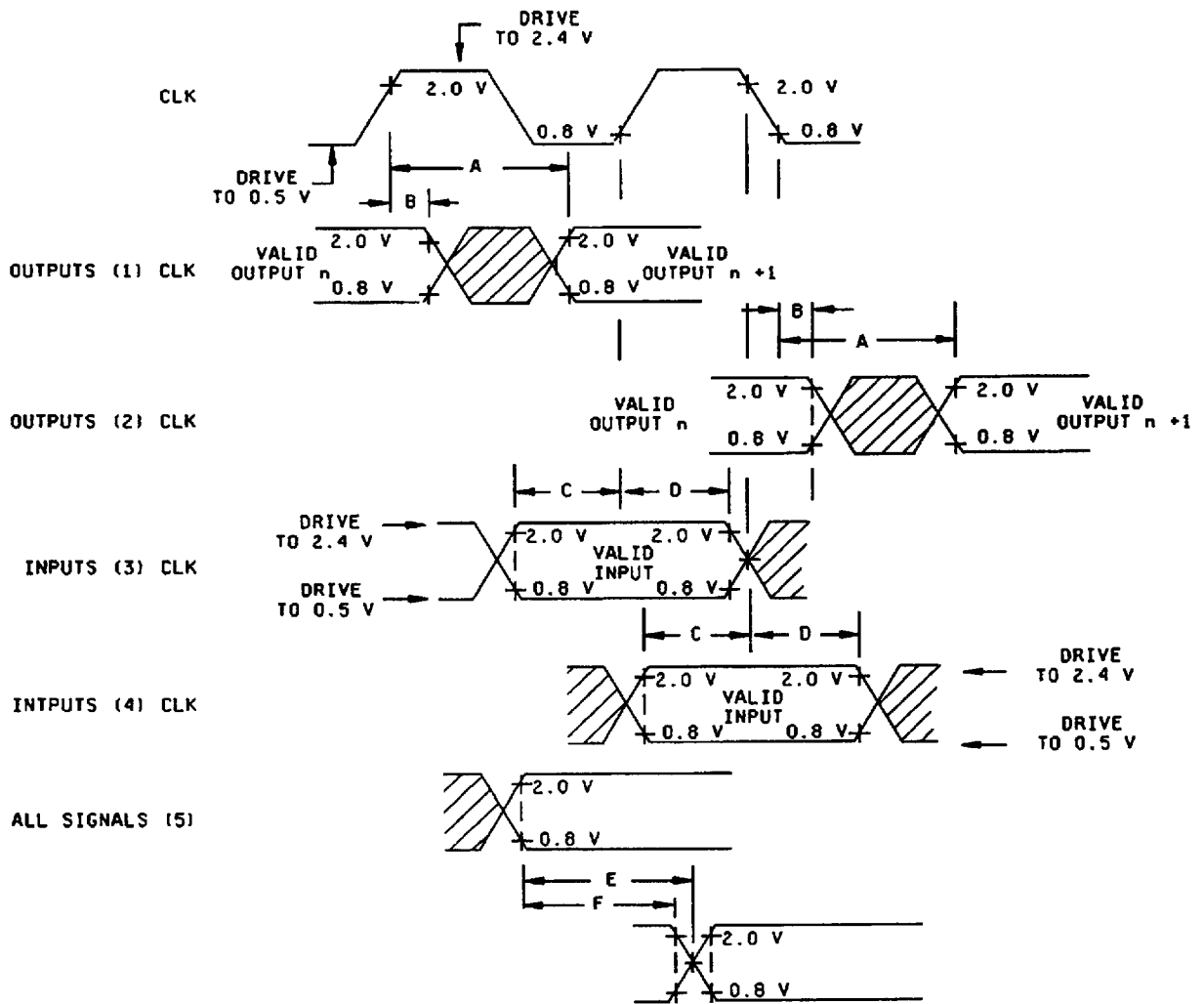
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

FIGURE 4. Switching test circuit and waveforms - Continued.

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**LEGEND:**

- A. Maximum output delay specification.
- B. Minimum output hold time.
- C. Minimum input set-up time specification.
- D. Minimum input hold time specification.
- E. Signal valid to signal valid specification (maximum or minimum).
- F. Signal valid to signal invalid specification (maximum or minimum).

**NOTES:**

1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negative of another signal.

FIGURE 4. Switching test circuit and waveforms - Continued.

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3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8a, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 4, 7, 8a, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	2, 7, 8a, 9, 10

\* PDA applies to subgroup 1

\*\* Subgroup 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

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4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.
- d. Subgroups 7 and 8 functional testing shall include verification of the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}C$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Symbols, definitions, and functional descriptions. The symbols, definitions and functional descriptions shall be as described in TABLE III.

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TABLE III. Functional descriptions

FC0 through FC2 functional code signals:

These three-state outputs identify the processor state (supervisor or user) and the address space of the bus cycle currently being executed as defined in table III.

Function code assignments.

FC2	FC1	FC0	Cycle type
0	0	0	(Undefined, reserved) <u>1/</u>
0	0	1	User data space
0	1	0	User program space
0	1	1	(Undefined, reserved) <u>1/</u>
1	0	0	(Undefined, reserved) <u>1/</u>
1	0	1	Supervisor data space
1	1	0	Supervisor program space
1	1	1	CPU space

1/ Address space 3 is reserved for user definition, while 0 and 4 are reserved for future use by vendor.

By decoding the function codes, a memory system can utilize the full 4 gigabyte address range for several address spaces.

A0 through A31 address bus:

These three-state outputs provide the address for a bus transfer during all currently defined cycles except CPU-space references. During CPU-space references the address bus provides CPU related information. The address bus is capable of addressing 4 gigabytes ( $2^{32}$ ) of data.

D0 through D31 data bus:

These three-state, bidirectional signals provide the general purpose data path between the device and all other devices. The data bus can transmit and accept data using the dynamic bus sizing capabilities of the device.

SIZ0, SIZ1 transfer size:

These three-state outputs are used in conjunction with the dynamic bus sizing capabilities of the device. The SIZ0 and SIZ1 outputs indicate the number of bytes of an operand remaining to be transferred during a given bus cycle.

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ECS external cycle start:

This output is asserted during the first one-half clock of every bus cycle to provide the earliest indication that the device may be starting a bus cycle. The use of this signal must be validated later with address strobe, since the device may start an instruction fetch cycle and then abort it if the instruction word is found in the cache. The device drives only the address, size, and function code outputs (not address strobe) when it aborts a bus cycle due to cache hit.

DCS operand cycle start:

This output signal has the same timing as ECS, except that it is asserted only during the first bus cycle of an operand transfer or instruction prefetch.

RMC read-modify-write cycle:

This three-state output signal provides an indication that the current bus operation is an indivisible read-modify-write cycle. This signal is asserted for the duration of the read-modify-write sequence. RMC should be used as a bus lock to insure integrity of instructions which use the read-modify-write operation.

AS address strobe:

This three-state output signal indicates that valid function code, address, size, and R/W state information is on the bus.

DS data strobe:

In a read cycle, this three-state output indicates that the slave device should drive the data bus. In a write cycle, it indicates that the device has placed valid data on the data bus.

R/W read/write:

This three-state output signal defines the direction of a data transfer. A high level indicates a read from an external device, a low level indicates a write to an external device.

DBEN data buffer enable:

This three-state output provides an enable to external data buffers. This signal allows the R/W signal to change without possible external buffer contention.

This pin is not necessary in all systems.

DSACK0, DSACK1 data transfer and size acknowledge:

These outputs indicate that a data transfer is complete and the port size of the external device (8, 16, or 32 bits). During a read cycle, when the processor recognizes DSACKx, it latches the data and then terminates the bus cycle; during a write cycle, when the processor recognizes DSACKx, the bus cycle is terminated.

CDIS cache disable:

This input signal dynamically disables the on-chip cache. The cache is disabled internally after the cache disable input is asserted and synchronized internally. The cache will be reenabled internally after the input negation has been synchronized internally.

IPL0, IPL1, IPL2 interrupt priority level:

These inputs indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority and cannot be masked; level zero indicates that no interrupts are requested. The least significant bit is IPL0 and the most significant bit is IPL2.

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IPEND interrupt pending:

This output indicates that the encoded interrupt priority level active on the  $\overline{IPL0}$ - $\overline{IPL2}$  inputs is higher than the current level of the interrupt mask in the status register or that a nonmaskable interrupt has been recognized.

AVEC autovector:

The  $\overline{AVEC}$  input is used to request internal generation of the vector number during an interrupt acknowledge cycle.

BR bus request:

This input is wire-ORed with all request signals from all potential bus masters and indicates that some device other than the device requires bus mastership.

BG bus grant:

This output signal indicates to potential bus masters that the device will release ownership of the bus when the current bus cycle is completed.

BGACK bus grant acknowledge:

This input indicates that some other device has become the bus master. This signal should not be asserted until the following conditions are met:

- (1)  $\overline{BG}$  (bus grant) has been received through the bus arbitration process,
- (2)  $\overline{AS}$  is negated, indicating that the device is not using the bus,
- (3)  $\overline{DSACK0}$  and  $\overline{DSACK1}$  are negated indicating that the previous external device is not using the bus, and
- (4)  $\overline{BGACK}$  is negated, which indicates that no other device is still claiming bus mastership.

$\overline{BGACK}$  must remain asserted as long as any other device is bus master.

RESET reset:

This bidirectional open-drain signal is used as the systems reset signal. If  $\overline{RESET}$  is asserted as an input, the processor will enter reset exception processing. As an output, the processor asserts  $\overline{RESET}$  to reset external devices, but is not affected internally.

HALT halt:

The assertion of this bidirectional, open-drain signal stops all processor bus activity at the completion of the current bus cycle. When the processor has been halted using this input, all control signals will be placed in their inactive state, the R/W, function code, and size signals, and the address bus remain driven with the previous bus cycle information. The  $\overline{RMC}$  signal will be driven inactive, if asserted. The data bus is three-stated.

When the processor has stopped executing instructions, due to a double bus fault condition, the  $\overline{HALT}$  line is driven by the processor to indicate to external devices that the processor has stopped.

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BERR bus error:

This input signal informs the processor that there has been a problem with the bus cycle currently being executed. These problems may be the result of:

- (1) Nonresponding devices,
- (2) Interrupt vector number acquisition failure,
- (3) Illegal accesses as determined by a memory management unit, or
- (4) Various other application dependent errors.

This bus error signal interacts with the halt signal to determine if the current bus cycle should be rerun or aborted with a bus error.

CLK clock:

The device clock input is a TTL-compatible signal that is internally buffered to develop internal clocks needed by the processor. The clock should not be gated off at any time and must conform to minimum and maximum period and pulse width times.

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## Signal summary

Signal function	Signal name	Input/output	Active state	Three state
Function codes	FC0-FC2	Output	High	Yes
Address bus	A0-A31	Output	High	Yes
Data bus	D0-D31	Input/output	High	Yes
Size	SIZE0-SIZE1	Output	High	Yes
External cycle start	$\overline{\text{ECS}}$	Output	Low	No
Operand cycle start	$\overline{\text{OCS}}$	Output	Low	No
Read-modify-write cycle	$\overline{\text{RMC}}$	Output	Low	Yes
Address strobe	$\overline{\text{AS}}$	Output	Low	Yes
Data strobe	$\overline{\text{DS}}$	Output	Low	Yes
Read/write	$\text{R}/\overline{\text{W}}$	Output	High/low	Yes
Data buffer enable	$\overline{\text{DBEN}}$	Output	Low	Yes
Data transfer and size acknowledge	$\overline{\text{DSACK0}}-\overline{\text{DSACK1}}$	Input	Low	
Cache disable	$\overline{\text{CDIS}}$	Input	Low	
Interrupt priority level	$\overline{\text{IPL0}}-\overline{\text{IPL2}}$	Input	Low	
Interrupt pending	$\overline{\text{IPEND}}$	Output	Low	No
Autovector	$\overline{\text{AVEC}}$	Input	Low	
Bus request	$\overline{\text{BR}}$	Input	Low	
Bus grant	$\overline{\text{BG}}$	Output	Low	No
Bus grant acknowledge	$\overline{\text{BGACK}}$	Input	Low	
Reset	$\overline{\text{RESET}}$	Input/output	Low	No <sup>1/</sup>
Halt	$\overline{\text{HALT}}$	Input/output	Low	No <sup>1/</sup>
Bus error	$\overline{\text{BERR}}$	Input	Low	
Clock	CLK	Input		
Power supply	V <sub>CC</sub>	Input		
Ground	GND	Input		

<sup>1/</sup> Open drain.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD  
MICROCIRCUIT DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
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REVISION LEVEL  
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DESC FORM 193A  
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