REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Inactivate case outline 3 for new design. Change drawing CAGE code to 67268. Editorial changes throughout.	1988 NOV 17	M. A. Frye

CURRENT CAGE CODE 67268

REV																								
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REV																								
SHEET																								
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A				A	A	A	A							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY: [signature]

DRAWING APPROVAL DATE: 11 APRIL 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, PROGRAM CONTROL UNIT, BIPOLAR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-87573

SHEET 1 OF 16

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1007

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87573	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2930	4-bit program control unit

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	F-11 (28-lead, .740" x .380" x .090"), flat package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.32 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, and 3	See MIL-M-38510, appendix C
Junction temperature (T_J)	+200°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V dc
Maximum low level input voltage (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ 1/ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = min, $V_{IN} = V_{IL}$ or V_{IH}	Y_0, Y_1, Y_2, Y_3 $\overline{G}$, $C_n + 4$ $C_i + 4$	I_{OH} = -1.6 mA	1,2,3	2.4		V
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OH} = -1.2 mA	1,2,3	2.4		V
Output low voltage	V_{OL}	V_{CC} = min, $V_{IN} = V_{IL}$ or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 16 mA	1,2,3		0.5	V
			$\overline{G}$, $C_n + 4$ $C_i + 4$	I_{OL} = 16 mA	1,2,3		0.5	V
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OL} = 12 mA	1,2,3		0.5	V
Input high level 2/ voltage	V_{IH}				1,2,3	2.0		V
Input low level 2/ voltage	V_{IL}				1,2,3		0.8	V
Input clamp voltage	V_I	V_{CC} = min, I_{IN} = -18 mA			1,2,3		-1.5	V
Input low current	I_{IL}	V_{CC} = max, V_{IN} = 0.5 V	D_{0-3}		1,2,3		-.360	mA
			I_{0-4}, $\overline{RE}$, $\overline{TEN}$, CP, $\overline{OE}$				-.702	
			$\overline{CC}$				-.657	
			C_i				-2.31	
			C_n				-3.25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +125^{\circ}C$ $4.5\ V \le V_{CC} \le 5.5\ V$ 1/ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Input high current	I_{IH}	V_{CC} = max, V_{IN} = 2.7 V	D_{0-3}		1,2,3		20	µA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				40	
			$\overline{CC}$				50	
			C_i				90	
			C_n				250	
Input high current	I_I	V_{CC} = max, V_{IN} = 5.5 V			1,2,3		1.0	mA
Output short circuit current 3/	I_{SC}	V_{CC} = max			1,2,3	-30	-85	mA
Output off current	I_{OZL}	V_{CC} = max,	Y_{0-3}	V_{OUT} = 0.5 V	1,2,3		-50	µA
	I_{OZH}	$\overline{OE}$ = 2.4 V		V_{OUT} = 2.4 V			50	
Power supply current 4/	I_{CC}	V_{CC} = max	T_C = -55°C to +125°C		1,2,3		239	mA
			T_C = +125°C				170	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time 1 hold time 1 Input: I_{4-0}	t_{s1} t_{h1}	See figure 3 NOTE: All setup and hold times are relating to clock low-to-high transition.	9,10,11	124 0		ns ns
Setup time 2 hold time 2 Input: $\overline{CC}$	t_{s2} t_{h2}		9,10,11	80 0		ns ns
Setup time 3 hold time 3 Input: $\overline{IEN}$	t_{s3} t_{h3}		9,10,11	69 0		ns ns
Setup time 4 hold time 4 Input: C_n	t_{s4} t_{h4}		9,10,11	52 0		ns ns
Setup time 5 hold time 5 Input: C_i	t_{s5} t_{h5}		9,10,11	37 5		ns ns
Setup time 6 hold time 6 Input: D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	t_{s6} t_{h6}		9,10,11	30 2		ns ns
Setup time 7 hold time 7 Input: D, all other conditions	t_{s7} t_{h7}		9,10,11	72 2		ns ns
Setup time 8 hold time 8 Input: $\overline{RE}$	t_{s8} t_{h8}		9,10,11	29 4		ns ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Combinational delays 1-6 Input: I_{4-0} Outputs: Y		See figure 3 NOTE: All outputs fully loaded for combinational delays C_L = 50 pF				
$\overline{G}$, $\overline{P}$	t_{pd1}		9,10,11		88	ns
$C_n + 4$	t_{pd2}				74	ns
$C_i + 4$, I_4 = L	t_{pd3}				82	ns
$C_i + 4$, I_4 = H	t_{pd4}				87	ns
$\overline{FULL}$	t_{pd5}				97	ns
	t_{pd6}				78	ns
Combinational delays 7-11 Input: $\overline{CC}$ Outputs: Y						
$\overline{G}$, $\overline{P}$	t_{pd7}		9,10,11		68	ns
$C_n + 4$	t_{pd8}				52	ns
$C_i + 4$, I_4 = H	t_{pd9}				60	ns
$\overline{FULL}$	t_{pd10}				78	ns
	t_{pd11}				47	ns
Combinational delays 12-14 Input: C_n Outputs: Y						
$C_n + 4$	t_{pd12}		9,10,11		37	ns
$C_i + 4$, I_4 = H	t_{pd13}				30	ns
	t_{pd14}				46	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Combinational delays 15-16		See figure 3				
Input: C_i		NOTE: All outputs fully loaded for combinational delays C_L = 50 pF				
Outputs:						
$C_i + 4$, I_4 = L	t_{pd15}		9,10,11		23	ns
$C_i + 4$, I_4 = H	t_{pd16}				23	ns
Combinational delays 17-23						
Input: CP						
Outputs:						
Y	t_{pd17}		9,10,11		74	ns
$\overline{G}$, $\overline{P}$	t_{pd18}				58	ns
$C_n + 4$	t_{pd19}				66	ns
$C_i + 4$, I_4 = L	t_{pd20}				48	ns
$C_i + 4$, I_4 = H	t_{pd21}				84	ns
$\overline{FULL}$	t_{pd22}				60	ns
$\overline{EMPTY}$	t_{pd23}				60	ns
Combinational delays 24-27						
Input: D						
Outputs:						
Y	t_{pd24}				55	ns
$\overline{G}$, $\overline{P}$	t_{pd25}				38	ns
$C_n + 4$	t_{pd26}				45	ns
$C_i + 4$, I_4 = H	t_{pd27}				65	ns
Combinational delay 28						
Input: $\overline{IEN}$						
Output: $\overline{FULL}$	t_{pd28}				45	ns

See footnotes at end of table.

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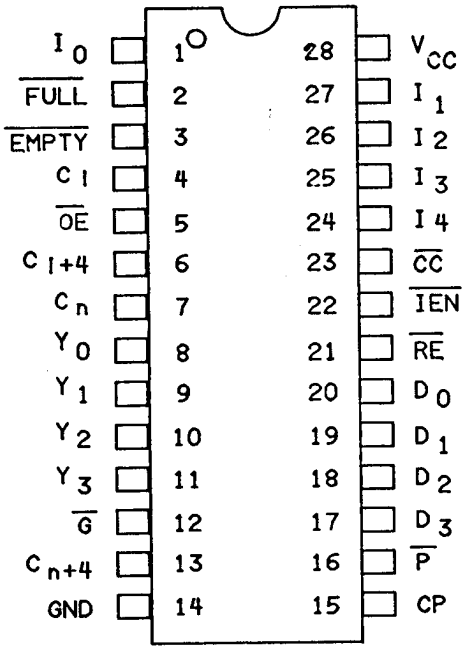
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Enable time 1	t_{EN1}	See figure 3	9,10,11		32	ns
Disable time 1 From: $\overline{OE}$ To: Y	t_{DIS1}				31	ns
Enable time 2	t_{EN2}		9,10,11		60	ns
Disable time 2 From: $\overline{CC}$ ("Suspend" instruction) To: Y	t_{DIS2}				42	ns
Enable time 3	t_{EN3}		9,10,11		85	ns
Disable time 3 From: I_{4-0} ("Suspend" instruction) To: Y	t_{DIS3}				60	ns
Minimum clock low time	t_{PWL}		9,10,11	35		ns
Minimum clock high time	t_{PWH}		9,10,11	35		ns

1/ For conditions shown as min or max, use the appropriate value specified under operating ranges for the applicable device type. For ac testing, measurements are made at 1.5 V with V_{IL} = 0 V and V_{IH} = 3.0 V. For three-state disable tests, C_L = 5.0 pF and measurement is to 0.5 V change on output voltage level.
2/ These input levels provide no guaranteed noise immunity and should only be tested in a static, noise-free environment. (Not during functional testing.)
3/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed 1 second.
4/ Minimum I_{CC} is at maximum temperature.

Case outlines X and Y

Top view



NOTES:
1. Flat package pin configuration identical to ceramic dual-in-line package.
2. Pin 1 is marked for orientation.

FIGURE 1. Terminal connections.

Case outline 3

Top view

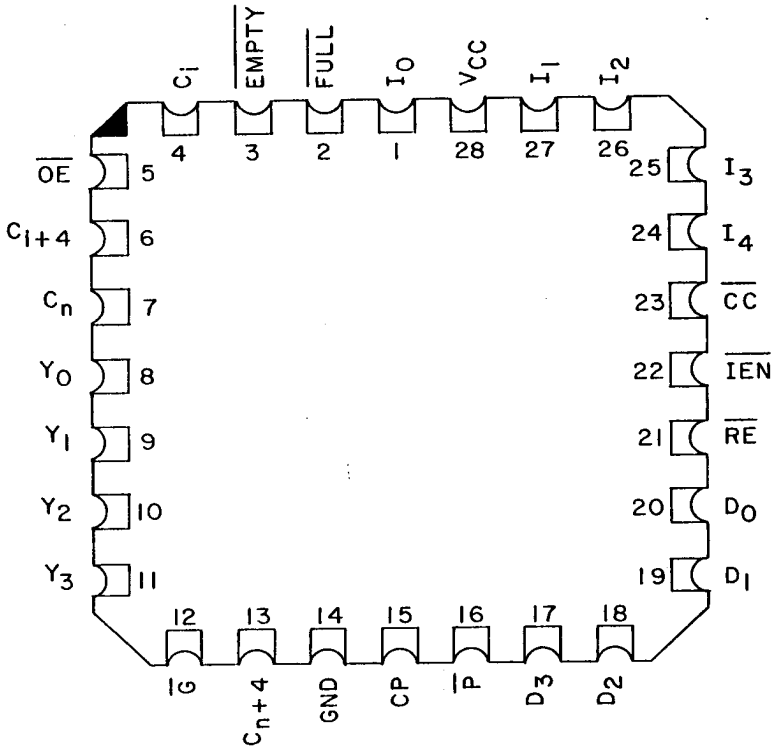


FIGURE 1. Terminal connections - Continued.

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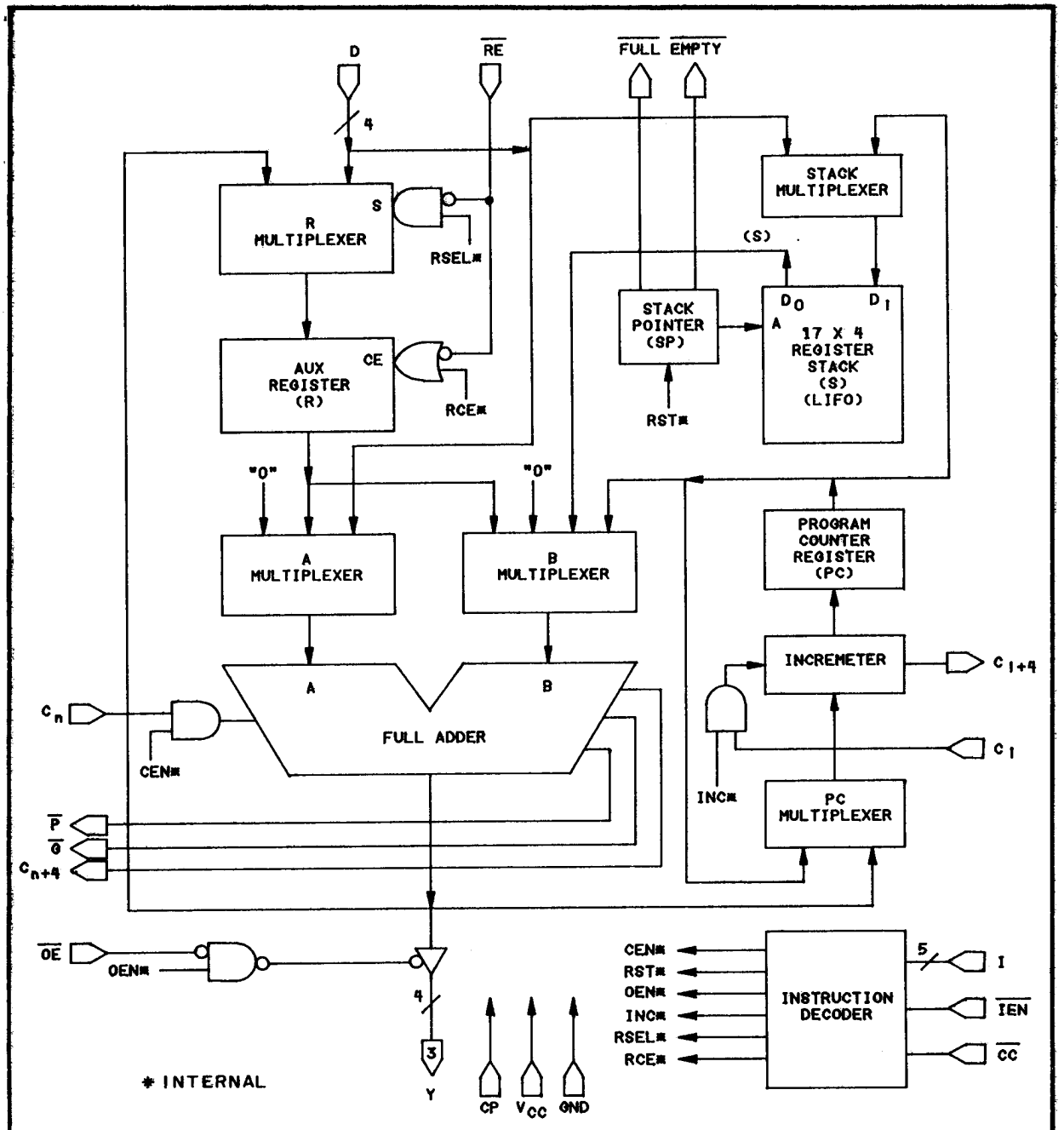

FIGURE 2. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87573
		REVISION LEVEL	SHEET 12

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SEP 87

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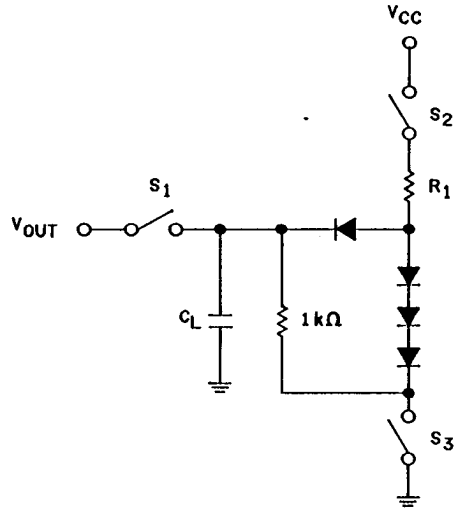
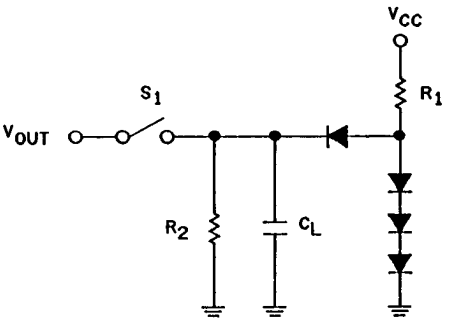
A. THREE-STATE OUTPUTS



B. NORMAL OUTPUTS



$$R = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1\ k\Omega} \qquad R_2 = \frac{2.4\ V}{I_{OH}} \qquad R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

NOTES:
1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, and S_3 are closed during function tests and all ac tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{EN} high test.
   S_1 and S_2 are closed while S_3 is open for t_{EN} low test.
4. C_L =5.0 pF for output disable tests.

Test output loads

Pin number	Pin label	Test circuit	R1	R2
2	$\overline{FULL}$	B	300	2 kΩ
3	$\overline{EMPTY}$	B	300	2 kΩ
6	C_{i+4}	B	240	1.5 kΩ
8-11	Y_{0-3}	A	240	1 kΩ

Pin number	Pin label	Test circuit	R1	R2
12	$\overline{G}$	B	240	1.5 kΩ
13	C_{n+4}	B	240	1.5 kΩ
16	$\overline{P}$	B	300	2 kΩ

FIGURE 3. Switching test circuit.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 functional testing shall include verification of instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8757301XX	34335	AM2930/BXA	---
5962-8757301YX	34335	AM2930/BYC	---
5962-87573013X	2/	AM2930/B3A	---

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Inactive for new design. Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088

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