REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete one vendor, CAGE 34335. Made changes to table I, table II, figure 1, and throughout drawing. Added figure 8. Device 02QX is inactive for new design.	1988 OCT 12	M. A. Frye

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REV STATUS OF SHEETS	REV	A	A	A	A	A	A		A	A						A	A	A	A					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick Offner

CHECKED BY: Ray Monnin

APPROVED BY: M. A. Frye

DRAWING APPROVAL DATE: 07 AUGUST 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, NMOS, 256X8 BIT RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87593

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E971

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87593	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8155/BQA	2K RAM W/ I/O ports and timer, I_{IL} ($\overline{CE}$)
02	8156/BQA	2K RAM W/ I/O ports and timer, I_{IL} (CE)

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range with respect to GND	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 5 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input low voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	All	1/ -0.5	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V	1, 2, 3	All	2.0	1/ V_{CC} +0.5	V
Output low voltage	V_{OL}	V_{IL} = 0.8 V V_{CC} = 5.5 V, V_{IH} = 2.0 V	1, 2, 3	All		0.45	V
Output high voltage	V_{OH}	V_{IL} = 0.8 V, V_{IH} = 2.0 V V_{CC} = 5.5 V, I_{OL} = -400 µA	1, 2, 3	All	2.4		V
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 5.5 V to 0 V	1, 2, 3	All		10 -10	µA µA
Output leakage current	I_{IO}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V to 0.45 V	1, 2, 3	All		10 -10	µA µA
V_{CC} supply current	I_{CC}	V_{CC} = 5.5 V 2/	1, 2, 3	All		125	nA
Chip enable leakage	I_{IL} ($\overline{CE}$)	V_{CC} = 5.5 V V_{IN} = 5.5 V to 0 V	1, 2, 3	01		160	µA
Chip enable leakage	I_{IL} (CE)	V_{CC} = 5.5 V V_{IN} = 5.5 V to 0 V	1, 2, 3	02		100	µA
Functional testing		See 4.3.1c	7, 8				

See footnotes at end of table.

mA
John B.13

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Address to LATCH setup time	t_{AL}	V_{CC} = 5.5 V, 4.5 V V_{IH} = 2.4 V V_{IL} = 0.45 V V_{OH} = 2.0 V V_{OL} = 0.8 V	9, 10, 11	All	50		ns
Address hold time after LATCH	t_{LA}		9, 10, 11	All	80		ns
LATCH to READ/WRITE control	t_{LC}		9, 10, 11	All	100		ns
Valid data out from READ control	t_{RD}		9, 10, 11	All		170	ns
Address stable to data out valid	t_{AD}		9, 10, 11	All		400	ns
LATCH enable width	t_{LL}		9, 10, 11	All	100		ns
Data bus float after READ 3/	t_{RDF}		9, 10, 11	All	0	100	ns
READ/WRITE control to LATCH enable	t_{CL}		9, 10, 11	All	20		ns
READ/WRITE control width	t_{CC}		9, 10, 11	All	250		ns
Data into WRITE setup time	t_{DW}	4/	9, 10, 11	All	150		ns
Data in hold time after WRITE	t_{WD}		9, 10, 11	All	25		ns
Recovery time between controls	t_{RV}		9, 10, 11	All	300		ns
WRITE to port output	t_{WP}		9, 10, 11	All		400	ns
Port input setup time	t_{PR}		9, 10, 11	All	70		ns
Port input hold time	t_{RP}		9, 10, 11	All	50		ns
STB to buffer full	t_{SBF}		9, 10, 11	All		400	ns
STB width	t_{SS}		9, 10, 11	All	200		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

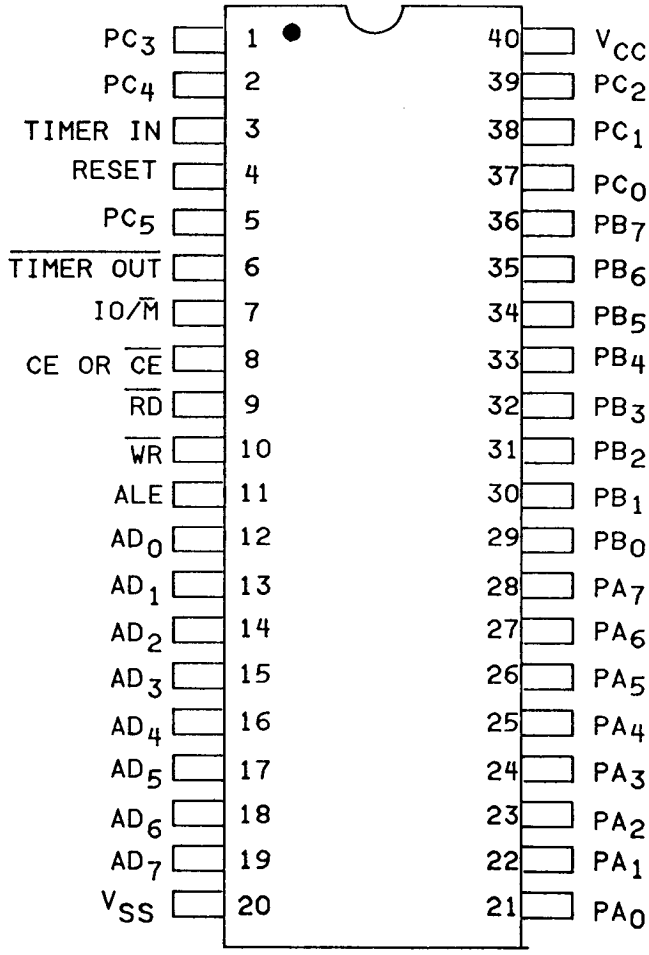
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits Min	Limits Max	Unit
READ to buffer empty	t_{RBE}	V_{CC} = 5.5 V, 4.5 V	9, 10, 11	All		400	ns
STB to INTR on	t_{SI}	V_{IH} = 2.4 V	9, 10, 11	All		400	ns
READ to INTR off	t_{RDI}	V_{IL} = 0.45 V	9, 10, 11	All		400	ns
Port setup time to STB	t_{PSS}	V_{OH} = 2.0 V	9, 10, 11	All	50		ns
Port hold time after STB	t_{PHS}	V_{OL} = 0.8 V V_{IL} = 0.45 V 4/	9, 10, 11	All	120		ns
STB to buffer empty	t_{SBE}		9, 10, 11	All		400	ns
WRITE to buffer full	t_{WBF}		9, 10, 11	All		400	ns
WRITE to INTR off	t_{WI}		9, 10, 11	All		400	ns
TIMER-IN to TIMER-OUT low	t_{TL}		9, 10, 11	All		400	ns
TIMER-IN to TIMER-OUT high	t_{TH}		9, 10, 11	All		400	ns
Data bus enable from READ control	t_{RDE}		9, 10, 11	All	10		ns
TIMER-IN low time	t_1		9, 10, 11	All	88		ns
TIMER-IN high time	t_2		9, 10, 11	All	120		ns

1/ These V_{IL} and V_{IH} values are guaranteed by design and are not tested.

2/ The supply current is measured with unloaded outputs while running functional patterns.

3/ AC float timing parameter t_{rdf} is tested logic 0 to float only.

4/ See figures 3, 4, 5, 6, 7, and 8.



NOTE: Pin 1 is marked for orientation.

FIGURE 1. Terminal connections.

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Pin description.

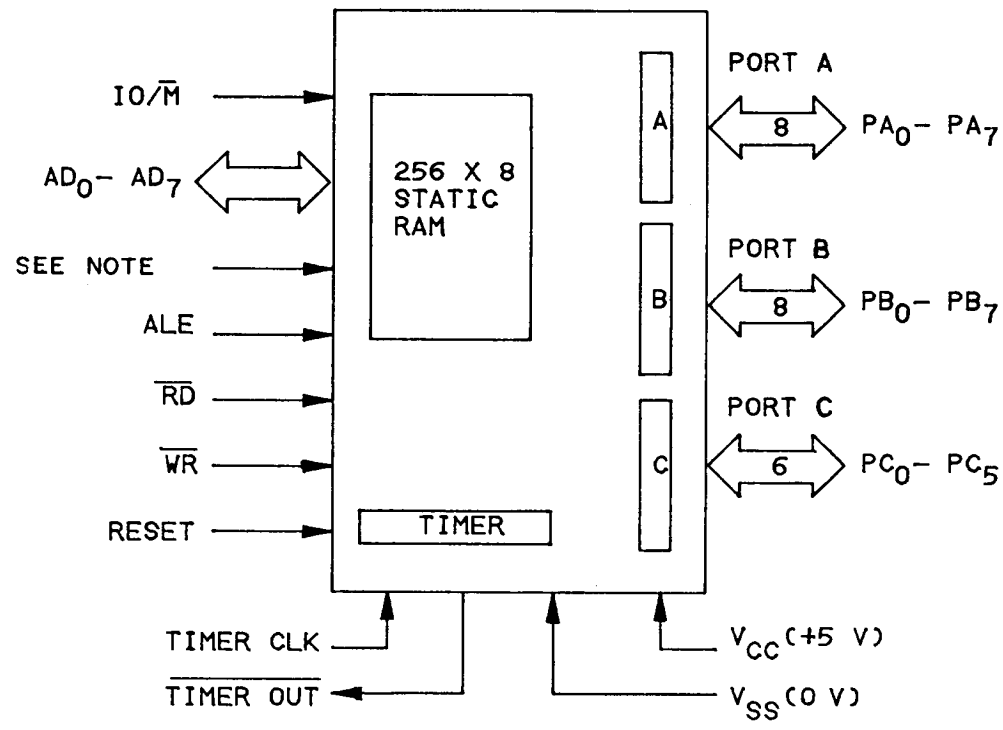
Pin no.	Name	I/O	Pin description
4	RESET	I	The RESET signal is a pulse provided by the 8085AH to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input code. The width of RESET pulse should typically be 600 ns. (Two 8085AH clock cycle times.)
12-19	AD_0-AD_7	I/O	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.
8	CE - $\overline{CE}$	I	Chip enable. On the 01 device, this pin is $\overline{CE}$ and is active low. On the 02 device, this pin is CE and is active high.
9	$\overline{RD}$	I	Input low on this line with the chip enable active enables the AD_{0-7} buffers. If IO/$\overline{M}$ pin is LOW, the RAM content will be read out to the AD bus. Otherwise, the content of the selected I/O port will be read to the AD bus.
10	$\overline{WR}$	I	Input low on this line with the chip enable active causes the data on the AD lines to be written to the RAM or I/O ports, depending on the of IO/$\overline{M}$.
11	ALE	I	Address latch enable. This control signal latches the address on the AD_{0-7} lines and the state of the chip enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
7	IO/$\overline{M}$	I	IO/$\overline{MEMORY}$ select. This line selects the memory if LOW and selects the IO if HIGH.

FIGURE 1. Terminal connections - Continued.

Pin description - Continued.

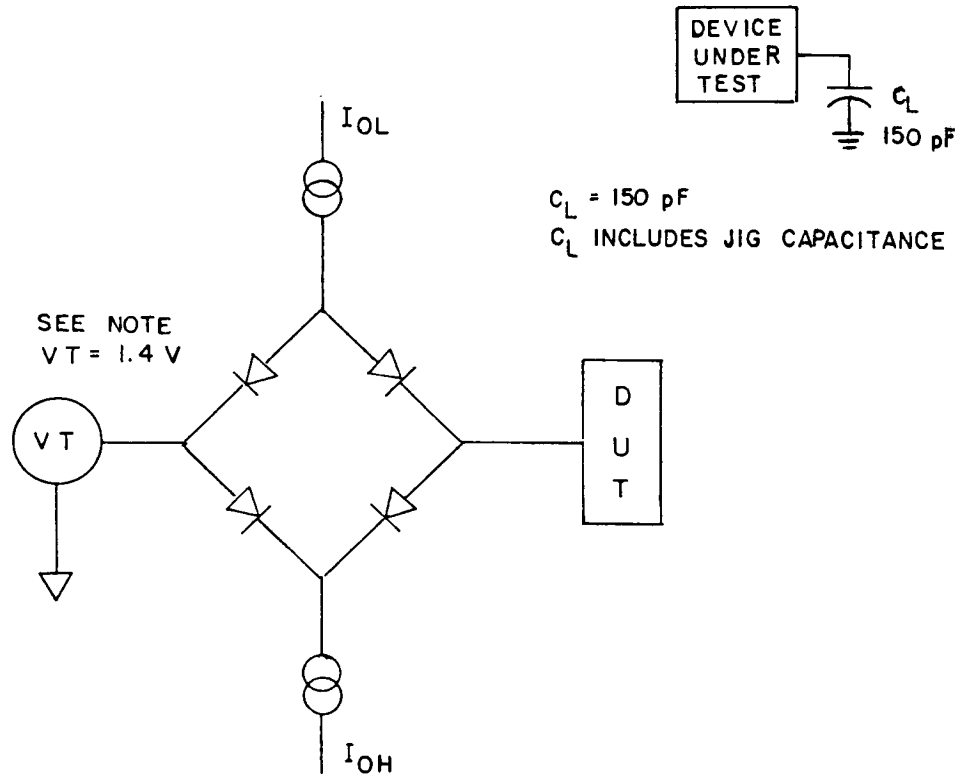
Pin no.	Name	I/O	Pin description
21-28	PA_0-PA_7	I/O	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status register.
29-36	PB_0-PB_7	I/O	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status register.
37-39 1, 2, 5	PC_0-PC_5	I/O	These 6 pins can function as either input port, output port or as control signals for PA and PB. Programming is done through the C/E register. When PC_{0-5} are used as control signals, they will produce the following: PC_0-A INTR (Port A interrupt) PC_1-A BF (Port A buffer full) PC_2-$\overline{\text{A STB}}$ (Port A strobe) PC_3-B INTR (Port B interrupt) PC_4-B BF (Port B buffer full) PC_5-$\overline{\text{B STB}}$ (Port B strobe)
3	TIMER IN	I	This is the input to the counter timer.
6	$\overline{\text{TIMER OUT}}$	O	This pin is the timer output. This output can be either a square wave a pulse depending on the timer code.
40	V_{CC}		+5 volt supply.
20	V_{SS}		Ground reference.

FIGURE 1. Terminal connections - Continued.



NOTE: Device 01 = $\overline{CE}$, device 02 = CE

FIGURE 2. Block diagram.



NOTE: This test circuit is the dynamic load of a Teredyne J941.

FIGURE 3. AC testing load circuit.

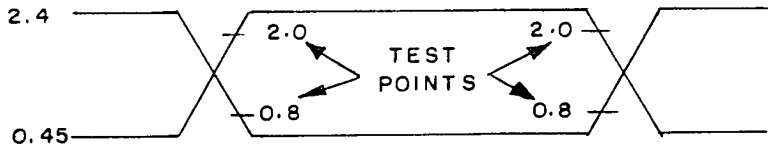
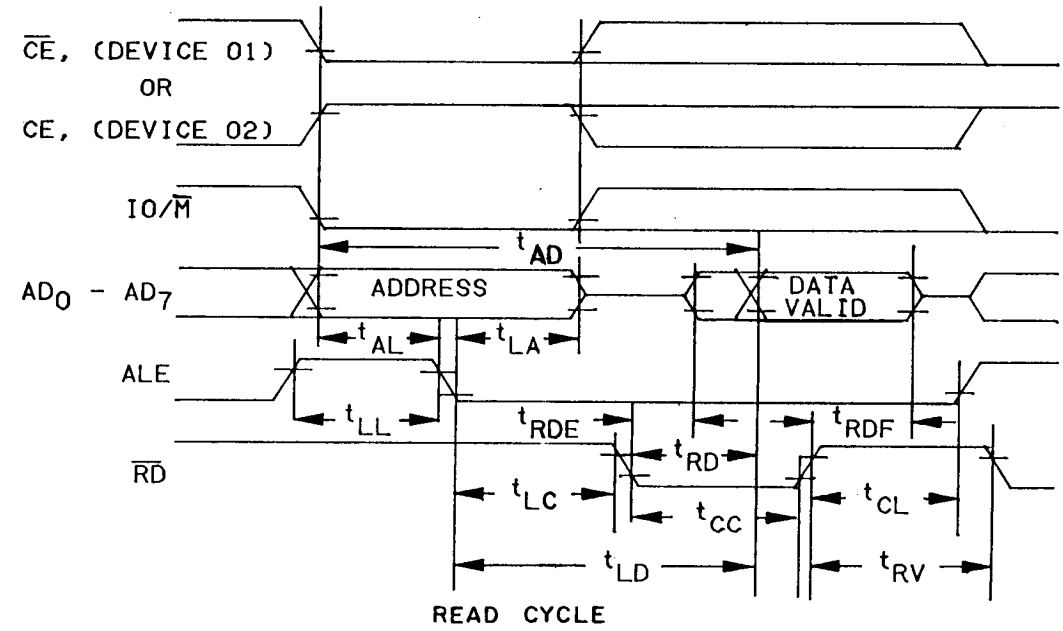
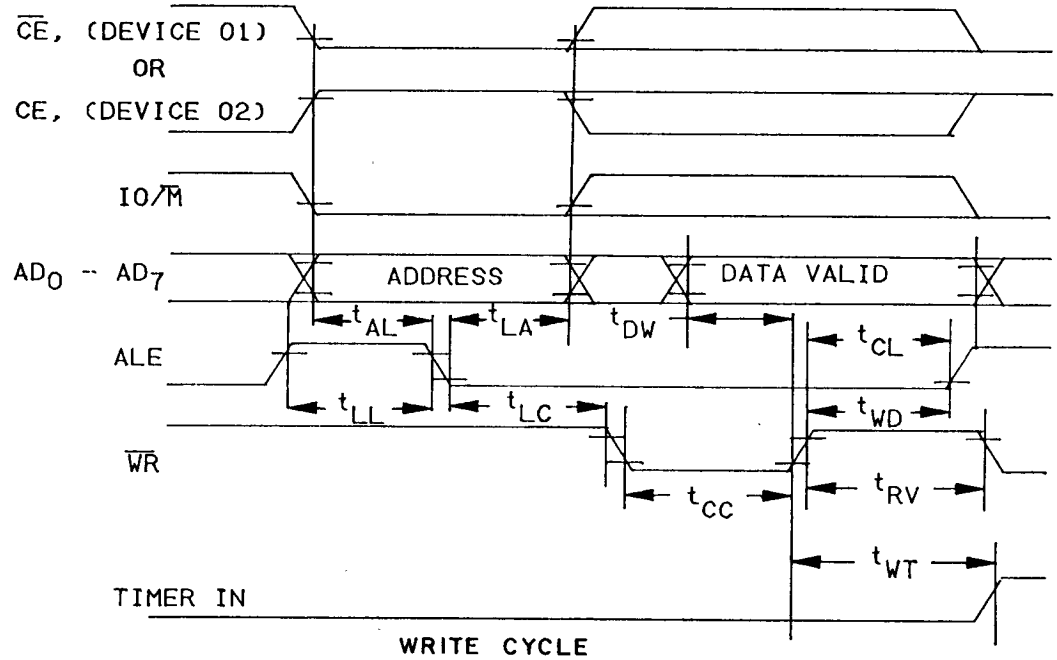


FIGURE 4. AC switching circuit and input/output waveform.



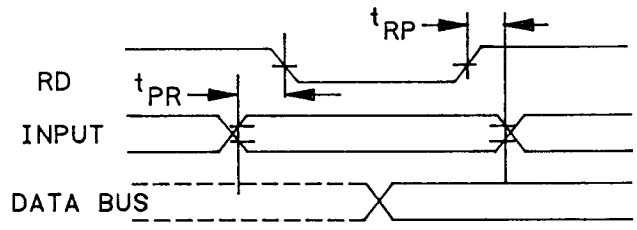
READ CYCLE



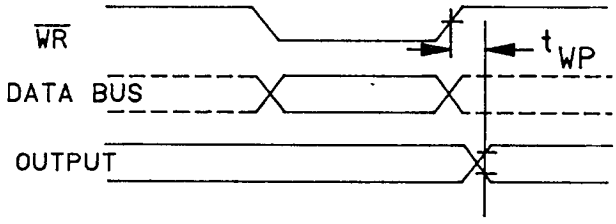
WRITE CYCLE

FIGURE 5. Timing diagrams.

BASIC INPUT MODE



BASIC OUTPUT MODE



NOTE: Data bus timing is shown on figure 5.

FIGURE 6. Basic input/output timing waveform.

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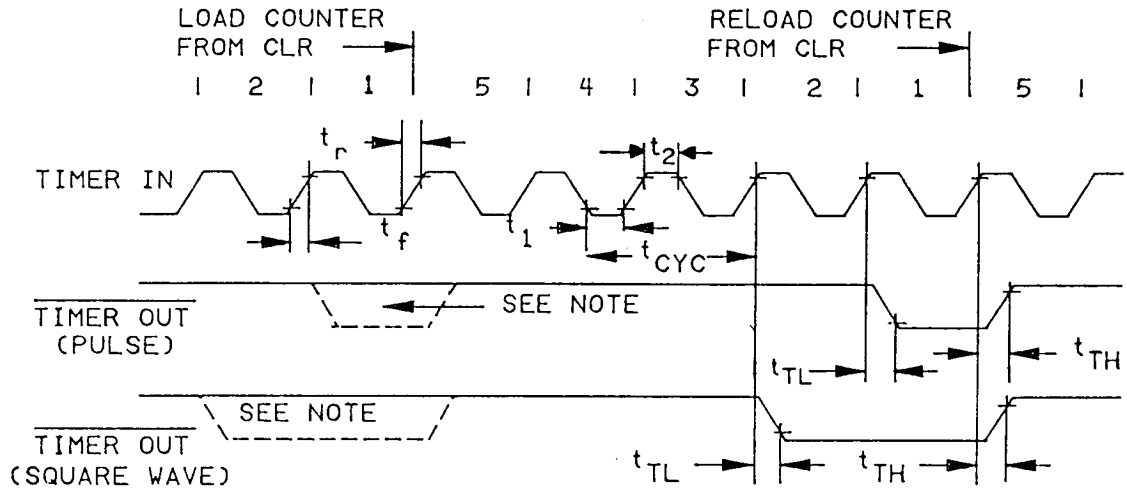

NOTE: The timer output is periodic if an automatic reload mode (M_1 mode bit = 1)

FIGURE 7. Timer output waveform countdown from five to one.

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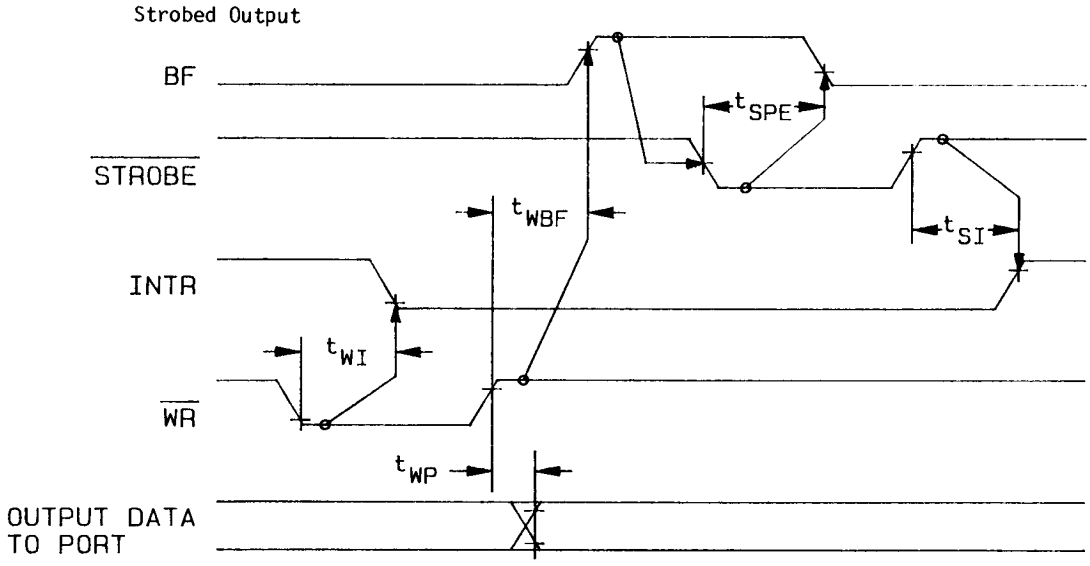

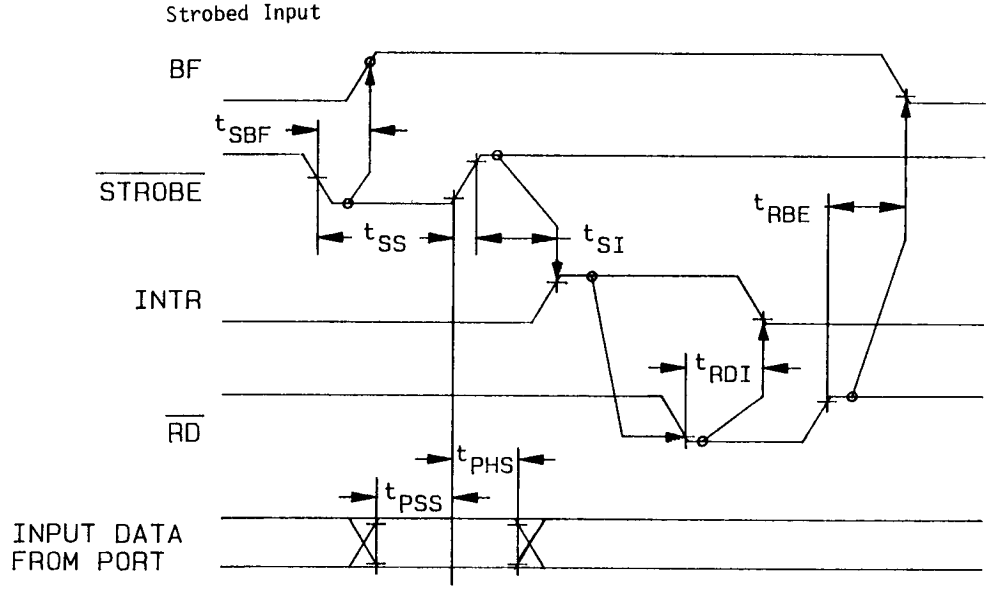

FIGURE 8. Strobed input/output timing waveforms.

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3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10**, 11**
Group A test requirements (method 5005)	1*, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	2, 8(hot), 10

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-87593012X	34649	MD8155H/B
5962-87593022X	2/	AM8156/BQA

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design, not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Chandler Boulevard Chandler, AZ 85226