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LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15								

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 11 April 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, PROGRAMMABLE SYNCHRONOUS STATE MACHINE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89546

SHEET 1 OF 15

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1278

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89546	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Clock frequency
01	See 6.4	Programmable synchronous state machine	28 MHz
02	See 6.4	Programmable synchronous state machine	40 MHz
03	See 6.4	Programmable synchronous state machine	50 MHz

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	See figure 1, (28-lead, 1.490" x .310" x .200"), dual-in-line package 1/
Y	F-11 (28-lead, .740" x .380" x .090"), flat package 1/
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package 1/

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines Y and 3	See MIL-M-38510, appendix C
Case outline X	26°C/W 2/
Maximum power dissipation (P_D) 3/	1.0 W
Maximum junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.2 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ When the thermal resistance for this case is specified in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics shall be as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA V_{IN} = V_{IH} or V_{IL}	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IN} = V_{IH} or V_{IL}	1,2,3	All		0.5	V
Input high voltage 2/	V_{IH}		1,2,3	All	2.2		V
Input low voltage 2/	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1,2,3	All	-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{OUT} = 5.5 V and GND	1,2,3	All	-40	+40	µA
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1,2,3	All	-30	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = GND	1,2,3	All		150	mA
Input capacitance 4/	C_{IN}	V_{IN} = 2.0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		7	pF
Output capacitance 4/	C_{OUT}	V_O = 2.0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		8	pF
Input or feedback setup to input register clock	t_{IS}	V_{CC} = 4.5 V See figures 4 and 5	9,10,11	01	10		ns
				02,03	5		
Input register clock to output register clock	t_{OS}		9,10,11	01	35		ns
				02	25		
				03	20		
Output register clock to output	t_{CO}		9,10,11	01		25	ns
				02		20	
				03		15	
Input register hold time	t_{IH}		9,10,11	All	5		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input register clock to output enable 5/	t_{CEA}	V_{CC} = 4.5 V See figures 4 and 5	9,10,11	01		35	ns
				02		25	
				03		20	
Input register clock to output disable 4/ 5/	t_{CER}		9,10,11	01		35	ns
				02		25	
				03		20	
Pin 14 enable to output enable 5/	t_{PZX}		9,10,11	01		35	ns
				02		25	
				03		20	
Pin 14 disable to output disable 4/ 5/	t_{PXZ}		9,10,11	01		35	ns
				02		25	
				02		20	
Input or output clock width high 4/	t_{WH}		9,10,11	01	15		ns
				02	10		
				03	8		
Input or output clock width low 4/	t_{WL}		9,10,11	01	15		ns
				02	10		
				03	8		
External clock period ($t_{CO} + t_{IS}$) input and output 4/ clock common	t_P		9,10,11	01	35		ns
				02	25		
				03	20		
Output data stable time from synchronous 4/ 6/ clock input	t_{OH}		9,10,11	All	3		ns
Output data stable time minus I/P 4/ 7/ register hold time	t_{OH}-t_{IH}		9,10,11	All	0		ns
External maximum frequency 4/ 8/ ($1/(t_{CO} + t_{IS})$)	f_{MAX1}		9,10,11	01	28.5		MHz
				02	40.0		
				03	50.0		
Data path maximum frequency 4/ 9/ ($1/(t_{WH} + t_{WL})$)	f_{MAX2}		9,10,11	01	33.3		MHz
				02	50.0		
				03	62.5		
Internal maximum frequency 4/ 10/	f_{MAX3}		9,10,11	01	30.0		MHz
				02	45.0		
				03	57.0		

See footnotes on next page.

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1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 4, circuit A, unless otherwise specified.

2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ Measured as the time after output register disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 V below V_{OH} minimum or a previous low level has risen to 0.5 V above V_{OL} maximum with the load in figure 4, circuit B. See figure 5 for enable and disable test waveforms.

6/ Measured as the time after output register clock input that the previous output data state remains stable on the output.

7/ This difference parameter guarantees that any output feedback to its own inputs externally or internally will satisfy the input register minumum input hold time. This parameter is guaranteed for a given individual device.

8/ This parameter guarantees the maximum frequency at which a state machine configuration with external feedback can operate.

9/ This parameter guarantees the maximum frequency at which an individual input or output register can be cycled.

10/ This parameter guarantees the maximum frequency at which a state machine configuration with only internal feedback can operate.

3.5 Processing EPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPLDs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPLDs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.5.3 Verification of erasure or programmed EPLDs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

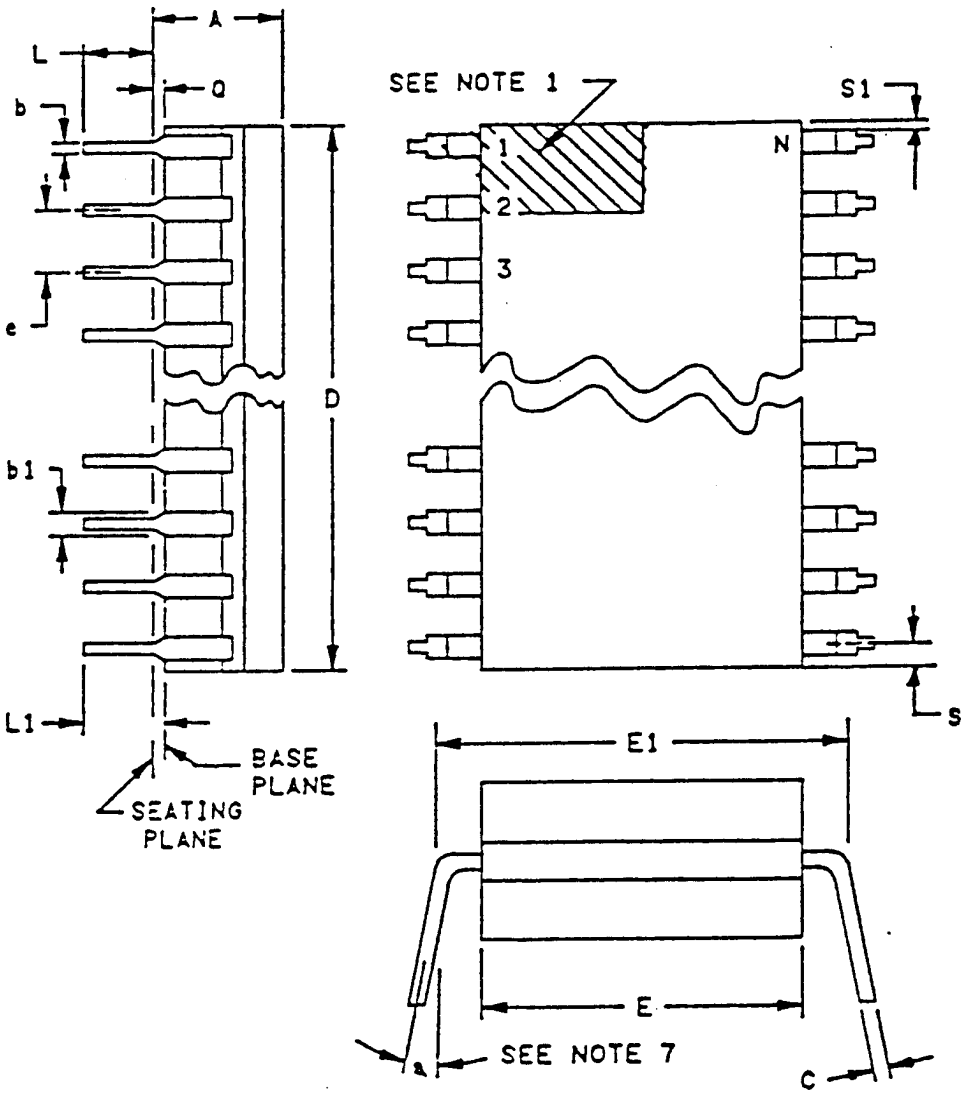

FIGURE 1. Case X (28-pin, 1.490" x 0.310" x 0.200"), dual-in-line package.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89546
		REVISION LEVEL	SHEET 7

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Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	.200	---	5.08	
b	.014	.023	0.36	0.58	8
b1	.038	.065	0.96	1.65	2, 8
c	.008	.015	0.20	0.38	8
D	---	1.490	---	37.89	4
D	---	1.490	---	37.89	4
E	.220	.310	5.59	7.87	4
E1	.290	.320	7.37	8.13	7

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L1	.150	---	3.81	---	
Q	.015	.060	0.38	1.52	3
S	---	.100	---	2.54	6
S	---	.100	---	2.54	6
S1	.005	---	0.13	---	6
a	0°	15°	0°	15°	

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b1 may be .023 (0.58 mm) for leads number 1, 14, 15, and 28 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each lead centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to leads 1 and 28.
6. Applies to all four corners (leads number 1, 14, 15, and 28) shall apply.
7. Lead center when a is 0°. E1 shall be measured at the centerline of the leads.
8. All leads - increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
9. Twenty-six spaces.

FIGURE 1. Case X (28-pin, 1.490" x 0.310" x 0.200"), dual-in-line package - Continued.

Device types	All
Case outlines	X, Y, 3
Terminal number	Terminal symbol
1	CLK
2	CK1
3	I_0/CK2
4	I_1
5	I_2
6	I_3
7	I_4
8	V_{SS}
9	I_5
10	I_6
11	I_7
12	I_8
13	I_9
14	$\overline{OE}/I_{10}$
15	I/O_{11}
16	I/O_{10}
17	I/O_9
18	I/O_8
19	I/O_7
20	I/O_6
21	GND
22	V_{CC}
23	I/O_5
24	I/O_4
25	I/O_3
26	I/O_2
27	I/O_1
28	I/O_0

FIGURE 2. Terminal connections.

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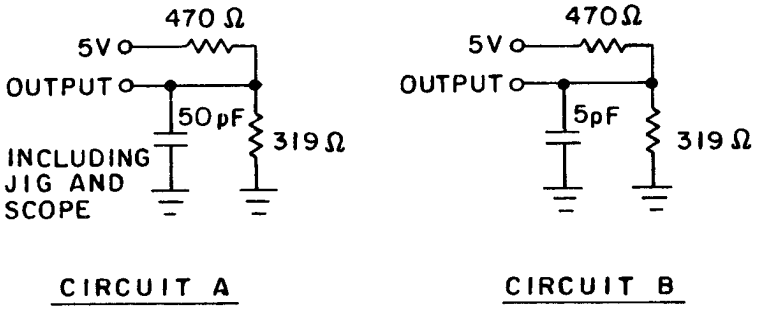
Truth table																								
Input pins													Output pins											
CLK	CK1	I/CK2	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	OE/I	I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = High impedance.
2. X = Don't care.

FIGURE 3. Truth table (unprogrammed).



NOTES: Circuit A for all parameters except t_{CEA}, t_{CER}, t_{PZX} and t_{PXZ}.
Circuit B for t_{CEA}, t_{CER}, t_{PZX} and t_{PXZ}.

FIGURE 4. Output load circuit.

Output control switching waveform

Parameter	V_X	Output waveform - measurement level
$t_{PXZ}(-)$ $t_{CER}(-)$	1.5 V	0.5V, V_{OH}, V_X
$t_{PXZ}(+)$ $t_{CER}(+)$	2.6 V	0.5 V, V_{OL}, V_X
$t_{PZX}(+)$ $t_{CEA}(+)$	2.0 V	0.5 V, V_X, V_{OH}
$t_{PZX}(-)$ $t_{CEA}(-)$	2.0 V	0.5 V, V_X, V_{OL}

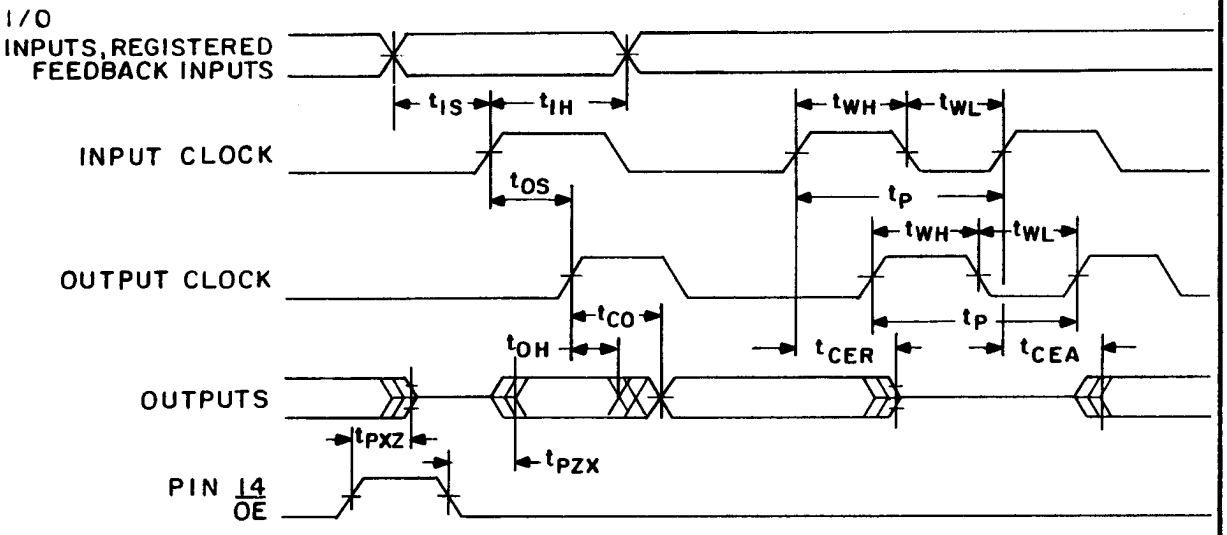


FIGURE 5. Switching waveforms.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method . 4/

(1) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell.

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.

(3) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(6) Perform electrical tests (see 4.2b).

(7) Erase (see 3.5.1). Devices may be submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.5.3).

4/ Steps 1 through 3 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7 and 8 shall consist of verifying the data pattern.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The intergrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of twentyfive Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum intergrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

4.6 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 and MIL-M-38510 for initial testing and after any design or process changes which may affect input or output protection circuitry.The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1000 volts or greater shall be considered as conforming to the requirements of this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8954601XX	65786	CY7C330-28WMB	
5962-8954601YX	65786	CY7C330-28TMB	
5962-89546013X	65786	CY7C330-28QMB	
5962-8954602XX	65786	CY7C330-40WMB	
5962-8954602YX	65786	CY7C330-40TMB	
5962-89546023X	65786	CY7C330-40QMB	
5962-8954603XX	65786	CY7C330-50WMB	
5962-8954603YX	65786	CY7C330-50TMB	
5962-89546033X	65786	CY7C330-50QMB	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134

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