REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Kenneth Rose

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DRAWING APPROVAL DATE: 26 MARCH 1990

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 16K X 4 SRAM WITH OE AND DUAL CE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89891

SHEET 1

DESC FORM 193
SEP 87

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89891	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.6	16K x 4 Static RAM with $\overline{OE}$ and dual $\overline{CE}$	25 ns (data retention)
02	See 6.6		25 ns
03	See 6.6		20 ns (data retention)
04	See 6.6		20 ns
05	See 6.6		15 ns (data retention)
06	See 6.6		15 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
X	C-11 (28-terminal, .560" x .358" x .120") leadless chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc 1/
DC output current	20 mA
Ambient storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases L and X	See MIL-M-38510, appendix C
Power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc 1/
Ground voltage (V_{SS}), (GND)	0 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to 0.8 V dc 2/
Operating case temperature range (T_C)	-55°C to +125°C

1/ All voltages referenced to V_{SS}.
2/ V_{IL} negative undershoots to a minimum of -2.0 V dc are allowed with a maximum 20 ns pulse width.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (reference MIL-M-38510, 3.1.3.8) shall be subjected to and pass the internal moisture content test, (test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial characterization and after any process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroup 7 and 8 tests sufficient to verify the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{CC} = max, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = max, V_{OUT} = GND to V_{CC} $\overline{CE} \ge V_{IH}$ $\overline{WE} \le V_{IL}$	1,2,3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA V_{IL} = 0.8 V; V_{IH} = 2.2 V	1,2,3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA V_{IL} = 0.8 V; V_{IH} = 2.2 V	1,2,3	All	2.4		V
Operating supply current	I_{CC1}	$\overline{CE} = V_{IL}$, outputs open V_{CC} = max, f = $1/t_{AVAV}$	1,2,3	01,03		120	mA
				02,04		130	
				05,06		150	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, outputs open V_{CC} = max, f = 0 Hz	1,2,3	01,03,05		20	mA
				02,04,06		50	
Standby power supply current (CMOS)	I_{CC3}	V_{CC} +0.2 V $\ge \overline{CE} \ge V_{CC}$ -0.2 V outputs open V_{CC} +0.2 V $\ge V_{IN} \ge V_{CC}$ -0.2 V or +0.2 V $\ge V_{IN} \ge$ -0.2 V f = 0 Hz	1,2,3	01,03,05		5	mA
				02,04,06		20	
Data retention current	I_{CC4}	$V_{CC} = V_{DR}$ = 2.0 V	1,2,3	01,03,05		600	µA
Input capacitance 1/	C_{IN}	V_I = 0 V f = 1 MHz, T_A = +25°C See 4.3.1c	4	All		10	pF
Output capacitance 1/	C_{OUT}	V_O = 0 V f = 1 MHz, T_A = +25°C See 4.3.1c	4	All		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ $V_{SS} = 0$ V, 4.5 V $\leq V_{CC} \leq 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	2/ 3/ 4/	9,10,11	01,02	25		ns
				03,04	20		
				05,06	15		
Address cycle time	t_{AVQV}		9,10,11	01,02		25	ns
				03,04		20	
				05,06		15	
Chip-enable access time	t_{ELQV}		9,10,11	01,02		25	ns
				03,04		20	
				05,06		15	
Output hold from address change	t_{AVQX}		9,10,11	All	0		ns
Output enable to output valid	t_{OLQV}		9,10,11	All		15	ns
Chip select to output in low-Z 1/ 5/	t_{ELQX}		9,10,11	All	3		ns
Output enable to output in low-Z 1/ 5/	t_{OLQX}		9,10,11	All	3		ns
Chip select to output in high-Z 1/ 5/	t_{EHQZ}		9,10,11	All		10	ns
Output disable to output in high-Z 1/ 5/	t_{OHQZ}		9,10,11	All		10	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write enable to output in high-Z 1/ 5/	t_{WLQZ}	2/ 3/ 4/	9,10,11	01,02		15	ns
				03,04		12	
				05,06		10	
Data valid to end of write	t_{DVWH}		9,10,11	01,02	15		ns
				03,04	12		
				05,06	10		
Data hold time	t_{WHDX}		9,10,11	All	0		ns
Output active from end of write 1/ 5/ write	t_{WHQX}		9,10,11	All	3		ns
Write-cycle time 1/	t_{AVAV}		9,10,11	01,02	25		ns
				03,04	20		
				05,06	15		
Chip-select to end of write 4/	t_{ELWH}		9,10,11	01,02	20		ns
				03,04	17		
				05,06	14		
Address valid to end of write	t_{AVWH}		9,10,11	01,02	20		ns
				03,04	17		
				05,06	14		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address-setup time	t_{AVWL}	2/ 3/ 4/	9,10,11	All	0		ns
Write pulse width	t_{WLWH}		9,10,11	01,02	20		ns
				03,04	17		
				05,06	14		
Write recovery time	t_{EHAX}		9,10,11	01-06	0		ns
Chip disable to data retention time	t_{CDR}		9,10,11	01,03,05	0		ns
Data retention recovery time	t_R		9,10,11	01,03,05	t_{AVAV}		ns

1/ This parameter tested intially and after any design or process change which could affect this parameter, and is therefore guaranteed to the limits specified in table I.
2/ For timing waveforms, see figure 3.
3/ AC parameters are tested using input rise and fall times of 5 ns and input pulse levels of GND to 3.0 V. Both input and output timing reference levels are 1.5 V, and the output load is shown on figure 4.
4/ Both chip selects must be active low for the device to be selected.
5/ Transition is measured ±500 mV from steady state.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125°C$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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Device types	01 - 06	
Case outlines	L	X
Terminal number	Terminal symbol	
1	A_0	NC
2	A_1	NC
3	A_2	A_0
4	A_3	A_1
5	A_4	A_2
6	A_5	A_3
7	A_6	A_4
8	A_7	A_5
9	A_8	A_6
10	$\overline{CE}_1$	A_7
11	$\overline{OE}$	A_8
12	GND	$\overline{CE}_1$
13	$\overline{WE}$	$\overline{OE}$
14	I/O_1	GND
15	I/O_2	$\overline{CE}_2$
16	I/O_3	$\overline{WE}$
17	I/O_4	I/O_1
18	$\overline{CE}_2$	I/O_2
19	A_9	I/O_3
20	A_{10}	I/O_4
21	A_{11}	A_9
22	A_{12}	A_{10}
23	A_{13}	A_{11}
24	V_{CC}	A_{12}
25	---	A_{13}
26	---	NC
27	---	NC
28	---	V_{CC}

NC = no connection

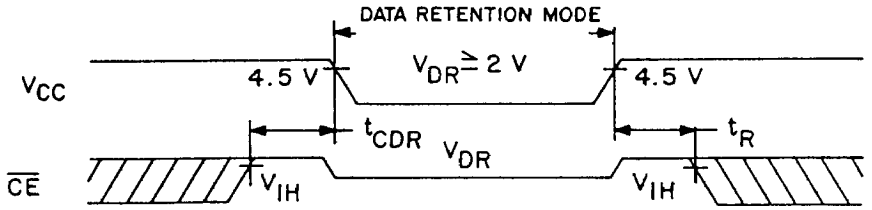
FIGURE 1. Terminal connections.

Mode	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	X	High-Z	Standby
Standby	X	H	X	X	High-Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write	L	L	L	X	D_{IN}	Active
Read	L	L	H	H	High-Z	Active

FIGURE 2. Truth table.

Low V_{CC} data retention waveform

(Device types 01, 03, and 05)



NOTE: t_{CDR} = 0 ns (minimum); may not be tested, but is guaranteed.
$t_r = t_{AVAX}$

Timing waveform of read cycle no. 1

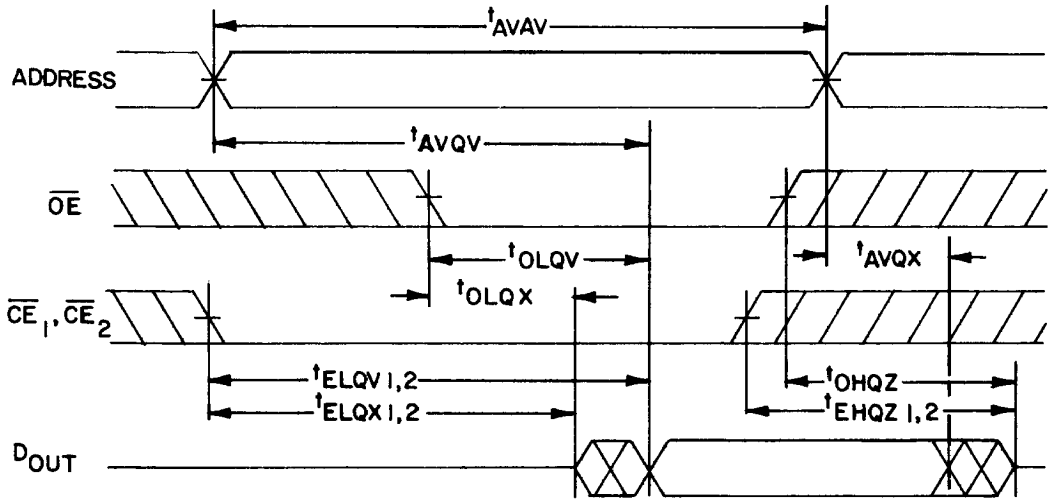
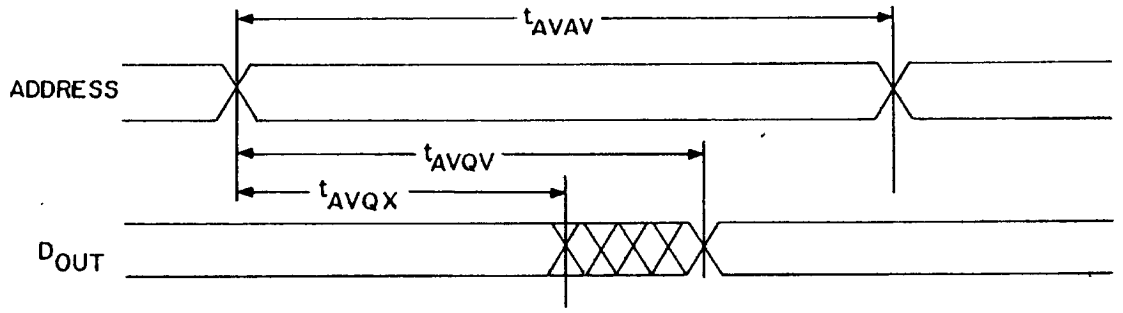


FIGURE 3. Switching time waveforms.

Timing waveform of read cycle no. 2



Timing waveform of read cycle no. 3

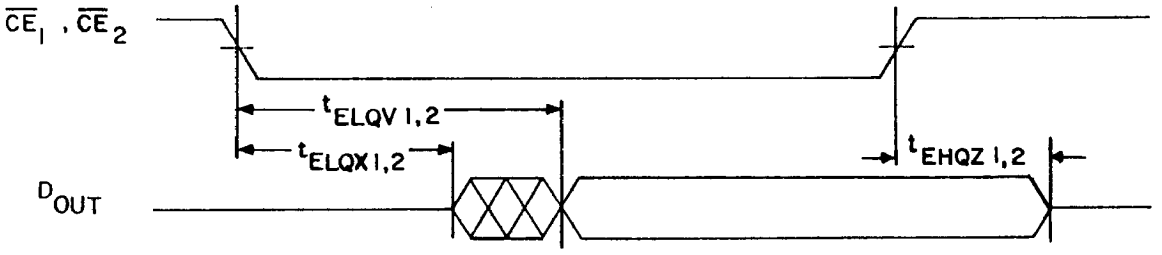


FIGURE 3. Switching time waveforms - Continued.

Timing waveform of write cycle no. 1

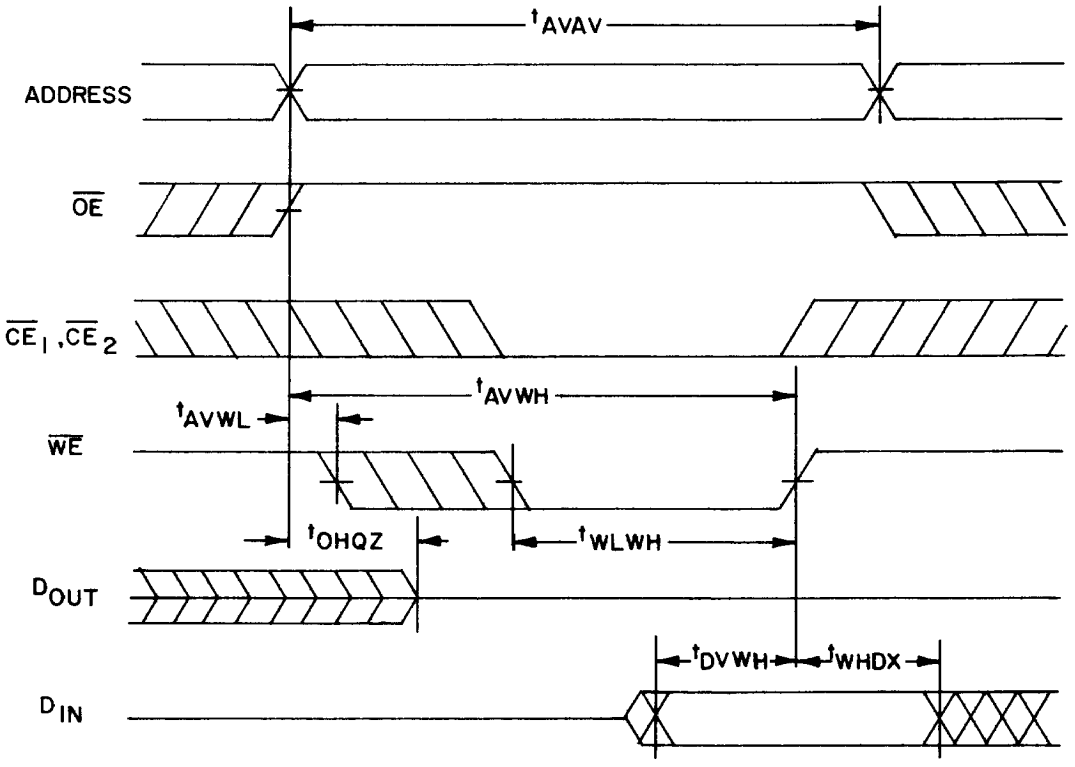


FIGURE 3. Switching time waveforms - Continued.

Timing waveform of write cycle no. 2

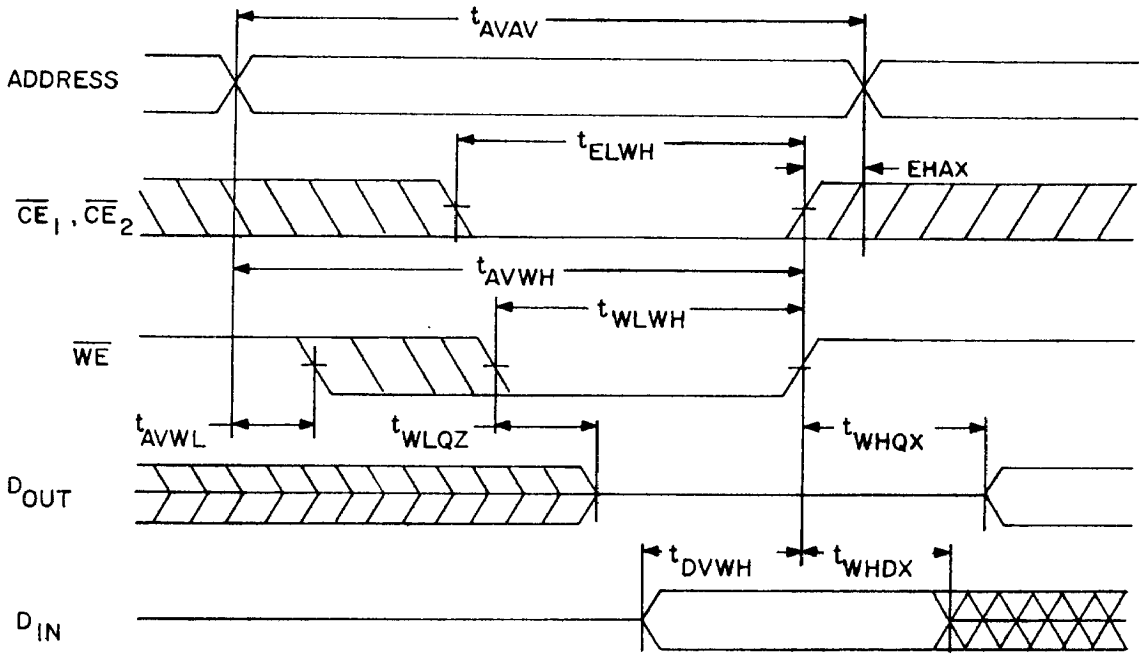
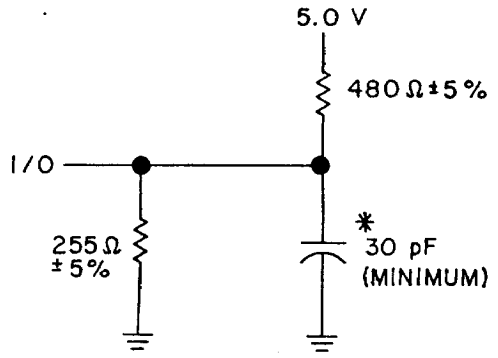
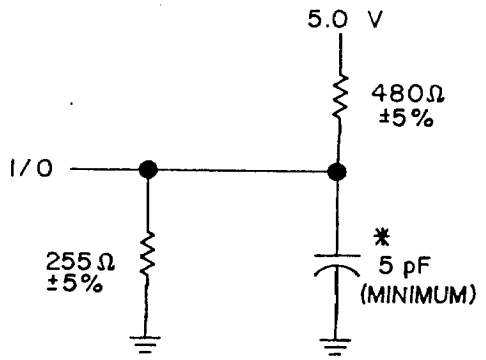


FIGURE 3. Switching time waveforms - Continued.



Circuit A or equivalent



Circuit B or equivalent

for (t_{ELQX}, t_{OLQX}, t_{EHQZ}, t_{OHQZ}, t_{WLQZ}, t_{WHQX})

*Including scope and jig

FIGURE 4. Output load circuits.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A, 8B,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, (8A,8B)***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroup 1 and 7
** See 4.3.1c.
*** See 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) have submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8989101LX	61772 75569	7198L25CB P4C198AL-25CMB
5962-8989101XX	61772	7198L25L28B
5962-8989102LX	61772 75569	7198S25CB P4C198A-25CMB
5962-8989102XX	61772	7198S25L28B
5962-8989103LX	61772	7198L20CB
5962-8989103XX	61772	7198L20L28B
5962-8989104LX	61772 75569	7198S20CB P4C198A-20CMB
5962-8989104XX	61772	7198S20L28B
5962-8989105LX	61772	7198L15CB
5962-8989105XX	61772	7198L15L28B
5962-8989106LX	61772 75569	7198S15CB P4C198A-15CMB
5962-8989106XX	61772	7198S15L28B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 1566 Moffet Boulevard Salinas, CA 95054 Point of contact: 3236 Scott Boulevard Santa Clara, CA 95054
75569	Performance Semiconductor Corporation 610 East Weddell Drive Sunnyvale, CA 94089

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