

**LIBERTY
CHIP™ IC**

Am99C58/Am99C59

4096 x 4 CMOS Static Random-Access Memory
PRELIMINARY

046408

24 pin

Am99C58/Am99C59

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 4096 x 4 organization
- High Speed
 - 20 ns t_{AA} Maximum
 - 10 ns t_{ACS} Maximum (Am99C59)
- Separate data inputs and outputs
- Automatic power-down when deselected (Am99C58)
- Maximum power dissipation: 990 mW
- Maximum standby power dissipation: 220 mW (Am99C58)
- TTL-compatible inputs and outputs
- Single +5-V $\pm 10\%$ power supply
- Slim 24-pin, 300-mil DIP and 28-pin ceramic leadless carrier

GENERAL DESCRIPTION

The Am99C58 and Am99C59 are high-performance CMOS Static RAMs organized as 4096 words by 4 bits. They are manufactured using an advanced high-performance CMOS process that combines high speed with low-power consumption and increased reliability.

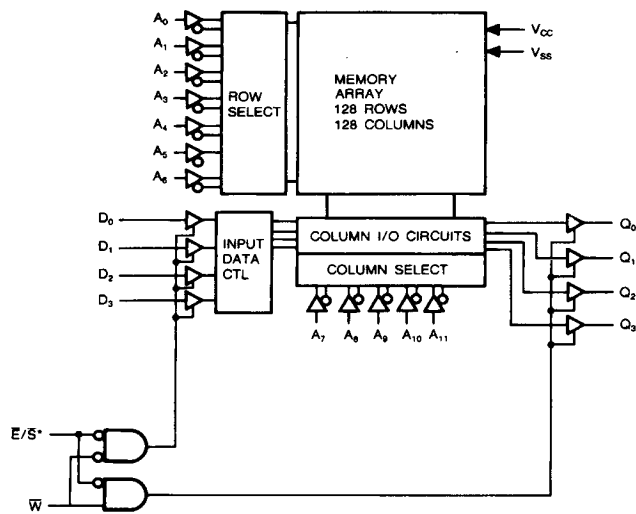
Both devices feature access times as fast as 20 ns and separate data inputs and outputs. The Am99C58 and Am99C59 operate from a single 5-V supply and all inputs and outputs are fully TTL-compatible. The Am99C58 provides a Chip Enable ($\bar{E}$) function that automatically powers down the device when deselected. The Am99C59 provides

a Chip Select ($\bar{S}$) function that offers a chip select access time of 10 ns.

Two inputs, $\bar{E}/\bar{S}^*$ and $\bar{W}$, are used to control the device. Chip Enable/Select ($\bar{E}/\bar{S}^*$) selects the device for operation and provides for easy memory expansion. Write Enable ($\bar{W}$) controls write and read operations. The data outputs will be in a high-impedance state when $\bar{E}/\bar{S}^*$ is HIGH, or $\bar{W}$ is LOW.

The Am99C58 and Am99C59 are packaged in a slim 24-pin, 300-mil DIP or 28-pin ceramic leadless chip carrier.

BLOCK DIAGRAM



BD006491

* $\bar{E}$ =Am99C58
 $\bar{S}$ =Am99C59

S-3

Orig

001662

7 1662

HMID

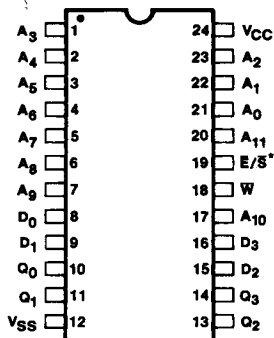
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Publication #	Rev.	Amendment
08116	B	/0
Issue Date: August 1986		

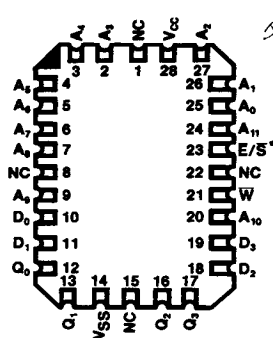
PRODUCT SELECTOR GUIDE

Part Number		Am99C58				Am99C59			
		-20	-25	-35	-45	-20	-25	-35	-45
Access Time Max. (ns)		20	25	35	45	20	25	35	45
0 to +70°C	I _{CC} Max. (mA)	180	180	160	160	180	180	160	160
	I _{SB} Max. (mA)	40	40	40	40	—	—	—	—
	I _{SBC} Max. (mA)	10	10	10	10	—	—	—	—
-55 to +125°C	I _{CC} Max. (mA)	—	—	180	180	—	—	180	180
	I _{SB} Max. (mA)	—	—	40	40	—	—	—	—
	I _{SBC} Max. (mA)	—	—	10	10	—	—	—	—

CONNECTION DIAGRAMS Top View



CD009012



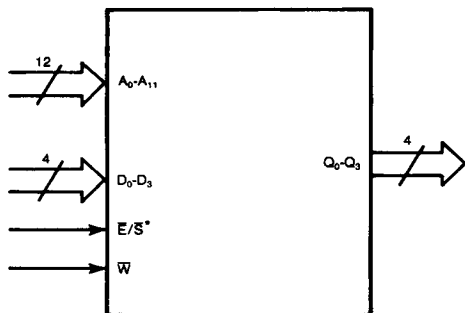
CD005933

* $\bar{E}$ = Am99C58

$\bar{S}$ = Am99C59

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS009651

* $\bar{E}$ = Am99C58

$\bar{S}$ = Am99C59

ADDRESS DESIGNATORS

External	Internal	Pin Number DIP Package
A ₀	AX ₀	21
A ₁	AX ₁	22
A ₂	AX ₂	23
A ₃	AX ₃	1
A ₄	AX ₄	2
A ₅	AX ₅	3
A ₆	AX ₆	4
A ₇	AY ₀	5
A ₈	AY ₁	6
A ₉	AY ₂	7
A ₁₀	AY ₃	17
A ₁₁	AY ₄	20

PIN DESCRIPTION

A₀ – A₁₁ Address (Inputs)

The 12 address inputs select one of the 4096 4-bit words in the RAM.

$\overline{E}/S$ Chip Enable/Chip Select (Input)

An active-LOW input which selects the device for operation. When $\overline{E}/S$ is HIGH, the device is deselected and the outputs will be in a high-impedance state. The $\overline{E}$ pin will also power down the Am99C58 when HIGH.

$\overline{W}$ Write Enable (Input)

$\overline{W}$ controls read and write operations. When $\overline{W}$ is HIGH and $\overline{E}/S$ is LOW, data will be present at the data outputs. When

$\overline{W}$ is LOW, data present on the data inputs will be written into the selected memory location. The data outputs will be in a high-impedance state.

D₀ – D₃ Data Input

Data inputs to the RAM.

Q₀ – Q₃ Data Output

Data outputs from the RAM. The data outputs will be in a high-impedance state when $\overline{E}/S$ is HIGH or $\overline{W}$ is LOW.

V_{CC} Power Supply +5 Volts

V_{SS} Ground

TABLE 1. MODE SELECT

Inputs		Outputs	Mode	Power
$\overline{E}/S$	$\overline{W}$			
H	X	Hi-Z	Not Selected	•
L	L	Hi-Z	Write	Active
L	H	Data Out	Read	Active

H = HIGH

L = LOW

X = Don't Care

*The Am99C58 will be in Standby;

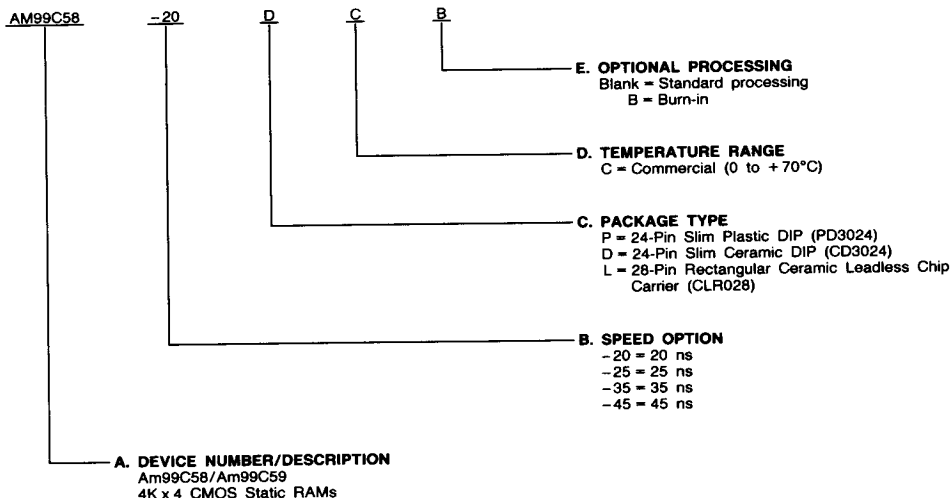
The Am99C59 will be Active

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations	
AM99C58-20	PC, PCB, DC, DCB, LC, LCB
AM99C58-25	
AM99C58-35	
AM99C58-45	
AM99C59-20	
AM99C59-25	
AM99C59-35	
AM99C59-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

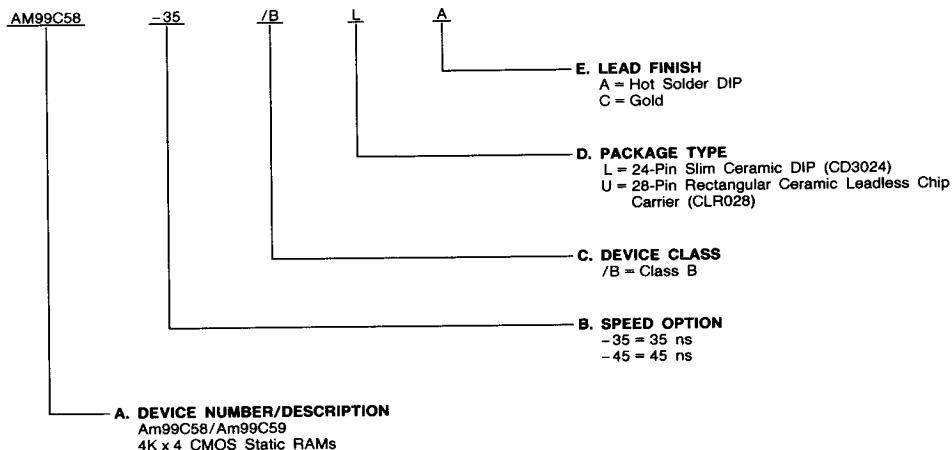
preliminary

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



Valid Combinations	
AM99C58-35	/BLA, /BUC
AM99C58-45	
AM99C59-35	
AM99C59-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

883 class B

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature -65 to +150°C
 Ambient Temperature with
 Power Applied -55 to +125°C
 Supply Voltage with
 Respect to Ground -0.5 V to +7.0 V
 Signal Voltages with
 Respect to Ground -0.5 V to +7.0 V
 Power Dissipation (Package Limitation) 1.2 W
 DC Output Current 20 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices

Temperature (T_A) 0 to +70°CSupply Voltage (V_{CC}) +5.0 V ±10%

Military (M) Devices*

Temperature (T_C) -55 to +125°CSupply Voltage (V_{CC}) +5.0 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions	Am99C58-20, -25 Am99C59-20, -25		Am99C58-35, -45 Am99C59-35, -45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4 mA	2.4		2.4		
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8 mA		0.4		0.4	
V _{IH}	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V _{IL}	Input LOW Voltage	(Note 3)	-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-2.0	2.0	-2.0	2.0	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-10	10	-10	10	μA
I _{CC}	V _{CC} Operating Supply Current	Max V _{CC} , E/S ≤ V _{IL} , Output Open Cycle = Min.	C Devices	180		160	mA
			M Devices	NA		180	
I _{SB}	Standby Power Supply Current, TTL Input Levels (Am99C58 only)	Max. V _{CC} , E = V _{IH}	C Devices	40		40	mA
			M Devices	NA		40	
I _{SB} C	Standby Power Supply Current, CMOS Input Levels (Am99C58 only)	Max. V _{CC} , E ≥ V _{CC} - 0.2 V V _{IN} ≥ V _{CC} - 0.2 V or ≤ 0.2 V	C Devices	10		10	mA
			M Devices	NA		10	

- Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
 2. For test and correlation purposes, operating temperature is defined as the "instant-ON" case temperature.
 3. V_{IL} = -1.5 V for pulse width less than 10 ns.
 4. This parameter is not tested, but guaranteed by characterization.
 5. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
 6. W is HIGH for read cycle.
 7. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 1b under Switching Test Circuits.
 8. The internal write time of the memory is defined by the overlap of E/S LOW and W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing is referenced to the rising edge of the signal that terminates the write.
 9. E/S is LOW for read cycle.
 10. Address Valid prior to or coincident with E/S LOW.
 11. E/S or W must be HIGH during address transitions.
 12. If E goes HIGH simultaneously with W HIGH, the output remains in a high-impedance state.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Min.	Max.	Units
C _I	Input Capacitance	Test Frequency = 1.0 MHz T _A = 25°C, All Pins at 0 V, V _{CC} = 5 V (Note 4)		5		5	pF
C _O	Output Capacitance			7		7	

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Note 5)

No.	Parameter Symbol		Parameter Description	Am99C58-20 Am99C59-20		Am99C58-25 Am99C59-25		Am99C58-35 Am99C59-35		Am99C58-45 Am99C59-45		Units	
	Standard	Alternate		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
READ CYCLE													
1	tAVAV	tRC	Read Cycle Time (Note 6)		20		25		35		45	ns	
2	tAVQV	tAA	Address Access Time			20		25		35		45	ns
3	tELQV	tACE	Chip Enable Access Time	Am99C58 only		20		25		35		45	ns
4	tSLQV	tACS	Chip Select Access Time	Am99C59 only		10		15		20		25	ns
5	tELQX tSLQX	tCLZ	Chip Enable/Select LOW to Output in Low-Z (Notes 4 & 7)		0		0		0		0		ns
6	tEHQZ tSHQZ	tCHZ	Chip Enable/Select HIGH to Output in Hi-Z (Notes 4 & 7)		0	15	0	20	0	25	0	30	ns
7	tAXQX	tOHA	Output Hold after Address Change	C Devices	3		3		3		3		ns
				M Devices	1		1		1		1		
8	tELICCH	tPU	Chip Enable to Power Up (Am99C58) (Note 4)		0		0		0		0		ns
9	tEHICCL	tPD	Chip Disable to Power Down (Am99C58) (Note 4)		0	20	0	25	0	35	0	40	ns
WRITE CYCLE													
10	tAVAV	tWC	Write Cycle Time (Note 8)		20		25		35		45		ns
11	tELWH tSLWH	tCW	Chip Enable/Select LOW to Write Enable HIGH		15		20		30		40		ns
12	tAVWH	tAW	Address Valid to End of Write		15		20		30		40		ns
13	tAVWL	tAS	Address Valid to Beginning of Write		0		0		0		0		ns
14	tWLWH	tWP	Write Pulse Width		15		20		30		40		ns
15	tWHAX	tWR	Address Hold after End of Write		5		5		5		5		ns
16	tDVWH	tDW	Data in Valid to Write Enable HIGH		10		10		15		20		ns
17	tWHDX	tDH	Data Hold after End of Write		5		5		5		5		ns
18	tWLQZ	tWZ	Write Enable LOW to Output in Hi-Z (Notes 4 & 7)		0	10	0	10	0	15	0	20	ns
19	tWHQX	tOW	Write Enable HIGH to Output in Low-Z (Notes 4 & 7)		0		0		0		0		ns

Notes: See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS

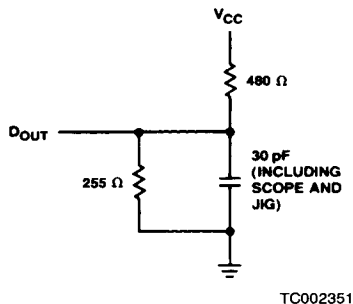


Figure 1a.

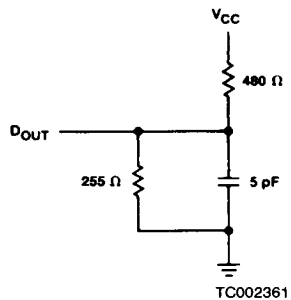


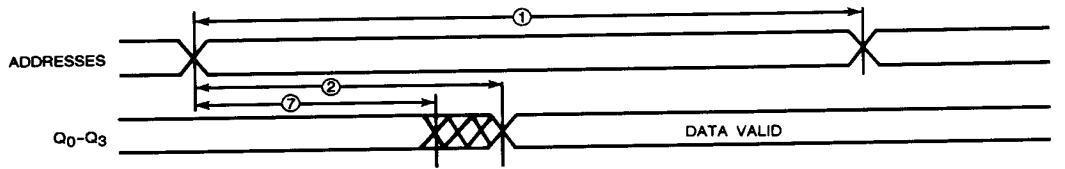
Figure 1b.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

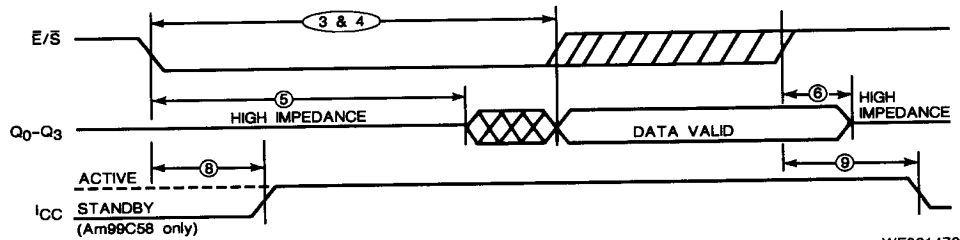
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SWITCHING WAVEFORMS



WF021462

Read Cycle One
(Notes 6 & 9)

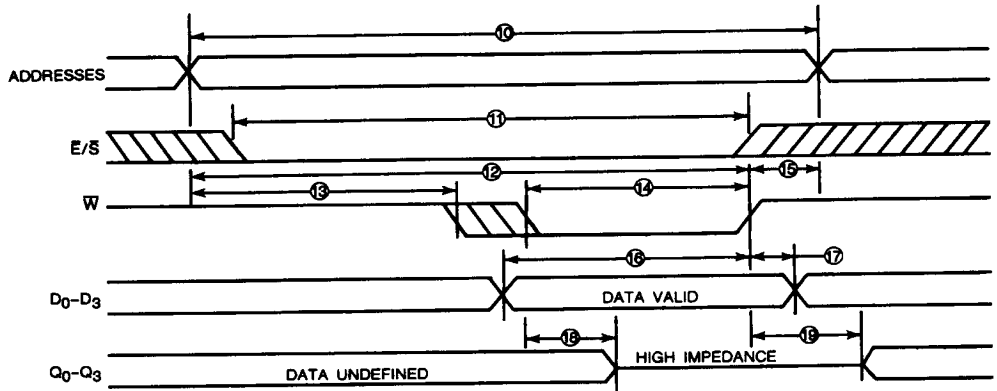


WF021472

Read Cycle Two
(Notes 6 & 10)

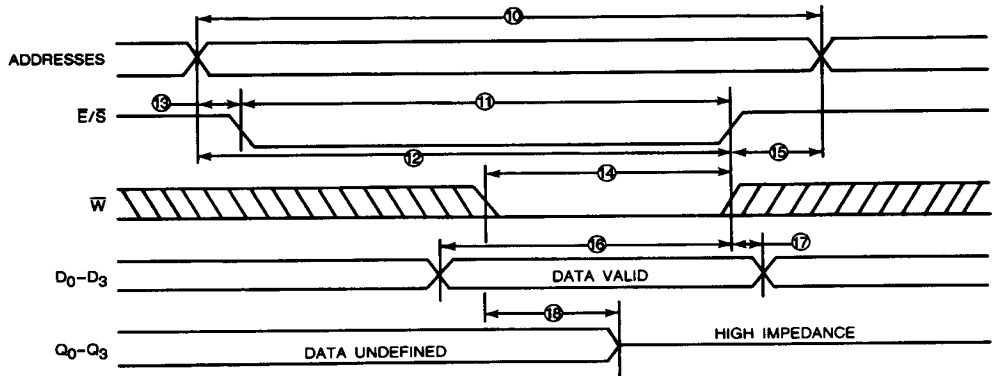
Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



WF021442

Write Cycle One ($\bar{W}$ Controlled)
(Notes 11 & 12)



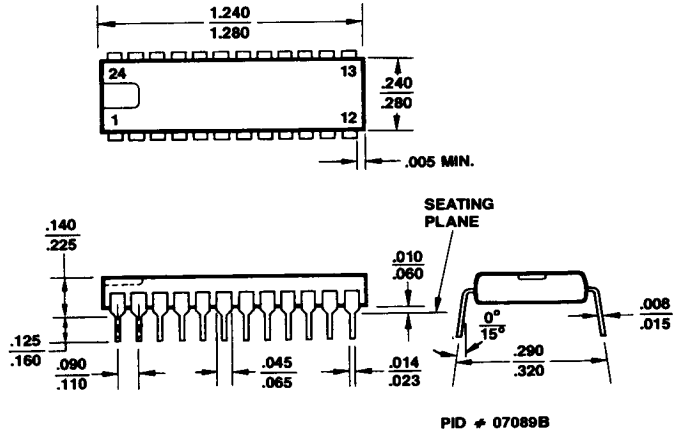
WF021452

Write Cycle Two ($\bar{E}/\bar{S}$ Controlled)
(Notes 11 & 12)

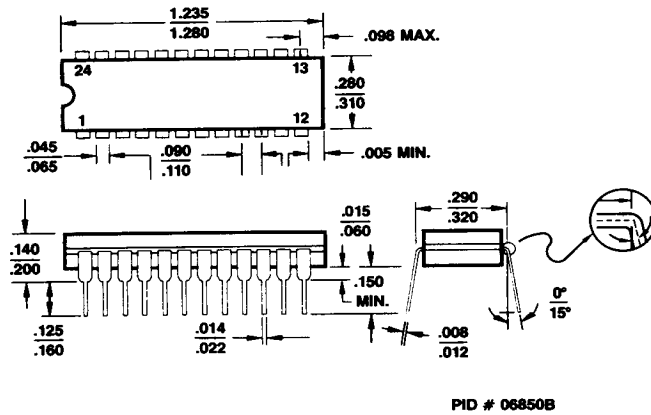
Notes: See notes following DC Characteristics table.

PHYSICAL DIMENSIONS

PD3024



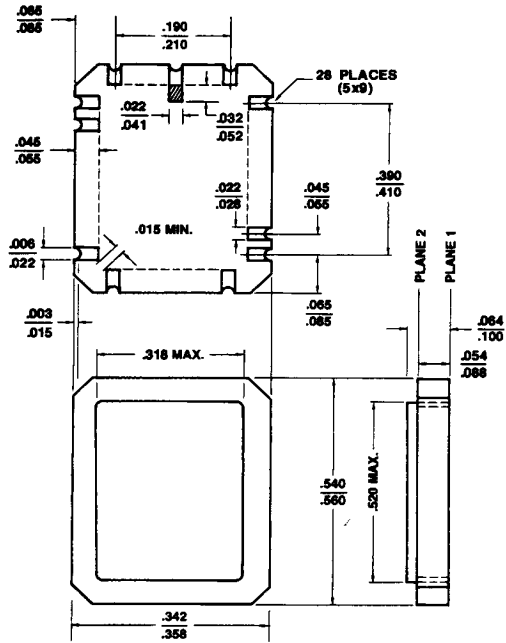
CD3024



PHYSICAL DIMENSIONS (Cont'd.)

CLR028

#125



PID # 06852B

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups	
V _{OH}	1, 2, 3	
V _{OL}	1, 2, 3	
V _{IH}	7, 8	
V _{IL}	7, 8	
I _{Ix}	1, 2, 3	
I _{OZ}	1, 2, 3	
I _{CC}	1, 2, 3	
I _{SB}	1, 2, 3	Am99C58 only
I _{SBC}	1, 2, 3	

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t _{AVAV} (t _{RC})	7, 8, 9, 10, 11	16	t _{DVWH} (t _{DW})	7, 8, 9, 10, 11
2	t _{AVQV} (t _{AA})	7, 8, 9, 10, 11	17	t _{WHDx} (t _{DH})	7, 8, 9, 10, 11
3	t _{ELQV} (t _{ACE}) (Am99C58 only)	7, 8, 9, 10, 11			
4	t _{SLQV} (t _{ACS}) (Am99C59 only)	7, 8, 9, 10, 11			
7	t _{AXQX} (t _{OHA})	7, 8, 9, 10, 11			
10	t _{AVAV} (t _{WC})	7, 8, 9, 10, 11			
11	t _{SLWH} (t _{CW}) t _{ELWH}	7, 8, 9, 10, 11			
12	t _{AVWH} (t _{AW})	7, 8, 9, 10, 11			
13	t _{AVWL} (t _{AS})	7, 8, 9, 10, 11			
14	t _{WLWH} (t _{WP})	7, 8, 9, 10, 11			
15	t _{WHAX} (t _{WR})	7, 8, 9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.