

256Kx8 Static RAM CMOS, Module

Features

256Kx8 bit CMOS Static

Random Access Memory

- Access Times 70, 85 and 100ns
- Data Retention Function (LP version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

High Density Packaging

- 32 Pin SOIC Module, No. 21
- 32 Pin DIP Module, No. 184

Single +5V ($\pm 10\%$) Supply Operation

The EDI8F8257C is a two megabit CMOS Static RAM based on two 128Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

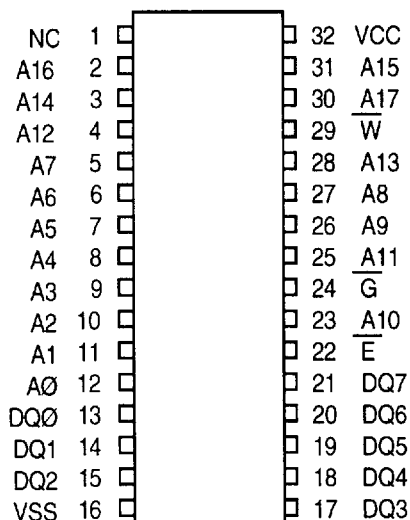
Functional equivalence to the monolithic two megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address (A17) to select one of the 128Kx8 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the two megabit device, to ensure compatibility with future monolithics.

The device is available with Low Power and Data Retention (EDI8F8257LP).

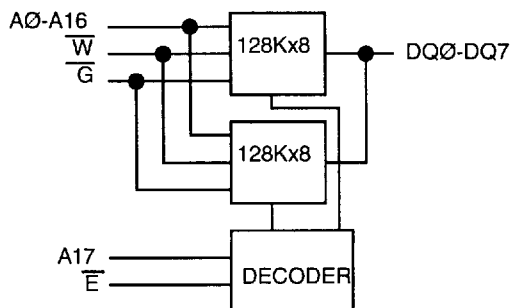
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F8257C requires no clocks or refreshing for operation.

Pin Configurations and Block Diagram



Pin Names

A0-A17	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	1 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 100pF

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power	ICC1	$\bar{W}, \bar{E} = VIL, I/O = 0mA,$	--	110	130	mA
Supply Current		Min Cycle				
Standby (TTL) Power	ICC2	$\bar{E} \geq VIH, VIN \leq VIL$	--	10	35	mA
Supply Current		$VIN \geq VIH$				
Full Standby Power	ICC3	$\bar{E} \geq VCC-0.2V$	--	2	5	mA
Supply Current (CMOS)		$VIN \geq VCC-0.2V$	--	40	400	μA
		$VIN \leq 0.2V$				
Input Leakage Current	ILI	$VIN = 0V$ to VCC	-10	--	10	μA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC	-10	--	10	μA
Output High Voltage	VOH	$IOH = -1.0mA$	2.4	--	--	V
Output Low Voltage	VOL	$IOL = 2.1mA$	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\bar{G}$	$\bar{E}$	$\bar{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance			
(Except DQ Pins)	CI	15	pF
Capacitance (DQ Pins)	CDI/Q	20	pF
Input (E)	CC	10	pF
Input (W) Line	CW	15	pF

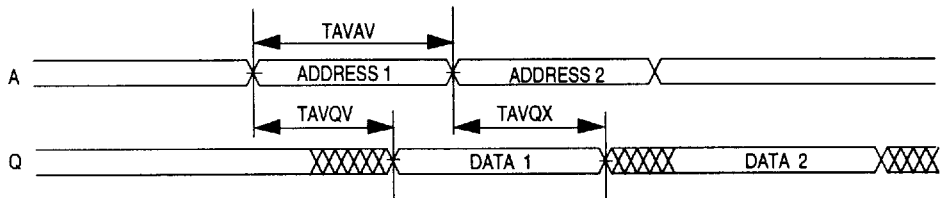
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

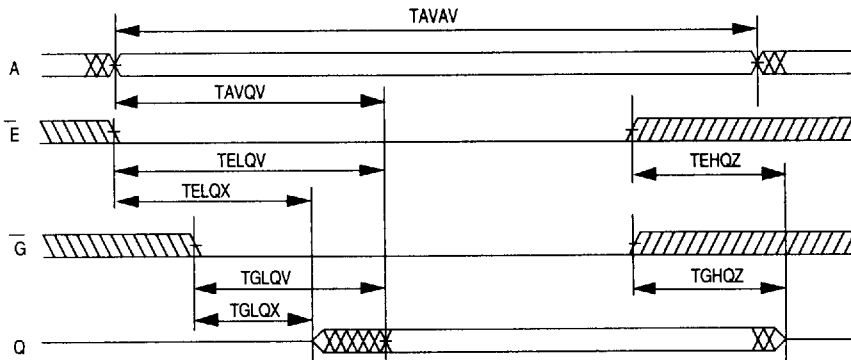
Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		30		35		40	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns

Note: Parameter guaranteed, but not tested

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High

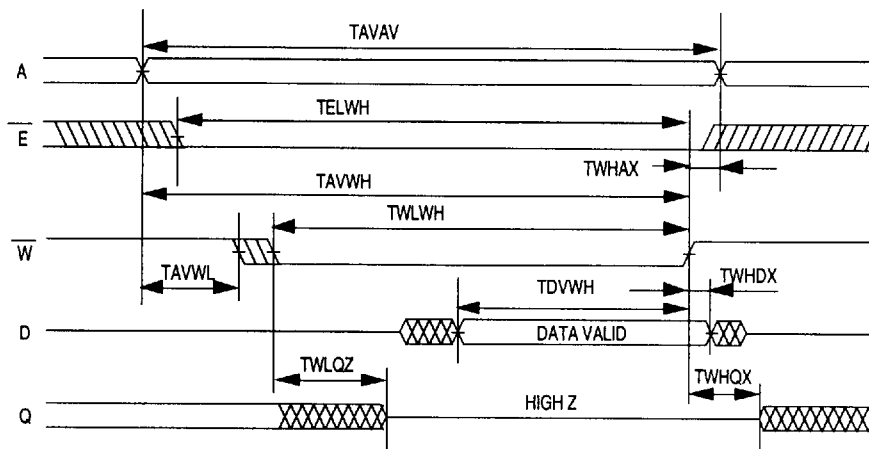


AC Characteristics Write Cycle

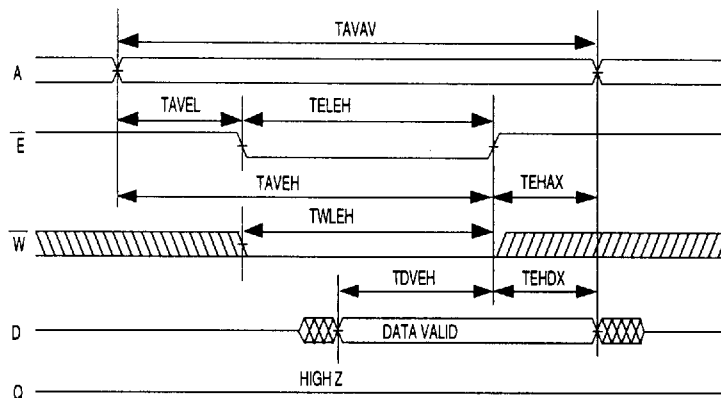
Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	65		70		80		ns
	TELEH	TCW	65		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	65		70		80		ns
	TAVEH	TAW	65		70		80		ns
Write Pulse Width	TWLWH	TWP	65		70		80		ns
	TWLEH	TWP	65		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW	30		35		40		ns
	TDVEH	TDW	30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - W Controlled



Write Cycle 2 - $\bar{E}$ Controlled



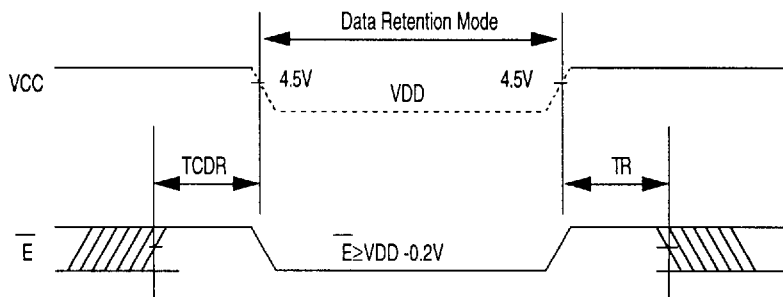
Data Retention Characteristics

LP Version Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 0.2V $\bar{E} \geq VDD - 0.2V$ VIN $\geq VDD - 0.2V$ or VIN $\leq 0.2V$				70°C 85°C	
Data Retention Quiescent Current	ICCDR		2V	–	10	125 185	μA
			3V	–	20	200 250	μA
Chip Disable to Data Retention Time	TCDR			0	–	–	ns
Operation Recovery Time	TR			TAVAV*	–	–	ns

*Read Cycle Time

Data Retention $\bar{E}$ Controlled



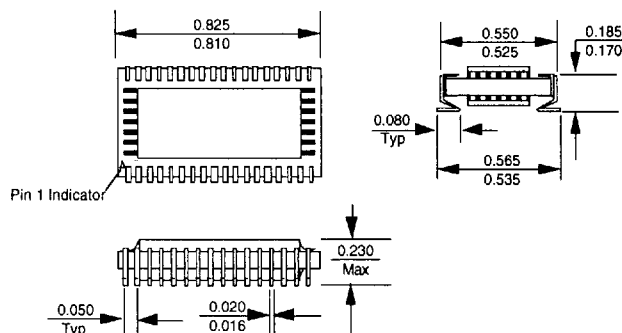
Ordering Information

Standard Power	Low Power with Data Retention	Speed (ns)	Package No.
EDI8F8257C70BPC	EDI8F8257LP70BPC	70	21
EDI8F8257C85BPC	EDI8F8257LP85BPC	85	21
EDI8F8257C100BPC	EDI8F8257LP100BPC	100	21
EDI8F8257C70B6C	EDI8F8257LP70B6C	70	184
EDI8F8257C85B6C	EDI8F8257LP85B6C	85	184
EDI8F8257C100B6C	EDI8F8257LP100B6C	100	184

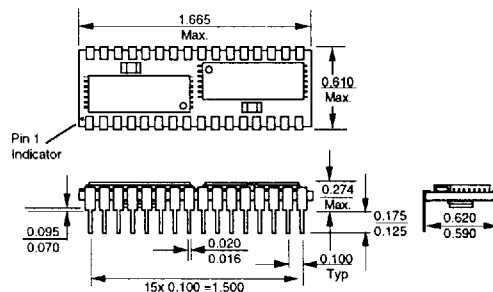
Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I,
eg. EDI8F8257C70BPC becomes EDI8F8257C70BPI.

Package Description

Package No. 21 32 Pin SOIC Module



Package No. 184 32 Pin Dual-in-line Package



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