

NC7SB3157, FSA3157 Low Voltage SPDT Analog Switch or 2:1 Multiplexer/Demultiplexer Bus Switch

General Description

The NC7SB3157 or FSA3157 is a high performance, single-pole/double-throw (SPDT) Analog Switch or 2:1 Multiplexer/Demultiplexer Bus Switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance. The break before make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The control input tolerates voltages up to 5.5V independent of the V_{CC} operating range.

Features

- Useful in both analog and digital applications
- Space saving SC70 6-lead surface mount package
- Ultra small MicroPak™ Pb-Free leadless package
- Low On Resistance; < 10Ω on typ @ 3.3V V_{CC}
- Broad V_{CC} operating range; 1.65V to 5.5V
- Rail-to-Rail signal handling
- Power down high impedance control input
- Overvoltage tolerance of control input to 7.0V
- Break before make enable circuitry
- 250 MHz, 3dB bandwidth

Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SB3157P6X	MAA06A	B7A	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SB3157P6X_NL ¹	MAA06A	B7A	Pb-Free 6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SB3157L6X	MAC06A	BB	Pb-Free 6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel
FSA3157P6X	MAA06A	B7A	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
FSA3157P6X_NL ¹	MAA06A	B7A	Pb-Free 6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
FSA3157L6X	MAC06A	BB	Pb-Free 6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

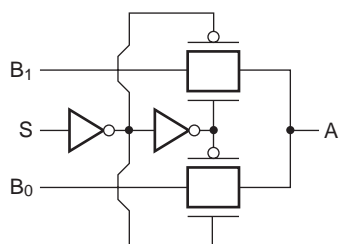
Pb-Free package per JEDEC J-STD-020B.

Note:

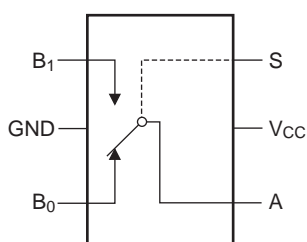
1. “_NL” indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbol



Analog Symbol



Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

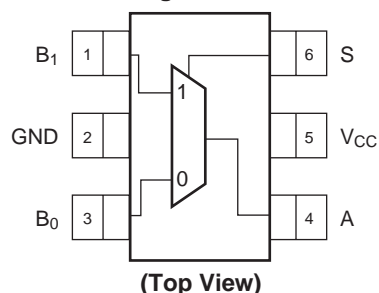
H = HIGH Logic Level
L = LOW Logic Level

Pin Descriptions

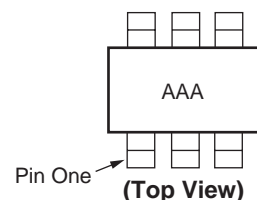
Pin Names	Description
A, B ₀ , B ₁	Data Ports
S	Control Input

Connection Diagrams

Pin Assignments for SC70



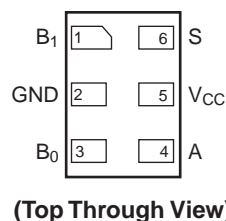
Pin One Orientation Diagram



AAA = Product Code Top Mark, see Ordering Information.

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



Absolute Maximum Ratings

(The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.)

Symbol	Parameter	Rating
V_{CC}	Supply Voltage ()	-0.5V to +7.0V
V_S	DC Switch Voltage ²	-0.5V to V_{CC} +0.5V
V_{IN}	DC Input Voltage ²	-0.5V to +7.0V
I_{IK}	DC Input Diode Current @ (I_{IK}) $V_{IN} < 0V$	-50 mA
I_{OUT}	DC Output Current	128 mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	±100 mA
T_{STG}	Storage Temperature Range	-65°C to +150°C
T_J	Junction Temperature under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation @ +85°C	180 mW
	ESD, Human Body Model	4000V

Recommended Operating Conditions³

Symbol	Parameter	Rating
V_{CC}	Supply Voltage Operating	1.65V to 5.5V
V_{IN}	Control Input Voltage	0V to V_{CC}
V_{IN}	Switch Input Voltage	0V to V_{CC}
V_{OUT}	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
t_r, t_f	Input Rise and Fall Time Control Input $V_{CC} = 2.3V-3.6V$ Control Input $V_{CC} = 4.5V-5.5V$	0 ns/V to 10 ns/V 0 ns/V to 5 ns/V
θ_{JA}	Thermal Resistance	350°C/W

Notes:

- The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
- Control input must be held HIGH or LOW, it must not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level		1.65 – 1.95	0.75 V _{CC}			0.75 V _{CC}		V
	Input Voltage		2.3 – 5.5	0.7 V _{CC}			0.7 V _{CC}		
V _{IL}	LOW Level		1.65 – 1.95			0.25 V _{CC}		0.25 V _{CC}	V
	Input Voltage		2.3 – 5.5			0.3 V _{CC}		0.3 V _{CC}	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5V	0 – 5.5		±0.05	±0.1		±1	μA
I _{OFF}	OFF State Leakage Current	0 ≤ A, B ≤ V _{CC}	1.65 – 5.5		±0.05	±0.1		±1	μA
R _{ON}	Switch On Resistance ⁴	V _{IN} = 0V, I _O = 30 mA	4.5		3.0	7.0		7.0	Ω
		V _{IN} = 2.4V, I _O = -30 mA			5.0	12.0		12.0	Ω
		V _{IN} = 4.5V, I _O = -30 mA			7.0	15.0		15.0	Ω
		V _{IN} = 0V, I _O = 24 mA	3.0		4.0	9.0		9.0	Ω
		V _{IN} = 3V, I _O = -24 mA			10.0	20.0		20.0	Ω
		V _{IN} = 0V, I _O = 8 mA	2.3		5.0	12.0		12.0	Ω
		V _{IN} = 2.3V, I _O = -8 mA			13.0	30.0		30.0	Ω
		V _{IN} = 0V, I _O = 4 mA	1.65		6.5	20.0		20.0	Ω
V _{IN} = 1.65V, I _O = -4 mA		17.0		50.0		50.0	Ω		
I _{CC}	Quiescent Supply Current All Channels ON or OFF	V _{IN} = V _{CC} or GND I _{OUT} = 0	5.5			1		10	μA
	Analog Signal Range		V _{CC}	0		V _{CC}	0	V _{CC}	V
R _{RANGE}	On Resistance Over Signal Range ^{4, 8}	I _A = -30 mA, 0 ≤ V _{Bn} ≤ V _{CC}	4.5					25.0	Ω
		I _A = -24 mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.0					50.0	
		I _A = -8 mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.3					100	
		I _A = -4 mA, 0 ≤ V _{Bn} ≤ V _{CC}	1.65					300	
ΔR _{ON}	On Resistance Match Between Channels ^{4, 5, 6}	I _A = -30 mA, V _{Bn} = 3.15	4.5		0.15				Ω
		I _A = -24 mA, V _{Bn} = 2.1	3.0		0.2				
		I _A = -8 mA, V _{Bn} = 1.6	2.3		0.5				
		I _A = -4 mA, V _{Bn} = 1.15	1.65		0.5				
R _{flat}	On Resistance Flatness ^{4, 5, 7}	I _A = -30 mA, 0 ≤ V _{Bn} ≤ V _{CC}	5.0		6.0				Ω
		I _A = -24 mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.3		12.0				
		I _A = -8 mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.5		28.0				
		I _A = -4 mA, 0 ≤ V _{Bn} ≤ V _{CC}	1.8		125				

Notes:

- Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
- Parameter is characterized but not tested in production.
- ΔR_{ON} = R_{ON} max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
- Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
- Guaranteed by Design.

AC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Figure Number
				Min	Typ	Max	Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus ¹⁰	V _I = OPEN	1.65 – 1.95			3.5		3.5	ns	Figure 7 Figure 8
			2.3 – 2.7			1.2		1.2		
			3.0 – 3.6			0.8		0.8		
			4.5 – 5.5			0.3		0.3		
t _{PZL} , t _{PZH}	Output Enable Time Turn on Time (A to B _n)	V _I = 2 x V _{CC} for t _{PZL} V _I = 0V for t _{PZH}	1.65 – 1.95	7.0		23.0	7.0	24.0	ns	Figure 7 Figure 8
			2.3 – 2.7	3.5		13.0	3.5	14.0		
			3.0 – 3.6	2.5		6.9	2.5	7.6		
			4.5 – 5.5	1.7		5.2	1.7	5.7		
t _{PLZ} , t _{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	V _I = 2 x V _{CC} for t _{PLZ} V _I = 0V for t _{PHZ}	1.65 – 1.95	3.0		12.5	3.0	13.0	ns	Figure 7 Figure 8
			2.3 – 2.7	2.0		7.0	2.0	7.5		
			3.0 – 3.6	1.5		5.0	1.5	5.3		
			4.5 – 5.5	0.8		3.5	0.8	3.8		
t _{B-M}	Break Before Make Time ⁹		1.65 – 1.95	0.5			0.5		ns	Figure 9
			2.3 – 2.7	0.5			0.5			
			3.0 – 3.6	0.5			0.5			
			4.5 – 5.5	0.5			0.5			
Q	Charge Injection ⁹	C _L = 0.1 nF, V _{GEN} = 0V,	5.0		7.0			pC	Figure 10	
		R _{GEN} = 0Ω	3.3		3.0					
OIRR	Off Isolation ¹¹	R _L = 50Ω, f = 10MHz	1.65 – 5.5		-57.0			dB	Figure 11	
Xtalk	Crosstalk	R _L = 50Ω, f = 10MHz	1.65 – 5.5		-54.0			dB	Figure 12	
BW	-3dB Bandwidth	R _L = 50Ω	1.65 – 5.5		250			MHz	Figure 15	
THD	Total Harmonic Distortion ⁹	R _L = 600Ω, 0.5 V _{P-P} f = 600 Hz to 20 KHz	5.0		.011			%		

Capacitance¹²

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C _{IN}	Control Pin Input Capacitance	2.3		pF	V _{CC} = 0V	
C _{IO-B}	B Port Off Capacitance	6.5		pF	V _{CC} = 5.0V	Figure 13
C _{IOA-ON}	A Port Capacitance When Switch Is Enabled	18.5		pF	V _{CC} = 5.0V	Figure 14

Notes:

9. Guaranteed by Design.

10. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

11. Off Isolation = 20 log₁₀ [V_A / V_{Bn}]

12. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

Typical Characteristics

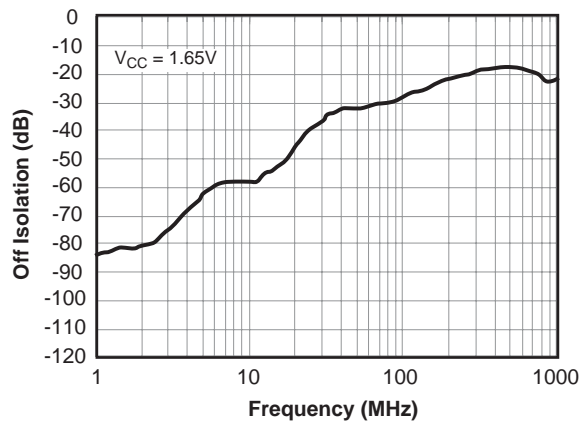


Figure 1. Off Isolation, $V_{CC} = 1.65V$

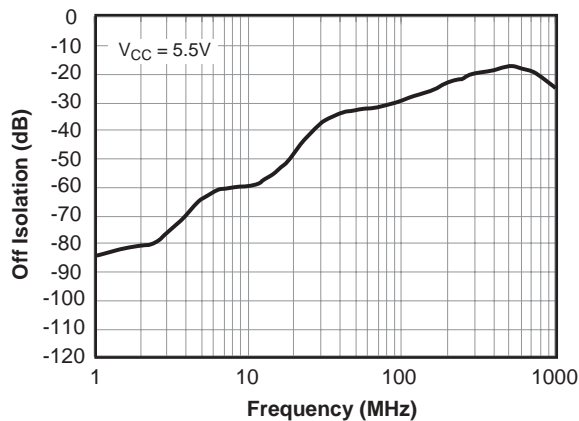


Figure 2. Off Isolation, $V_{CC} = 5.5V$

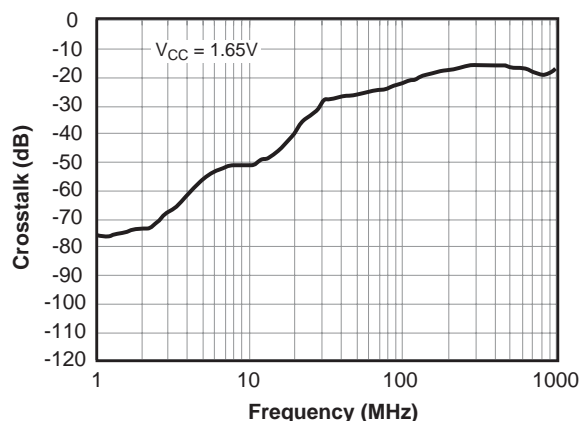


Figure 3. Crosstalk, $V_{CC} = 1.65V$

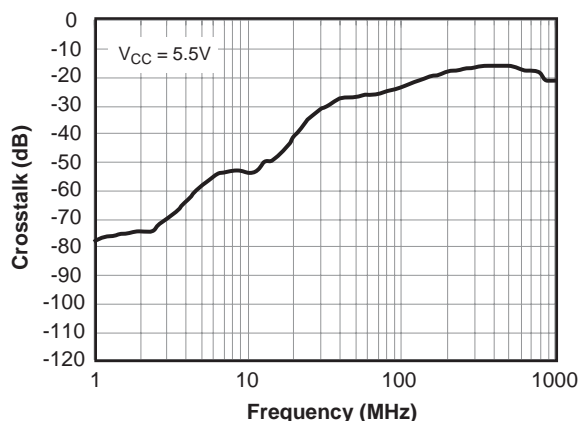


Figure 4. Crosstalk, $V_{CC} = 5.5V$

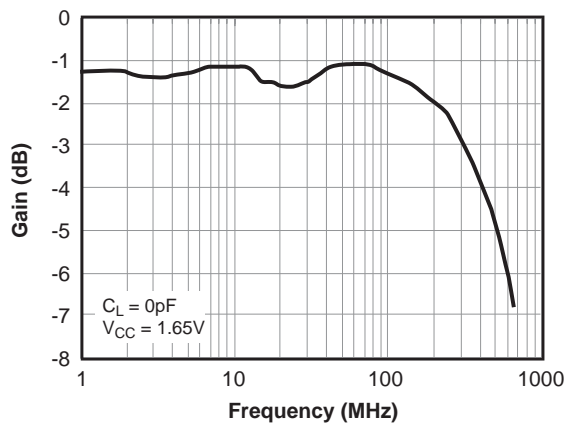


Figure 5. Bandwidth, $V_{CC} = 1.65V$

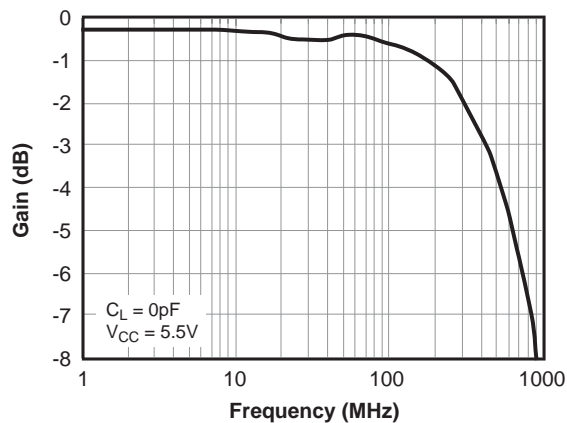
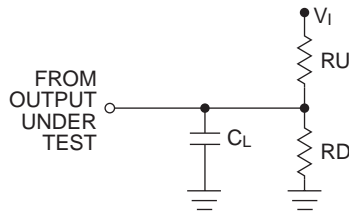


Figure 6. Bandwidth, $V_{CC} = 5.5V$

AC Loading and Waveforms



Notes:
 Input driven by 50Ω source terminated in 50Ω
 C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_W = 500 ns

Figure 7. AC Test Circuit

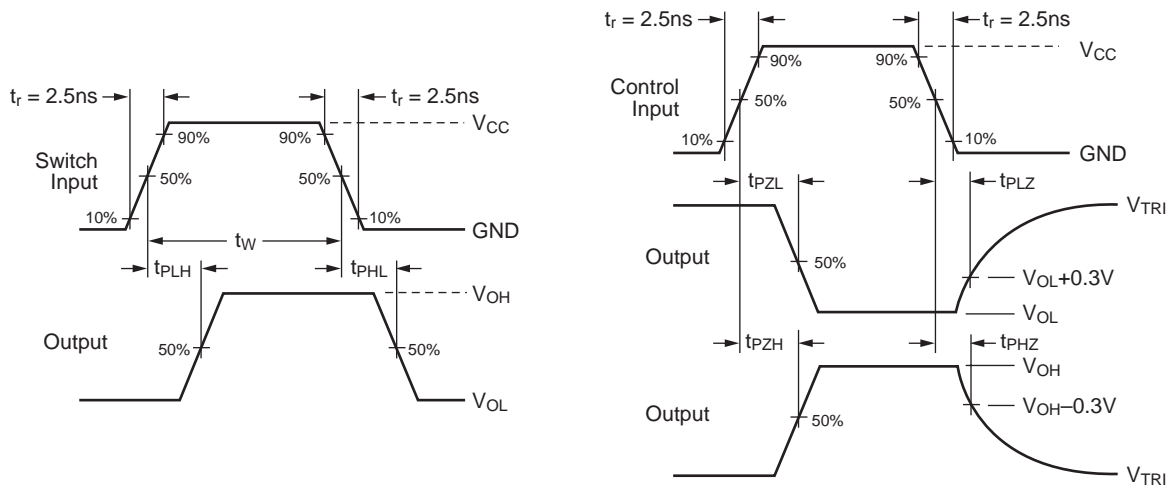


Figure 8. AC Waveforms

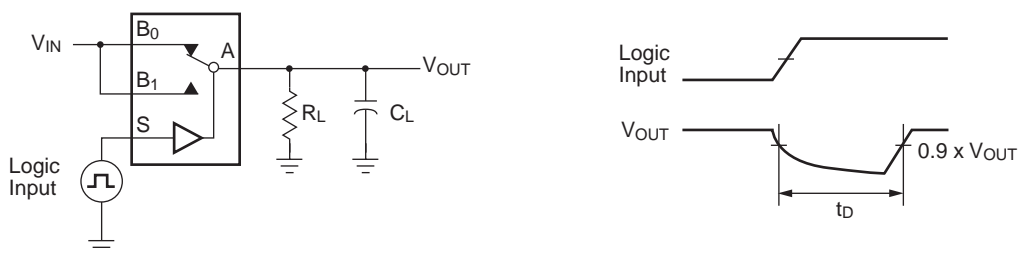


Figure 9. Break Before Make Interval Timing

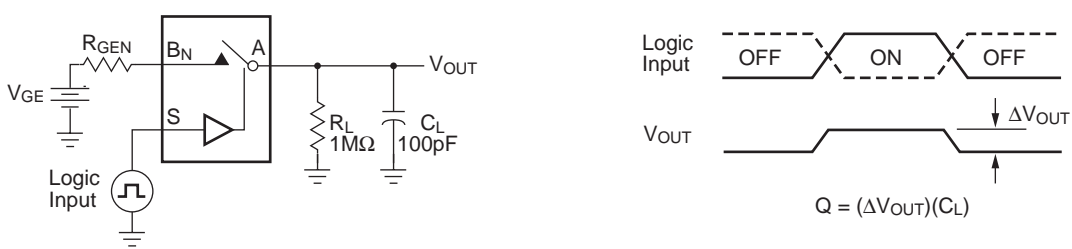


Figure 10. Charge Injection Test

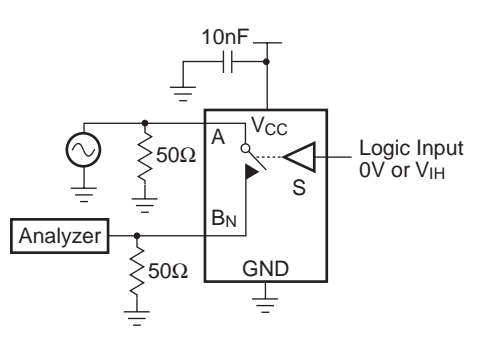


Figure 11. Off Isolation

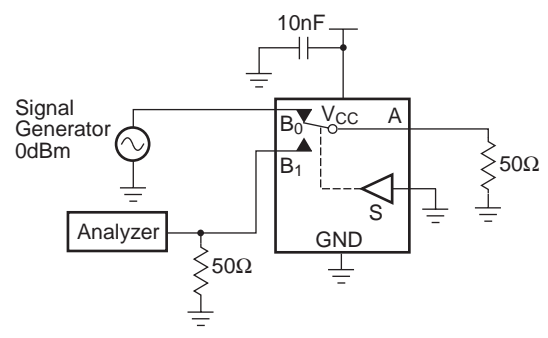


Figure 12. Crosstalk

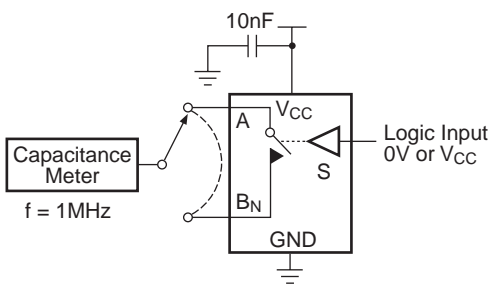


Figure 13. Channel Off Capacitance

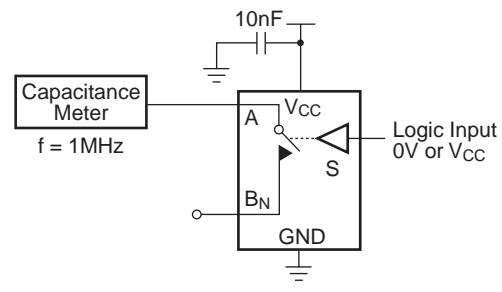


Figure 14. Channel On Capacitance

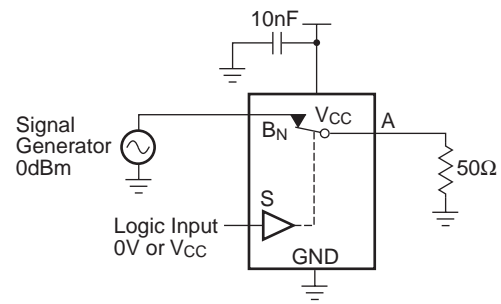


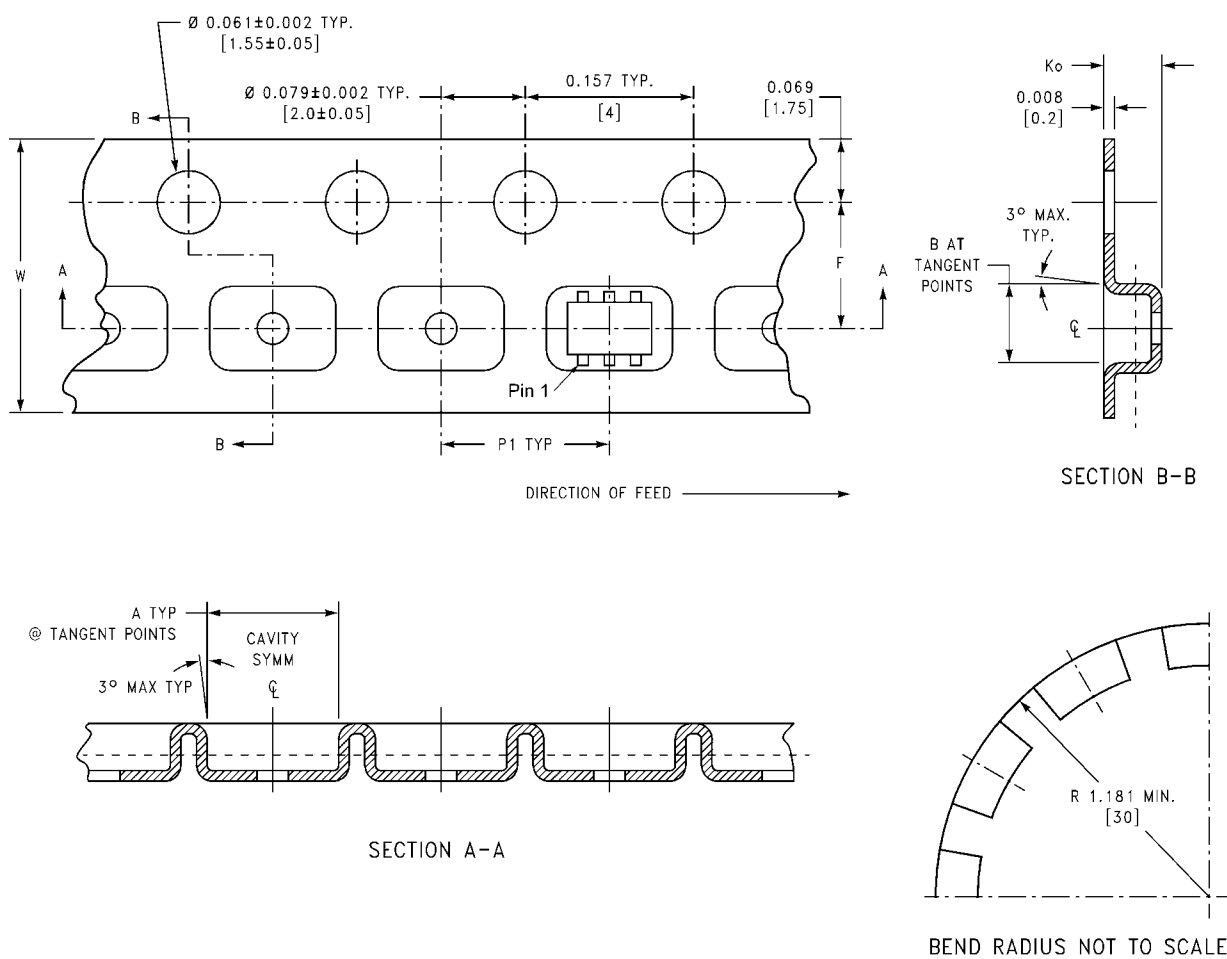
Figure 15. Bandwidth

Tape and Reel Specification

Tape Format for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions inches (millimeters)

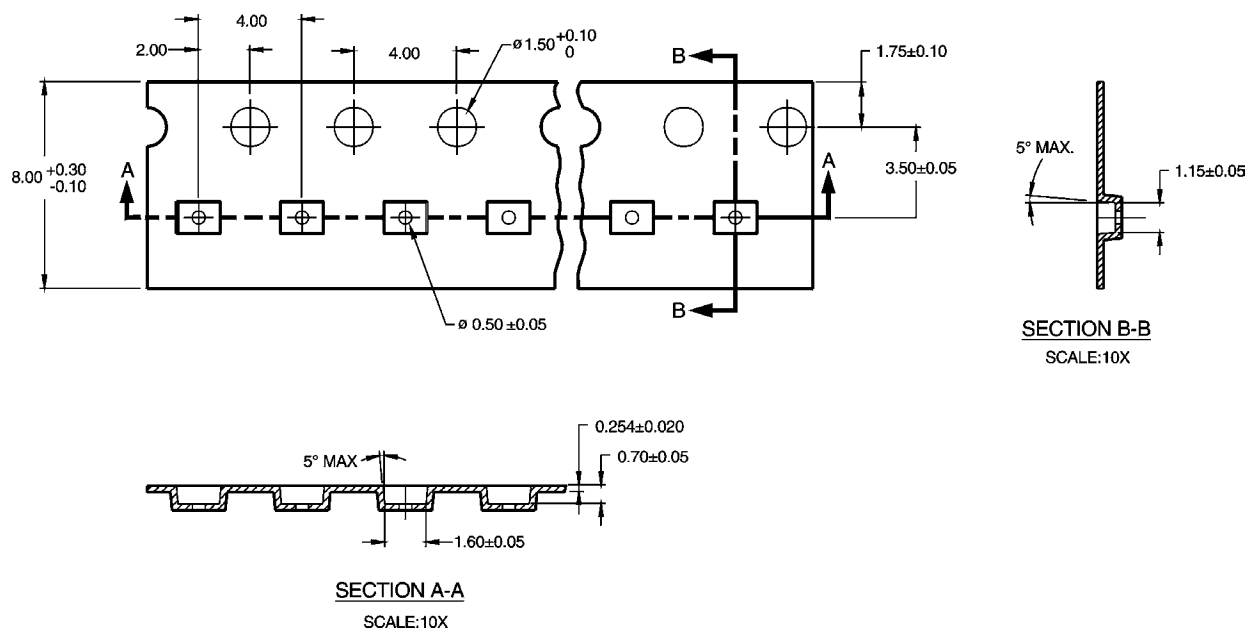


Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

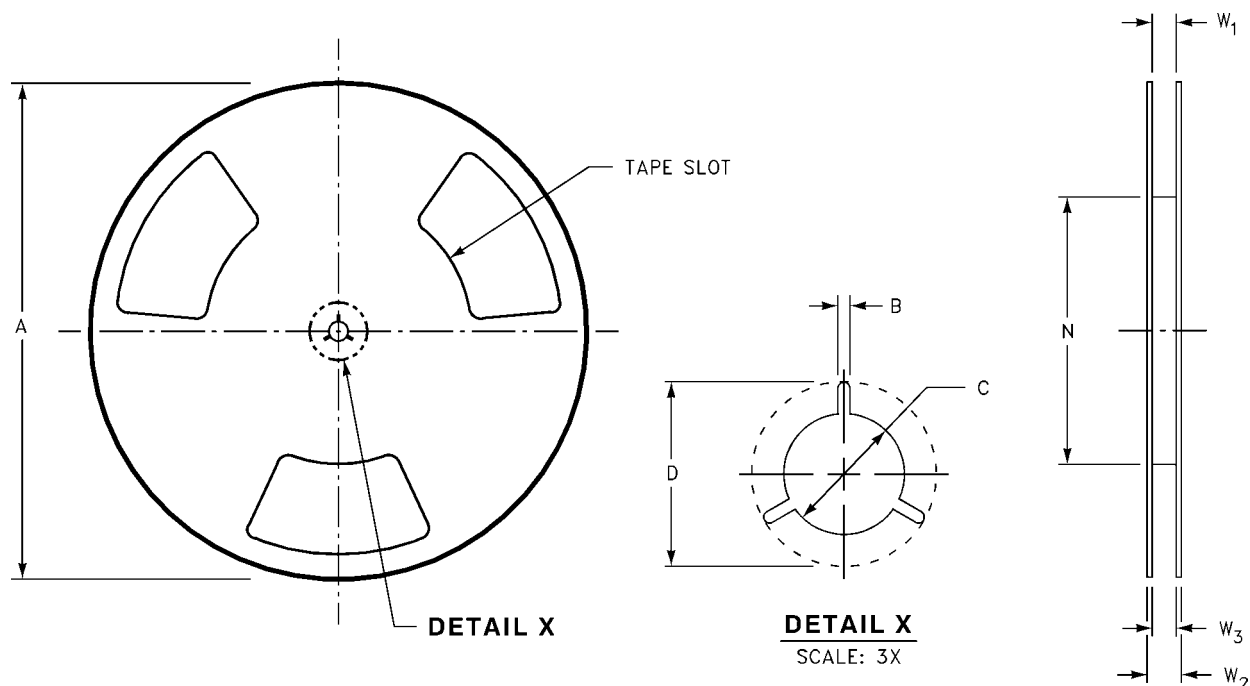
Tape Format for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions inches (millimeters)

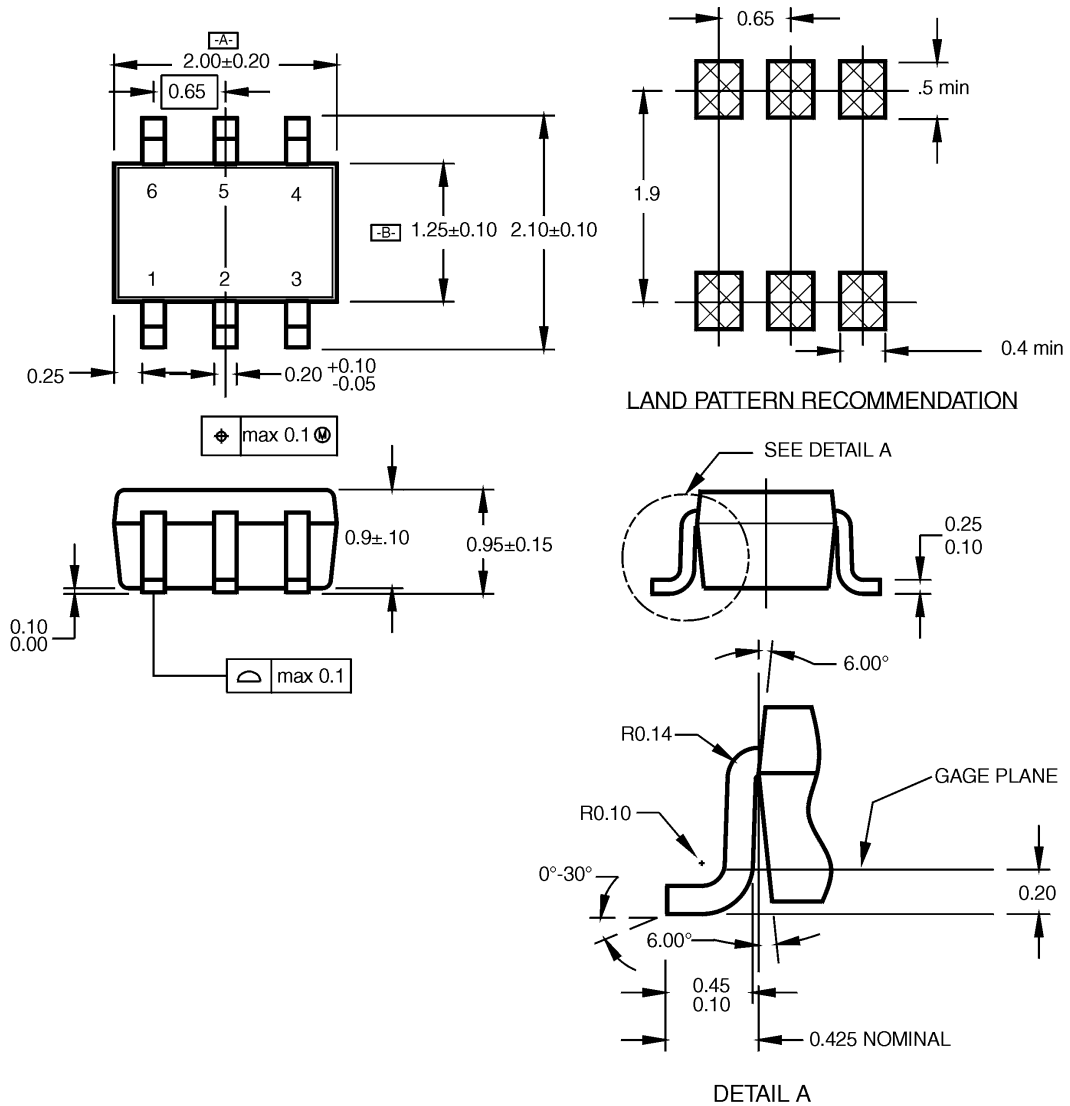


Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted

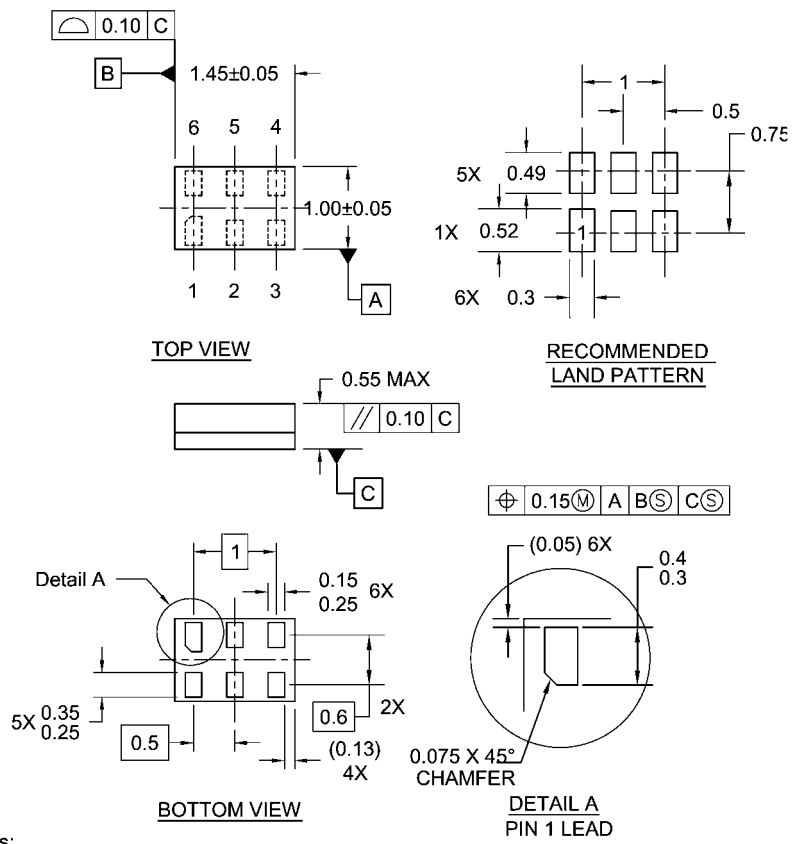


NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

**6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A**



- Notes:
1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
 2. DIMENSIONS ARE IN MILLIMETERS
 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**Pb-Free 6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerSaver™	SuperSOT™-6
ActiveArray™	FASTr™	LittleFET™	PowerTrench®	SuperSOT™-8
Bottomless™	FPS™	MICROCOUPLER™	QFET®	SyncFET™
Build it Now™	FRFET™	MicroFET™	QS™	TCM™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOMET™	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I ² C™	MSXPro™	RapidConnect™	UHC™
E ² CMOS™	i-Lo™	OCX™	μSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
The Power Franchise®		POP™	Stealth™	
Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. 118