

Features

- **Very Fast Settling Current** 75ns (Max) Output
- **Minimal Nonlinearity Error @ 25°C:**
HI-5618A $\pm 1/4$ LSB Max
HI-5618B $\pm 1/2$ LSB Max
- **Low Power Operation** 330mW Typ
- **On-Chip Resistors for Gain and Bipolar Offset**
- **Guaranteed Monotonic Over Temperature**
- **CMOS, TTL, or DTL Compatible**

Applications

- **High Speed Process Control**
- **CRT Display Generation**
- **High Speed A/D Conversion**
- **Waveform Synthesis**
- **High Reliability Applications**
- **Video Signal Reconstruction**

Description

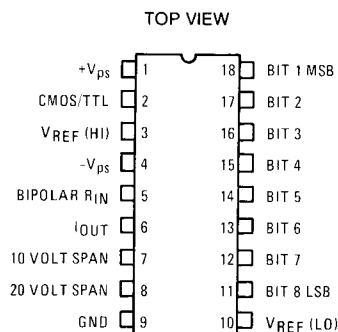
The HI-5618A/B are very high speed 8-bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 75ns (max) to $\pm 1/2$ LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy. For example, the HI-5618A has $\pm 1/4$ LSB maximum nonlinearity error at +25°C, with $\pm 3/8$ LSB guaranteed over the full operating temperature range.

The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

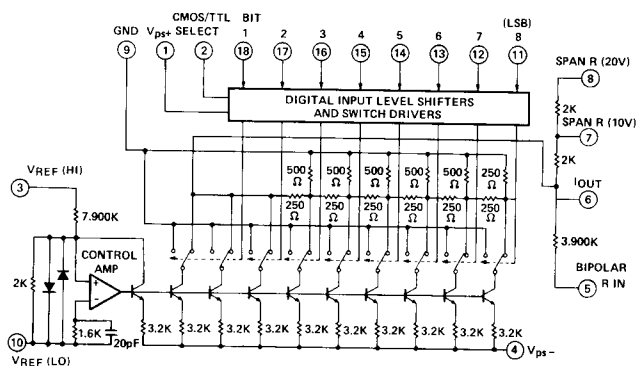
The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. The HI-5618A/B is offered in both commercial and military grades. For additional Hi-Rel screening, including 160 hour burn-in, specify the "-8" suffix.

Power requirements are +5V and -15V. The HI-5618A/B is packaged in an 18 pin Ceramic DIP.

Pinout



Functional Diagram



Absolute Maximum Ratings

(Referred to Ground) (1)

Power Supply Inputs	Vps+ +20V	Junction Temperature 175°C
	Vps- -20V	
Reference Inputs	VREF (Hi) ±16.5V	Operating Temperature Range
	VREF (Lo) 0V	HI-5618A/B-2 -55°C to +125°C
		HI-5618A/B-5 0°C to +75°C
Digital Inputs	Bits 1-12 (TTL) . . . -1V, +7.5V	HI-5618A/B-8 -55°C to +125°C
	Bits 1-12 (CMOS) . . -1V, Vps+	
	CMOS/TTL Logic Sel -1V, +16.5V	Storage Temperature Range -65°C to +150°C
Outputs	Pins 5, 7, 8 ±Vps	
	Pin 6 +Vps, -2.5V	

Electrical Specifications

(Vps+ = +5V; Vps- = -15V; VREF = +10V; Pin 2 to GND, unless otherwise specified.)

PARAMETER	TEMP	HI-5618A/B-2 HI-5618A/B-8			HI-5618A/B-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	

INPUT CHARACTERISTICS

Digital Inputs (2)								
TTL Logic Input Voltage (3)	Logic "1"	Full	2.0		2.0			V
	Logic "0"	Full		0.8		0.8		V
TTL Logic Input Current	Logic "1"	Full		500		500		nA
	Logic "0"	Full		-100		-100		μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	0.7Vps+		0.7Vps+			V
	Logic "0"	Full		0.3Vps+		0.3Vps+		V
CMOS Logic Input Current	Logic "1"	Full		500		500		nA
	Logic "0"	Full		-100		-100		μA
Reference Input								
Input Resistance		+25°C	8K			8K		Ω
Input Voltage (IOUT = 5mA ± 20%)		+25°C	+10			+10		V

TRANSFER CHARACTERISTICS

Resolution		Full		8		8		Bits
Nonlinearity, Integral and Differential	HI-5618A	25°C		± 1/4		± 1/4		LSB
		Full		± 3/8		± 3/8		LSB
	HI-5618B	25°C		± 1/2		± 1/2		LSB
		Full		± 5/8		± 5/8		LSB
Initial Accuracy (6)								
(Relative to External +10V Reference)								
Gain		25°C		± 2		± 2		LSB
Unipolar Zero		25°C		± 1/8		± 1/8		LSB
Bipolar Offset (Neg. Full Scale)		25°C		± 2		± 2		LSB
Temperature Stability								
Gain Drift		Full		± 1/4		± 1/4		LSB
Unipolar Zero Drift		Full		± 1/16		± 1/16		LSB
Bipolar Zero Drift		Full		± 1/4		± 1/4		LSB
Settling Time (5) to 1/2 LSB								
High Impedance (11)	(from all 0's to all 1's)	+25°C	65	75	65	75		ns
	or (from all 1's to all 0's)							

PARAMETER	TEMP	HI-5618A/B-2 HI-5618A/B-8			HI-5618A/B-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	

TRANSFER CHARACTERISTICS (Continued)

Glitch (5) - Major Carry Transition								
Duration	+25°C		20			20		ns
Amplitude (See Fig. 4)	+25°C		350			350		mV
Area	+25°C		3500			3500		mV-ns
Power Supply Sensitivity (5)								
$V_{PS+} = +5V$, $V_{PS-} = -13.5V$ to $-16.5V$								
Gain (Input Code 11...1)	+25°C			± 5			± 5	ppm of FSR/% V_{PS} (9)
Unipolar Zero (Input Code 00...0)	+25°C		± 0.5			± 0.5		
Bipolar Offset (Input Code 00...0)	+25°C		± 1.5			± 1.5		
$V_{PS-} = -15V$, $V_{PS+} = 4.5V$ to $5.5V$								
Gain (Input Code 11...1)	+25°C			± 5			± 5	
Unipolar Zero (Input Code 00...0)	+25°C		± 0.5			± 0.5		
Bipolar Offset (Input Code 00...0)	+25°C		± 1.5			± 1.5		

OUTPUT CHARACTERISTICS

Output Current	Unipolar	+25°C	-4	-5	-6	-4	-5	-6	mA
	Bipolar	+25°C	± 2.0	± 2.5	± 3.0	± 2.0	± 2.5	± 3.0	mA
Output Resistance		+25°C		500			500		Ω
Output Capacitance		+25°C		20			20		pF
Output Voltage Range (7)	Unipolar	+25°C		+10			+10		V
		+25°C		+5			+5		V
	Bipolar	+25°C		± 10			± 10		V
		+25°C		± 5			± 5		V
		+25°C		± 2.5			± 2.5		V
Output Compliance Voltage (5)		+25°C		± 1.5			± 1.5		V
Output Noise Voltage (8)	0.1Hz to 100Hz	+25°C		30			30		μV_{p-p}
	0.1Hz to 1MHz	+25°C		100			100		μV_{p-p}

POWER REQUIREMENTS (4)

V_{PS+}	Full	4.5	5	16.5	4.5	5	16.5	V
V_{PS-}	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
I_{PS+} (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)	+25°C Full		9	12		9	12	mA mA
I_{PS-} (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)	+25°C Full		19	26		19	26	mA mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The V_{PS+} tolerance is $\pm 10\%$ for HI-5618A/B-2, -8; and $\pm 5\%$ for HI-5618A/B-5.
4. For CMOS compatibility based on $V_{PS+} \geq 9.5V$, (switching thresholds equal $V_{PS+}/2$), connect pins 1 and 2. For CMOS levels below 9.5V, connect pin 2 to ground only (this provides a threshold of approximately $\pm 1.4V$).
5. See definitions.
6. These errors may be adjusted to zero using external potentiometers R_1 , R_2 , R_3 . R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100Ω $\pm 1\%$ resistors, in place of R_1 and R_2 .
7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.
8. Specified for all "1's" or all "0's" digital input.
9. FSR is "Full Scale Range", i.e., 20V for $\pm 10V$ range; 10V for $\pm 5V$ range, etc. Nominal full scale output current is 5mA.
10. After 30 seconds warm-up.
11. See Test Circuit, Figure 3.
12. See Test Circuit, Figure 4.

Operating Instructions

The HI-5618A/B accepts an 8 bit digital word in Straight Binary code. In the bipolar mode this code becomes Offset Binary. Also in bipolar mode, the MSB may be complemented using an external

inverter to obtain 2's complement code. Here are the correct outputs for some key input codes:

UNIPOLAR - STRAIGHT BINARY 0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT
11 1	FS - 1 LSB = 9.96094V
10 0	½FS = 5.00000V
01 1	½FS - 1 LSB = 4.96094V
00 0	Zero = 0.00000V

UNIPOLAR - STRAIGHT BINARY 0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT
11 1	FS - 1 LSB = 4.98047V
10 0	½FS = 2.50000V
01 1	½FS - 1 LSB = 2.48047V
00 0	Zero = 0.00000V

BIPOLAR - OFFSET BINARY ± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT
11 1	+FS - 1 LSB = +9.92188V
10 0	Zero = +0.00000V
01 1	Zero - 1 LSB = -0.07813V
00 0	-FS = -10.0000V

BIPOLAR - TWO'S COMPLEMENT ** ± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT
01 1	+FS - 1 LSB = +9.92188V
00 0	Zero = +0.00000V
11 1	Zero - 1 LSB = -0.07813V
10 0	-FS = -10.0000V

** Invert MSB with external inverter to obtain two's complement coding.

Output Accuracy of the HI-5618A/B is affected directly by the reference voltage, since $I_0(F/S) \approx 4 (V_{REF}/8k\Omega)$. For precision performance, a stable +10V reference with low temperature coefficient is recommended.

The output current may be converted to voltage using an external op amp with the internal span and offset resistors, as shown above in the table. The op amp should have good front end temperature coefficients. For example, the HA-2600/2605 is well suited to this application, with offset voltage and offset current tempco's of

5 μ V/°C and 1nA/°C, respectively. The input reference resistor (7.9k Ω) and bipolar offset resistor (3.9k Ω) are both intentionally set low by 100 Ω to allow the user to externally trim out initial errors to a high degree of precision.

For high speed voltage output applications where fast settling is required, the HA-2510/25 is recommended for settling times better than 250ns to 1/2 LSB. The HA-5190/95 is recommended for applications requiring settling times less than 150ns. (See Applications).

CALIBRATION (See Figure 2)

UNIPOLAR MODE -

1. Apply zero (all 0's) input, and adjust R₃ for 0V output.
2. Apply full scale (all 1's) input, and adjust R₁ for:
+9.96094 Volts, +10 Volt range
+4.98047 Volts, +5 Volt range

BIPOLAR MODE -

1. Apply negative full scale (also called bipolar offset): All 0's for offset binary; 1000 for 2's complement. Adjust R₂ for output voltages as follows:
-10 Volts, ±10 Volt Range

-5 Volts, ± 5 Volt Range
-2.5 Volts, ±2.5 Volt Range

2. Apply positive full scale (all 1's for offset Binary; 0111. for 2's complement) Adjust R₁ for output voltages as follows:
+9.92188 Volts, ± 10 Volt Range
+4.96094 Volts, ±5 Volt Range
+2.48047 Volts, ±2.5 Volt Range

3. Apply zero input (1000. for offset Binary; 0000. for 2's complement). Output should be zero volts. Any error is due to nonlinearity in the DAC, and cannot be nulled without disrupting the calibration in steps 2 and 3.

Test Circuits

SETTLING TIME

Turn-off settling time ($T_{S(OFF)}$) is somewhat longer than $T_{S(ON)}$ for the HI-5618. Typical $T_{S(OFF)}$ performance is shown in Figure 3C, using the circuit of Figure 3A.

Refer to Figure 3B; Settling time following turn-off equals T_X plus T_D . The comparator delay T_D may be measured at 1mV/cm, using a Tektronix 7A13 differential comparator or equivalent. Then, T_X is easily measured in a short procedure:

- Adjust delay on generator # 2 for T_X approximately $1\mu s$
- Switch the LSB to +5V (ON).

- Adjust the V_{LSB} supply for 50 percent triggering at COMP. OUT (equal brightness).
- DVM reads -1 LSB. Adjust V_{LSB} supply so DVM reads -1/2 LSB.
- Switch the LSB to P (pulse); COMP. OUT pulse disappears.
- Reduce generator #2 delay until COMP. OUT pulse reappears; adjust delay for "equal brightness".
- Measure T_X from scope. (Any overshoot will be less than 1/2 LSB, so it is not necessary to examine the other side of the envelope, i.e. final value plus 1/2 LSB.)

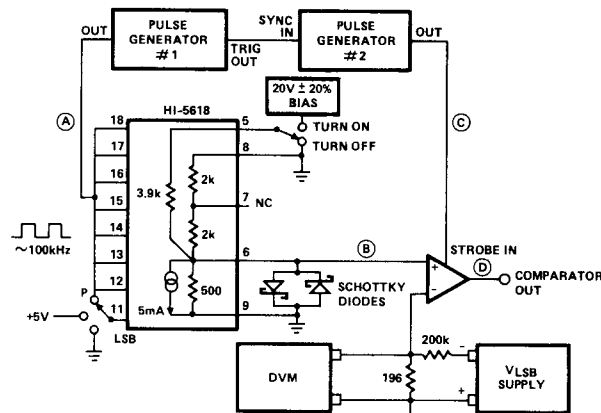


FIGURE 3A

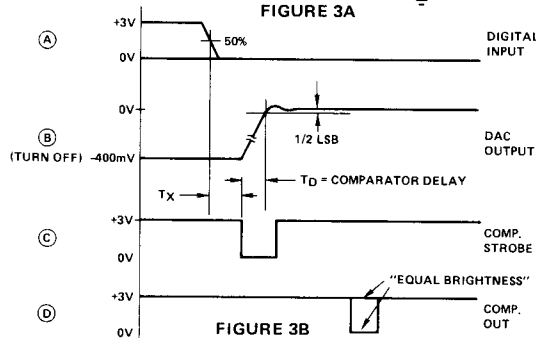


FIGURE 3B

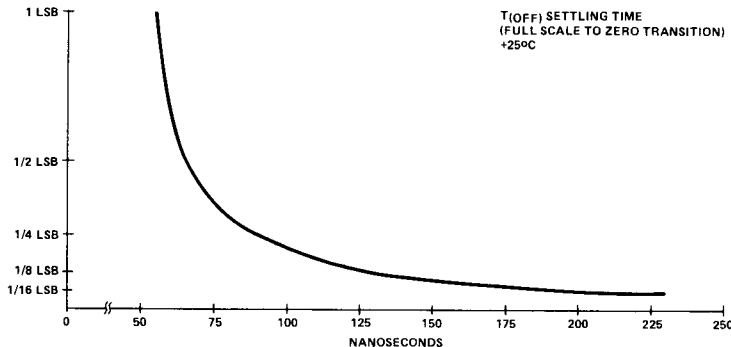
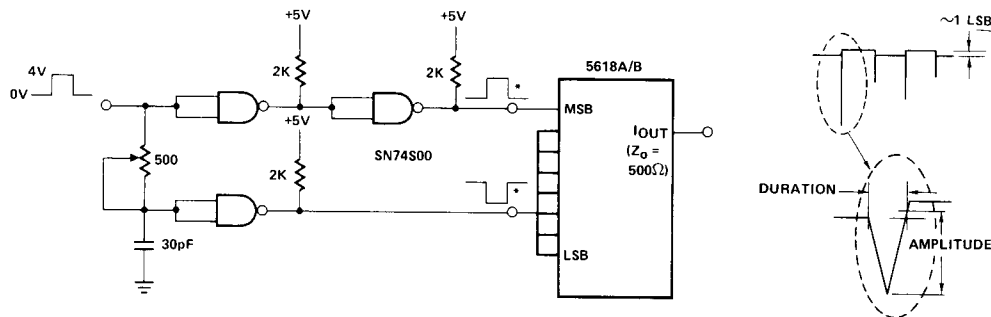


FIGURE 3C

Test Circuits

OUTPUT GLITCH MEASUREMENT

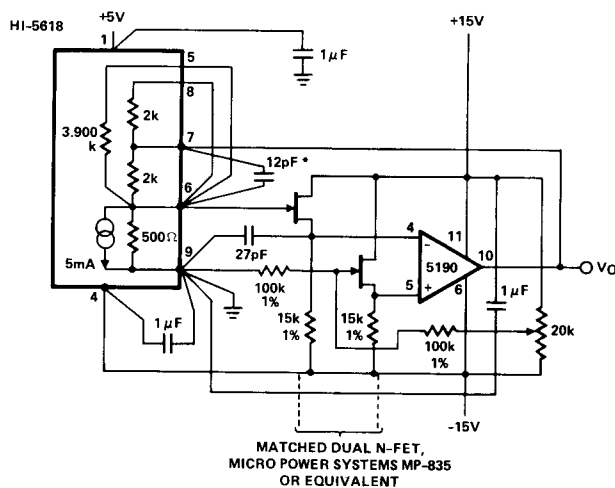


* ADJUST 500Ω TRIMMER SO THAT INPUT SIGNALS CROSS THEIR RESPECTIVE SWITCHING THRESHOLDS AT THE SAME TIME.

FIGURE 4

Applications

HIGH SPEED VOLTAGE OUTPUT



* NOMINAL VALUE, SELECTED FOR OPTIMUM STEP RESPONSE.

Die Characteristics

Transistor Count	122
Die Size:	103 x 209 mils
Thermal Constants; θ_{ja}	75°C/W
θ_{jc}	17°C/W
Tie Substrate to:	Ground (V_{REF} Lo)
Process:	Bipolar - DI

HARRIS SEMICONDUCTOR

Package Configuration

A

B

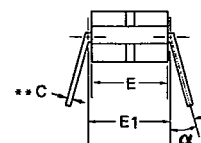
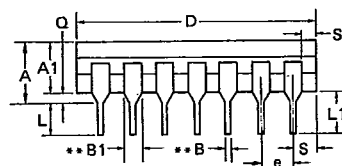
C

D

E

.300 CERAMIC DUAL-IN-LINE

T-90-20



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 SSI	—	.140 .200	.016 .023	.050 .065	.008 .015	.375 .395	.245 .265	.290 .310	.100 BSC	.125 .150	.150 —	— .055	.005 —	.015 .060	0° 15°
B1	14 MSI	—	.140 .170	.016 .023	.050 .065	.008 .015	.753 .785	.265 .285	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
B2	14 LSI	—	.140 .170	.016 .023	.050 .065	.008 .015	.753 .785	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
C1	16* MSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.753 .785	.265 .285	.290 .310	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
C2	16* LSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.753 .785	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
D	18 LSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.882 .915	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
E	20 LSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.940 .970	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°

* End leads are half leads where B remains the same and B1 is 0.035
 ** Solder dip finish add +0.003 inches 0.045

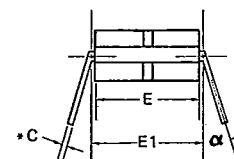
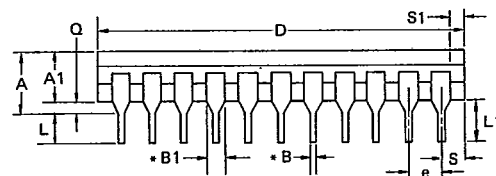
F

.400 CERAMIC DUAL-IN-LINE

G

H

.600 CERAMIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 LSI	—	.150 .225	.016 .023	.050 .065	.008 .015	1.055 1.085	.375 .395	.395 .415	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
G .600	24 LSI	—	.150 .225	.016 .023	.050 .065	.008 .015	1.24 1.27	.515 .535	.595 .615	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
H .600	26 LSI	—	.160 .225	.016 .023	.050 .065	.008 .015	1.44 1.47	.515 .535	.595 .615	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°

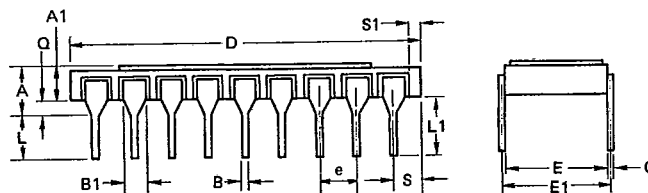
* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

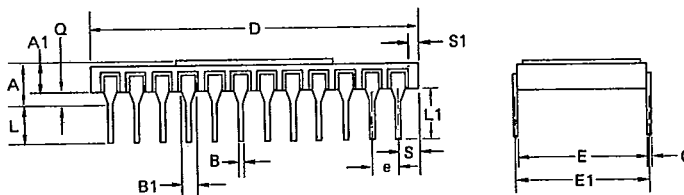
BSC means basic spacing between centerlines.

Package Configuration

T-90-20

I .300 SIDEBRAZE DUAL-IN-LINE

PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	— .200	.080 .110	.016 .023	.045 .060	.008 .015	.890 .910	.280 .300	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.025 .045

J K L .600 SIDEBRAZE DUAL-IN-LINE

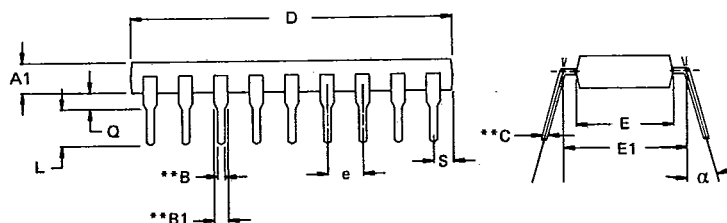
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.185 1.215	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060
K	28	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.385 1.415	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.030 .060
L	40	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.980 2.020	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060

NOTE: Dimensions are $\frac{\text{Min.}}{\text{Max}}$. Dimensions in inches.

BSC means basic spacing between centerlines.

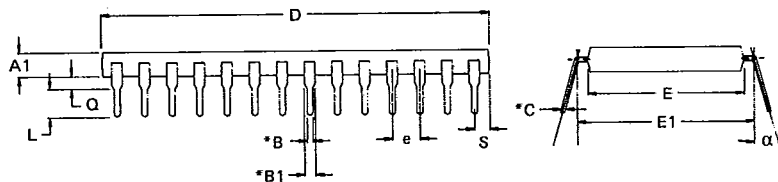
Package Configuration

T-90-20

M N O P Q .300 PLASTIC DUAL-IN-LINE

PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125 .140	.016 .023	.050 .070	.008 .015	.370 .390	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
N	14	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
O	16*	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.025 .035	.020 .040	0° 15°
P	18	.125 .140	.016 .023	.050 .070	.008 .015	.900 .920	.245 .265	.290 .310	.090 .110	.110 .150	.040 .060	.020 .040	0° 15°
Q	20	.130 .145	.016 .023	.050 .070	.008 .015	1.030 1.050	.250 .270	.290 .310	.090 .110	.110 .150	.060 .080	.020 .040	0° 15°

* End leads are half leads where B remains the same and B1 is 0.035
 ** Solder dip finish add 0.003 inches. 0.045

R S .600 PLASTIC DUAL-IN-LINE

PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24	.145 .155	.016 .023	.050 .070	.008 .015	1.24 1.26	.540 .560	.590 .610	.090 .110	.110 .150	.045 .095	.020 .040	0° 15°
S	28	.145 .155	.016 .023	.050 .070	.008 .015	1.54 1.57	.540 .560	.590 .610	.090 .110	.110 .150	.110 .160	.020 .040	0° 15°

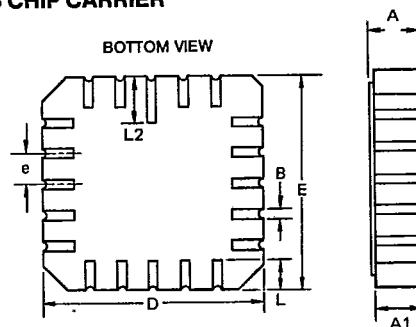
* Solder dip finish add 0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

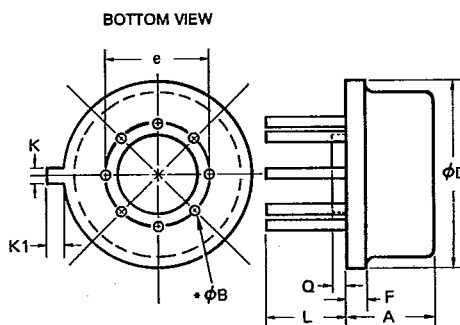
Package Configuration

T-90-20

T .350 CERAMIC LEADLESS CHIP CARRIER***U** .450 CERAMIC LEADLESS CHIP CARRIER***V** .650 CERAMIC LEADLESS CHIP CARRIER*

PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 .350 SQ	.073 .089	.063 .077	.022 .028	.342 .358	.342 .358	.050 BSC	.045 .055	.075 .095
U	28 .450 SQ	.074 .088	.064 .076	.022 .028	.442 .458	.442 .458	.050 BSC	.045 .055	.075 .095
V	44 .650 SQ	.073 .089	.063 .077	.022 .028	.643 .662	.643 .662	.050 BSC	.045 .055	.075 .095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN**X** TO-100 METAL CAN

PKG. CODE	LEAD COUNT	DIM. A	DIM. φB	DIM. φD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	.165 .185	.016 .018	.345 .365	.190 .210	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040
X	10 TO-100	.165 .185	.016 .018	.345 .365	.220 .240	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040

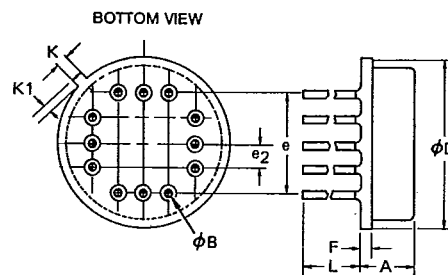
* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

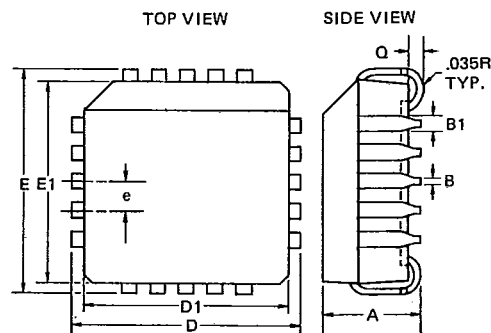
BSC means basic spacing between centerlines.

Package Configuration

T-90-20

Y TO-8 METAL CAN

PKG. CODE	LEAD COUNT	DIM. A	DIM. phi B	DIM. phi D	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130 .150	.016 .021	.585 .615	.400 BSC	.100 BSC	.020 .040	.027 .034	.027 .045	.500 .550

AA AB AC PLASTIC LEADED CHIP CARRIER

PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165 .180	.013 .021	.026 .032	.385 .395	.350 .356	.050 BSC	.020 —
AB	28	.165 .180	.013 .021	.026 .032	.485 .495	.450 .456	.050 BSC	.020 —
AC	44	.165 .180	.013 .021	.026 .032	.685 .695	.650 .656	.050 BSC	.020 —

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.