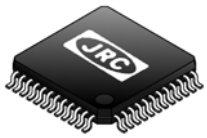
Dolby Virtual Speaker / Dolby Headphone Decoder

■ General Description

The NJU26220 simulates a highly realistic 5.1-speaker surround sound listening environment from as few as two speakers or headphone by Dolby Virtual Speaker/Dolby Headphone technology.
The NJU26220 processes the Dolby Virtual Speaker and Dolby Headphone technology that combined with Pro Logic II processing. It includes Pro Logic II decoder. Moreover, multi-channel signal inputs from an external decoder are possible.
It is suitable for digital TVs, stereo mini-components, PCs, and any audio/visual products.

■Package



NJU26220FN2

■ FEATURES

- Dolby Virtual Speaker
- Dolby Headphone
- Dolby Pro Logic II (Max 5.1ch Output)
- Multi-channel signals input (Max 5.1ch Input)
- Monitor output
- Lip-Sync Delay function (Digital Audio Delay)

■ Digital Signal Processor Specification

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 4 Output ports
- Microcomputer Interface : I^2C Bus (Standard-mode/100kbps, Fast-mode/400kbps)
  : 4-Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Power Supply : DSP Core : 1.8V
  : I/O interface: 3.3V(+5.0V Input tolerant)
- Package : QFP48-N2 (Pb-Free)

■ DSP Block Diagram

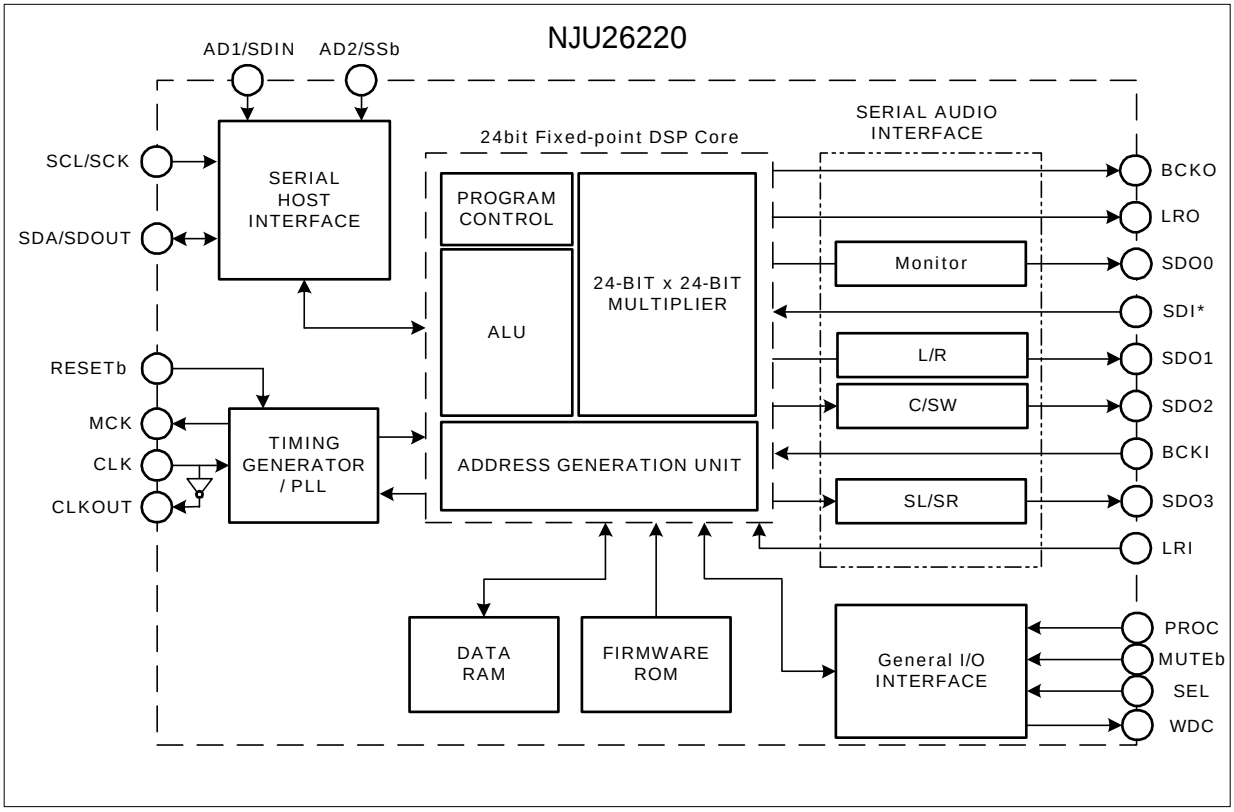


Fig.1 NJU26220 Block Diagram

■ Function Diagram

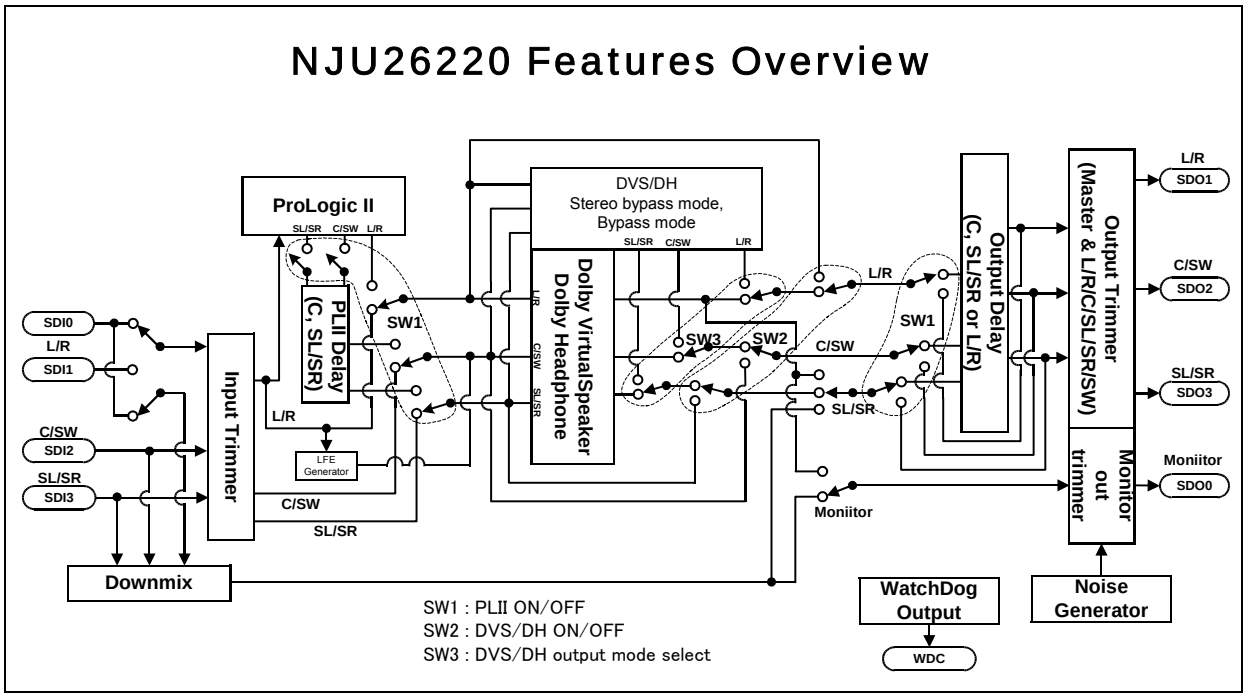


Fig.2 NJU26220 Function Diagram

■ Pin Configuration

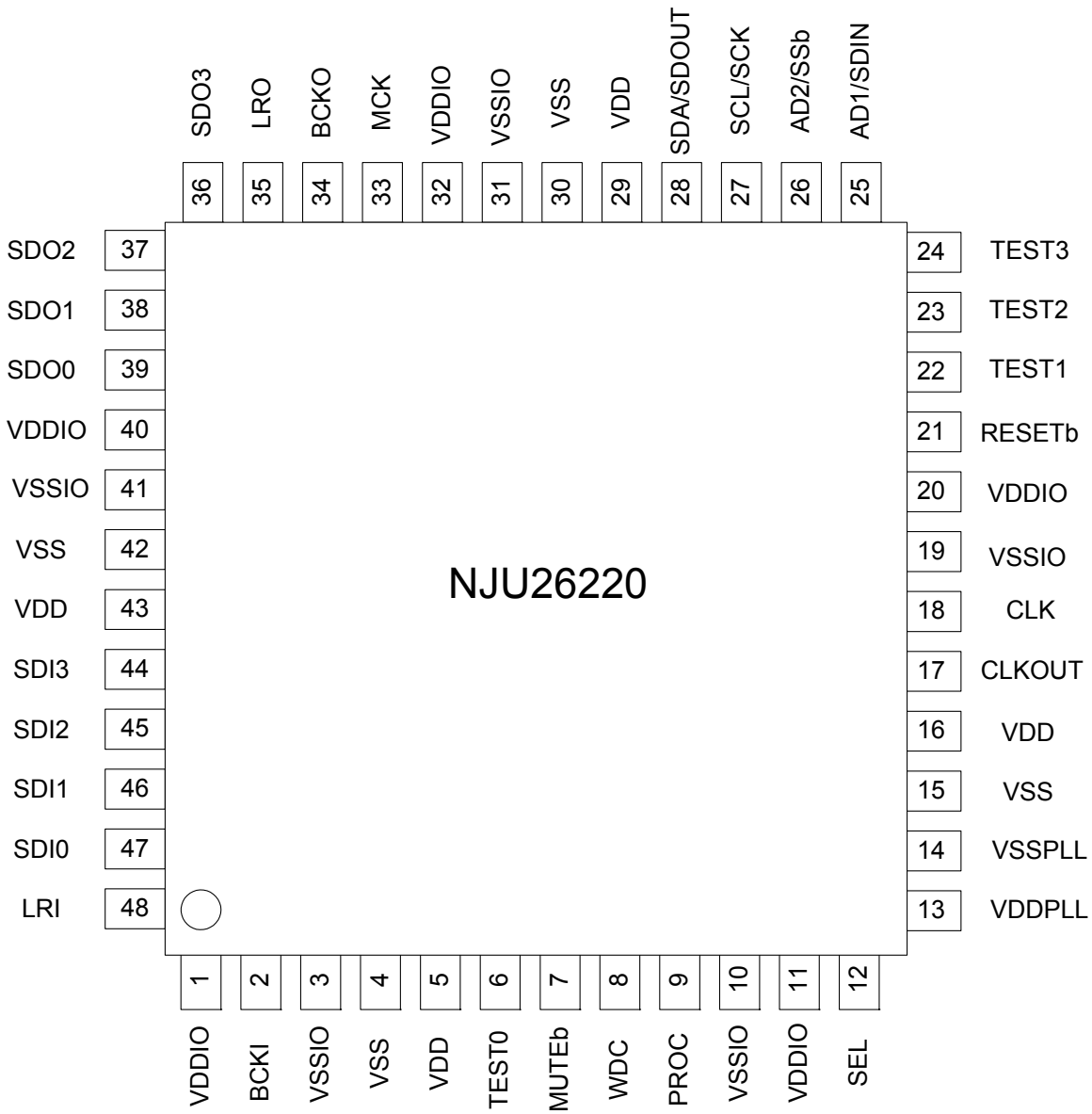


Fig.3 Pin Configuration

■ Pin Description

Table1 Pin Description

Pin No.	Symbol	I/O	Function
1	VDDIO	P	I/O Power Supply +3.3V
2	BCKI	I	Bit Clock Input
3	VSSIO	G	I/O Power Supply GND
4	VSS	G	DSP Core Power Supply GND
5	VDD	P	DSP Core Power Supply +1.8V
6	TEST0	I*	for test (connect with VSSIO through 3.3-ohm resistance.)
7	MUTEb	I*	Master Volume Status after reset '1': 0dB, '0': Mute
8	WDC	OD*	Watchdog Clock output pin (Open-Drain Output)
9	PROC	I*	Signal Processing after reset '1':Normal Processing, '0': Waiting for a Command without Processing
10	VSSIO	G	I/O Power Supply GND
11	VDDIO	P	I/O Power Supply +3.3V
12	SEL	I	Host Interface Selection '1': Serial Interface, '0': I^2C bus
13	VDDPLL	P	PLL Power Supply +1.8V
14	VSSPLL	G	PLL Power Supply GND
15	VSS	G	DSP Core Power Supply GND
16	VDD	P	DSP Core Power Supply +1.8V
17	CLKOUT	O	OSC Clock Output
18	CLK	I	OSC Clock Input (12.288MHz)
19	VSSIO	G	I/O Power Supply GND
20	VDDIO	P	I/O Power Supply +3.3V
21	RESETb	I	Reset (RESETb='0': DSP Reset)
22	TEST1	I	for test (connect to VDDIO)
23	TEST2	I	for test (connect to VSSIO)
24	TEST3	I	for test (connect to VSSIO)
25	AD1/SDIN	I	I^2C Address (I^2C mode) / Serial In (4-wire serial mode)
26	AD2/SSb	I	I^2C Address (I^2C mode) / Serial enable (4-wire serial mode)
27	SCL/SCK	I	I^2C SCL (I^2C mode) / Serial clock (4-wire serial mode)
28	SDA/SDOUT	I/O	I^2C SDA (I^2C mode) / Serial Out (4-wire serial mode)
29	VDD	P	DSP Core Power Supply +1.8V
30	VSS	G	DSP Core Power Supply GND
31	VSSIO	G	I/O Power Supply GND
32	VDDIO	P	I/O Power Supply +3.3V
33	MCK	O	A/D, D/A clock output (buffer output of a CLK pin)
34	BCKO	O	Bit Clock Output
35	LRO	O	LR Clock Output
36	SDO3	O	Audio Data Output ch.3 (Surround channel (LS/RS) output)
37	SDO2	O	Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)
38	SDO1	O	Audio Data Output ch.1 (Front channel (L/R) output)
39	SDO0	O	Audio Data Output ch.0 (Monitor output)
40	VDDIO	P	I/O Power Supply +3.3V
41	VSSIO	G	I/O Power Supply GND
42	VSS	G	DSP Core Power Supply GND
43	VDD	P	DSP Core Power Supply +1.8V
44	SDI3	I	Audio Data Input ch.3
45	SDI2	I	Audio Data Input ch.2
46	SDI1	I	Audio Data Input ch.1
47	SDI0	I	Audio Data Input ch.0
48	LRI	I	LR Clock Input

Note1: I: Input, O: Output, OD: Open-Drain Output, I/O: Bidirectional, P: +Power, G: GND

Note2: I/O with * operate as bidirectional pins when test. Connect with VDDIO or VSSIO through 3.3k-ohm resistance.

1. Audio Interface

The serial audio interface carries audio data to and from the NJU26220. Industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified are supported. Table 2 shows pin description of input pin and output pin of NJU26220.

Table 2 Serial Audio Input/Output Pin Description

Pin No.	Symbol	Description
47	SDI0	Stereo L/R input (Pin select)
46	SDI1	
45	SDI2	C/SW input
44	SDI3	SL/SR input
39	SDO0	Monitor output
38	SDO1	L/R output
37	SDO2	C/SW output
36	SDO3	SL/SR output

L/R: Front channel, C/SW: Center channel and Sub woofer, SL/SR: Surround channel.

The NJU26220 has a pair of bit clock lines (BCKI and BCKO) and a pair of left/right clock lines (LRI and LRO). The clock inputs BCKI and LRI are used to accept timing signals from an external device when the NJU26220 operates in SLAVE mode.

The clock outputs BCKO and LRO are provided for delta-sigma A/D and D/A converters when the NJU26220 operates in MASTER mode. In SLAVE mode, the output of BCKO and LRO are the buffered output of BCKI and LRI.

The MCK always generates the system clock supplied to the NJU26220 expect RESET sequence.

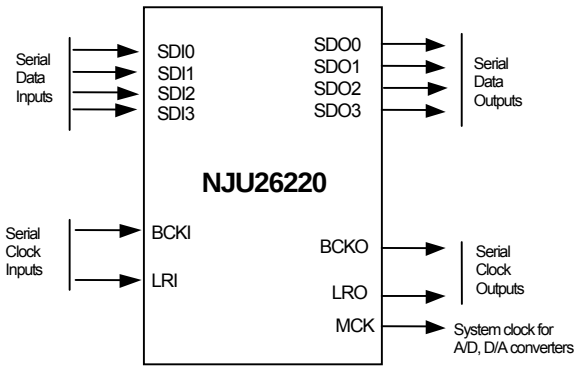


Fig. 4 Serial Audio Interface

2. Host Interface

The NJU26220 can be controlled via Serial Host Interface (SHI) using either of two serial bus format: I^2C bus or 4-Wire serial bus. Data transfers are in 8 bit packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The SEL pin controls the serial bus mode. When the SEL is low during the NJU26220 initialization, I^2C bus is available. When the SEL is high during the NJU26220 initialization, 4-Wire serial bus is available.

Table 3 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C / Serial)	I^2C bus Format	4-Wire Serial bus Format
27	SCL/SCK	Serial Clock	Serial Clock
28	SDA/SDOUT	Serial Data	Serial Data Output
25	AD1/SDIN	I^2C bus address Bit1	Serial Data Input
26	AD2/SSb	I^2C bus address Bit2	SLAVE Select

Note: When I^2C is selected, SDA/SDOUT pin is a bi-directional open drain. SDA/SDOUT pin, which is assigned for I^2C, requires a pull-up resister. When 4-Wire Serial bus is selected, SDA/SDOUT pin is CMOS output.

2.1 I^2C Bus

When the NJU26220 is configured for I^2C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistor. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. This offers additional flexibility in a system design by offering two different possible SLAVE addresses for which the NJU26220 will respond to.

An address can be arbitrarily set up with an internal setup and these AD1/AD2 pins.

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Table 4 I^2C Bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	1	1	1	AD2*1	AD1*1	R/W

*1 SLAVE address is 0 when AD1 is "Low". SLAVE address is 1 when AD1 is "High".

The figure on the following shows the basic timing relationships for transfers. A transfer is initiated with a START condition, followed by the SLAVE address byte. The SLAVE address consists of the seven-bit SLAVE address followed by a read/write (R/W) bit. When an address with an effective serial host interface is detected, the acknowledgement bit which sets a SDA line to "Low" in the ninth bit clock cycle is returned.

The R/W bit in the SLAVE address byte sets the direction of data transmission until a STOP condition terminates the transfer. R/W = “Low” indicates the host will send to the NJU26220 while R/W = “High” indicates the host will receive data from the NJU26220.

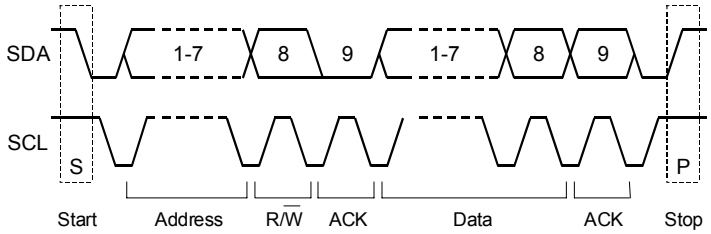

Fig. 5 I^2C Bus Format

The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” I^2C bus data transfer.

2.2 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL=”High” during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb=“Low”. Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. SDOUT is always CMOS output. SDOUT does not require a pull-up resistor.

3. Pin setting

The NJU26220 operates default command setting after resetting the NJU26220. In addition, the NJU26220 restricts operation at power on by setting PROC pin and MUTEb pin. These pins are input pin. However, these pins operate as bi-directional pins when test for internal. Connect with VDDIO or VSSIO through 3.3k-ohm resistance.

Table 5 The function of a functional setting pin

Pin	Setting	Function
PROC	HIGH	The NJU26220 operates default setting after reset.
	LOW	The NJU26220 does not operate after reset. Sending start command is required for starting operation.
MUTEb	HIGH	Master volume is set 0dB after reset.
	LOW	Master volume is set mute after reset.

4 Watchdog Clock

The NJU26220 outputs clock pulse through WDC (Pin No.8) during normal operation. The WDC clock is useful to check the status of the NJU26220 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26220. When the WDC clock pulse is lost or not normal clock cycle, the NJU26220 does not operate correctly. Then reset the NJU26220 and set up the NJU26220 again.

The WDC pin is open drain output. Connect with VDDIO through 3.3k-ohm resistance when WDC is useful. Connect with VSSIO through 3.3k-ohm resistance when WDC is not useful. Do not open WDC pin.

Note: The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing.
In slave mode, when there is no input of BCKI/LRI, WDC can not output.
It is required to set up a sampling rate correctly.

5. NJU26220 Command Table

Host processor can control the NJU26220 via I^2C bus interface or 4-Wire serial bus. The following table summarizes the available user commands.

No.	Command	Command Description
1	SET_TASK_CMD	Decode Mode: Pro Logic II, Dolby Virtual Speaker, Dolby Headphone, Pink Noise Generator, Downmix, Delay select, LFE Generator
2	PRO2MODE_CMD	Mode setting: Pro Logic II (Movie, Music etc.,), Panorama mode
3	PRO2CDCFG_CMD	Dimension setting, Center Width Control
4	PRO2FLAGS_CMD	Mode setting: Auto Balance, 3 stereo, Phantom Center etc.,
5	DVS_DH_CMD	DVS/DH select, DVS output speaker layout, DVS/DH output mode
6	SAMPLERATE_CMD	32.0kHz, 44.1kHz, 48.0kHz
7	PNG_MODE_CMD	Pink Noise Generator output channel configuration
8	DELAY_CMD	Delay time at Center and Surround Channel
9	GAIN_CMD	Each Channel Trimmer
10	SYSTEM_STATE_CMD	Serial audio interface format, Clock, Master/Slave
11	WATCHDOG_CMD	Watchdog Clock interval
12	SMOOTH_CMD	Smooth Control time
13	OUTPUT_SEL_CMD	Output select
14	LFE_CONFIG_CMD	LFE cutoff frequency select
15	REINIT_CMD	Re-initialization command
16	SOFTWARE_RESET_CMD	Software RESET
17	START_CMD	Start Command at Power on
18	NOP_CMD	NOP command

■ License

Ver. 1.01