SIEMENS

1M x 4-Bit Dynamic RAM (Hyper Page Mode (EDO) version)

HYB 314405BJ/BJL-50/-60/-70

Advanced Information

- 1 048 576 words by 4-bit organization
- 0 to 70 ˚C operating temperature
- Hyper Page Mode - EDO
- Performance:

		-50	-60	-70	
t_{RAC}	$\overline{RAS}$ access time	50	60	70	ns
t_{CAC}	$\overline{CAS}$ access time	13	15	20	ns
t_{AA}	Access time from address	25	30	35	ns
t_{RC}	Read/Write cycle time	89	104	124	ns
t_{HPC}	Hyper page mode (EDO) cycle time	20	25	30	ns

- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 252 mW active (-50 version)
  max. 216 mW active (-60 version)
  max. 198 mW active (-70 version)
- Standby power dissipation:
  7.2 mW max. standby (LVTTL)
  3.6 mW max. standby (LVCMOS)
  720 µW max. standby (LVCMOS) for Low Power Version
- Read, write, read-modify write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh and test mode capability
- All inputs and outputs LVTTL compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms for Low Power Version
- Plastic Packages: P-SOJ-26/20-5 with 300 mil width

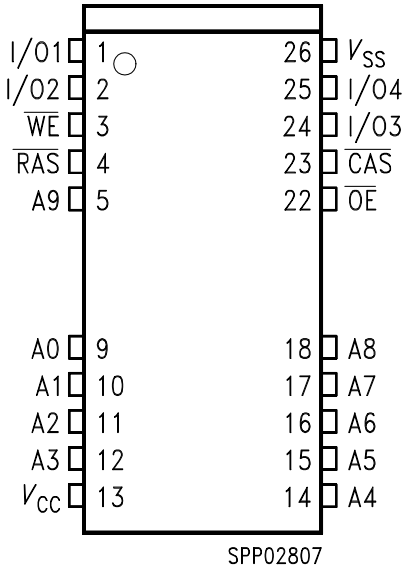
The HYB 314405BJ/BJL is the new generation dynamic RAM organized as 1 048 576 words by 4-bit. The HYB 314405BJ/BJL utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 314405BJ/BJL to be packed in a standard plastic P-SOJ-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 3.3 V (± 0.3 V) power supply, direct interfacing with high performance logic device families.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 314405BJ-50	Q67100-Q2122	P-SOJ-26/20-5	3.3 V EDO-DRAM (access time 50 ns)
HYB 314405BJ-60	Q67100-Q2124	P-SOJ-26/20-5	3.3 V EDO-DRAM (access time 60 ns)
HYB 314405BJ-70	Q67100-Q2126	P-SOJ-26/20-5	3.3 V EDO-DRAM (access time 70 ns)
HYB 314405BJL-50	on request	P-SOJ-26/20-5	3.3 V Low Power EDO-DRAM (access time 50 ns)
HYB 314405BJL-60	on request	P-SOJ-26/20-5	3.3 V Low Power EDO-DRAM (access time 60 ns)
HYB 314405BJL-70	on request	P-SOJ-26/20-5	3.3 V Low Power EDO-DRAM (access time 70 ns)

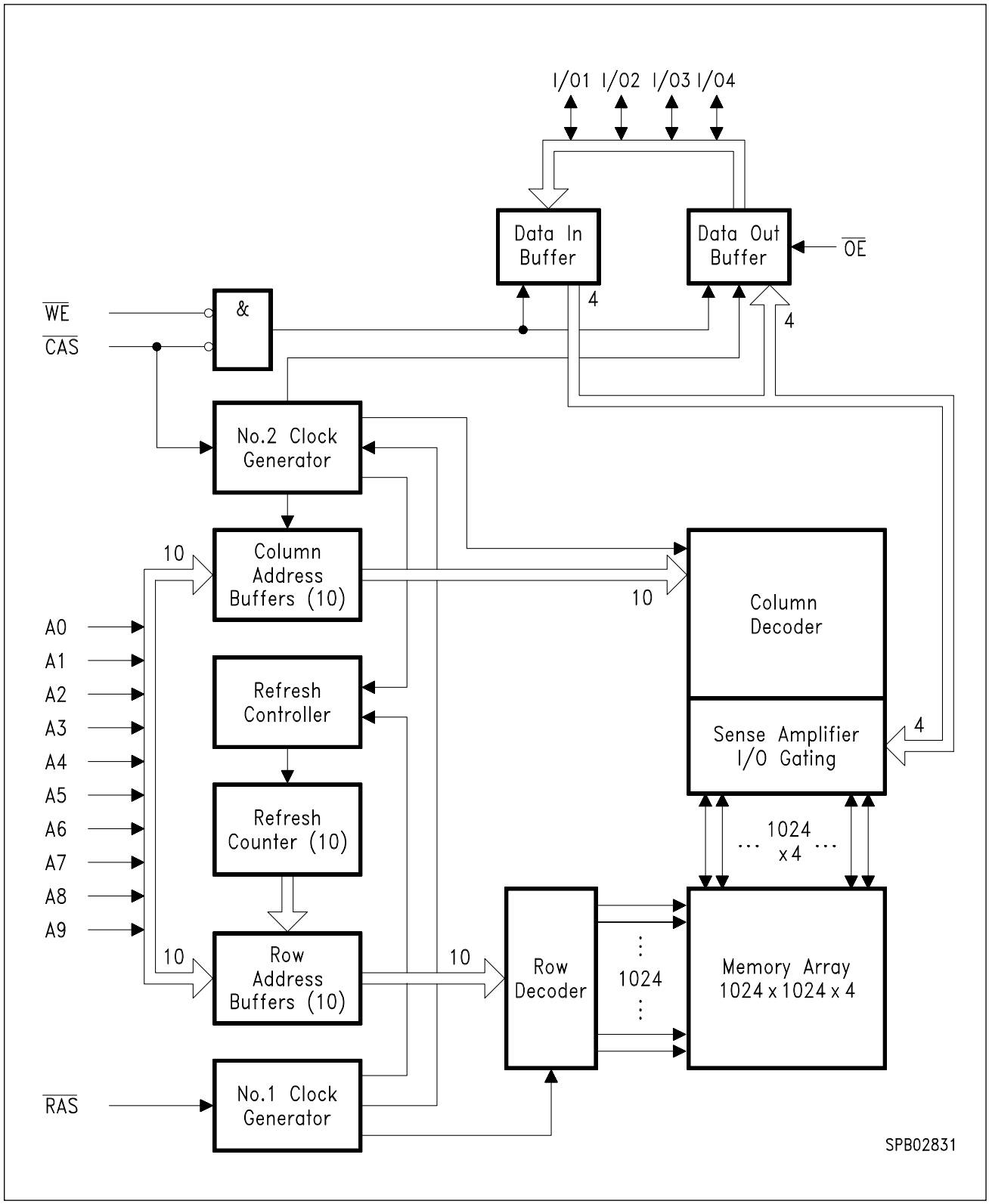
Pin Configuration
(top view)

P-SOJ-26/20-5



Pin Names

A0-A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 - I/O4	Data Input/Output
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	No Connection



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 ˚C
Storage temperature range ..... – 55 to + 150 ˚C
Input/output voltage ..... – 1 to + 4.6 V
Power Supply voltage ..... – 1 to + 4.6 V
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 ˚C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = – 100 µA)	V_{OH}	V_{CC} – 0.2	–	V	
CMOS Output low voltage (I_{OUT} = 100 µA)	V_{OL}	–	0.2	V	
Input leakage current, any input (0 V < V_{in} < V_{CC} + 0.3 V, all other input = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current, any input (DO is disabled, 0 V < V_{OUT} < V_{CC} + 0.3 V)	$I_{I(L)}$	– 10	10	µA	
Average V_{CC} supply current -50 version -60 version -70 version	I_{CC1}	 – – –	 70 60 55	mA	2) 3)4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = VIH)	I_{CC2}	–	2	mA	–
Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles -50 version -60 version -70 version	I_{CC3}	 – – –	 70 60 55	mA	2)4)
Average V_{CC} supply current during hyper page mode (EDO) operation -50 version -60 version -70 version	I_{CC4}	 – – –	 70 60 55	mA	2) 3)4)

DC Characteristics (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1 200	mA µA	1) L-version
Average V_{CC} supply current during $\overline{CAS}$ before $\overline{RAS}$ refresh mode -50 version -60 version -70 version	I_{CC6}	 – – –	 70 60 55	mA	2)4)
For Low Power Version only: Battery backup current (average power supply current in battery backup mode): ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A10 = V_{CC} – 0.2 V or 0.2 V; DI = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min = 1 µs)	I_{CC7}	–	250	µA	–

AC Characteristics 5)6)
T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Common Parameters									
Random read or write cycle time	t_{RC}	89	–	104	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10 k	60	10 k	70	10 k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10 k	10	10 k	12	10 k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	12	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	14	53	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	12	35	ns	

AC Characteristics (cont'd) [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	17	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	7
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
Refresh period for L-version	t_{REF}	–	128	–	128	–	128	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	17	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	–	17	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	17	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	17	ns	12
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	10	–	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	10	–	13	–	15	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	8	–	10	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	10	–	ns	

AC Characteristics (cont'd) [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	17	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	17	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	8	–	10	–	12	–	ns	16
Read-modify-Write Cycle									
Read-write cycle time	t_{RWC}	118	–	138	–	162	–	ns	
$\overline{RAS}$ to WE delay time	t_{RWD}	64	–	77	–	89	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	36	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	54	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	10	–	13	–	15	–	ns	
Hyper Page Mode (EDO) Cycle									
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	27	–	32	–	37	ns	7
Output data hold time	t_{COH}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width in hyper page mode	t_{RAS}	50	200 k	60	200 k	70	200 k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	27	–	32	–	37	–	ns	
Hyper Page Mode (EDO) Read-modify-Write Cycle									
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	58	–	68	–	77	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	41	–	49	–	56	–	ns	

AC Characteristics (cont'd) [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	10	–	ns	
CAS-before-RAS Counter Test Cycle									
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	ns	
Test Mode									
Write command setup time	t_{WTS}	10	–	10	–	10	–	ns	
Write command hold time	t_{WTH}	10	–	10	–	10	–	ns	

Capacitance

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{OE}$)	C_{I2}	–	7	pF
Output capacitance (IO1 to IO4)	C_{IO}	–	7	pF

Notes:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

4) Address can be changed once or less while RAS = V_{IL}. In case of I_{CC4} it can be changed once or less during a hyper page mode (EDO) cycle

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume t_T = 2 ns.

7) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

8) Measured with the specified current load and 100 pF at V_{OL} = 0.8 V and V_{OH} = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA}, t_{CPA} , t_{OEA}, t_{CAC} is measured from tristate.

9) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

10) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

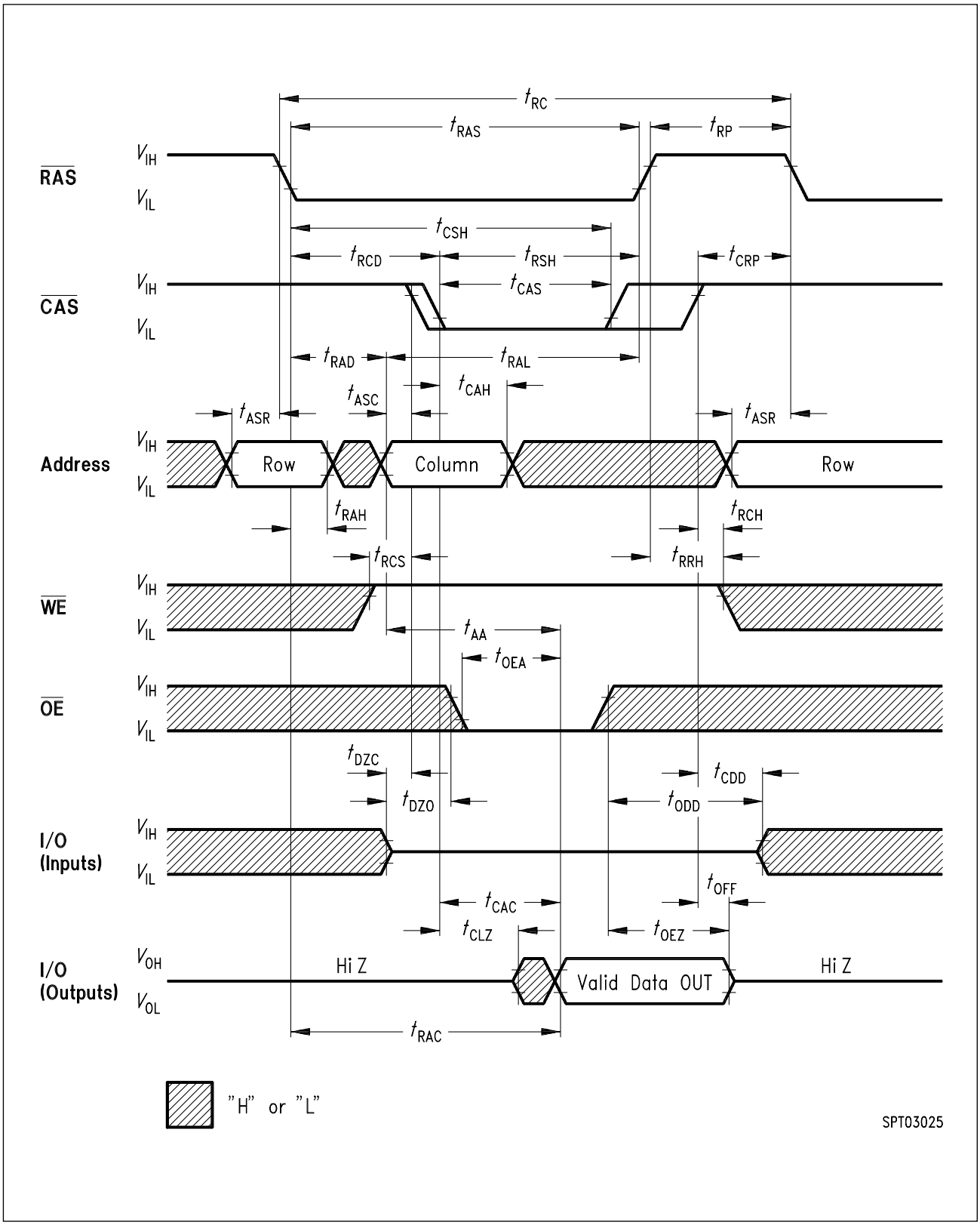
12) $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

13) Either t_{DZC} or t_{DZO} must be satisfied.

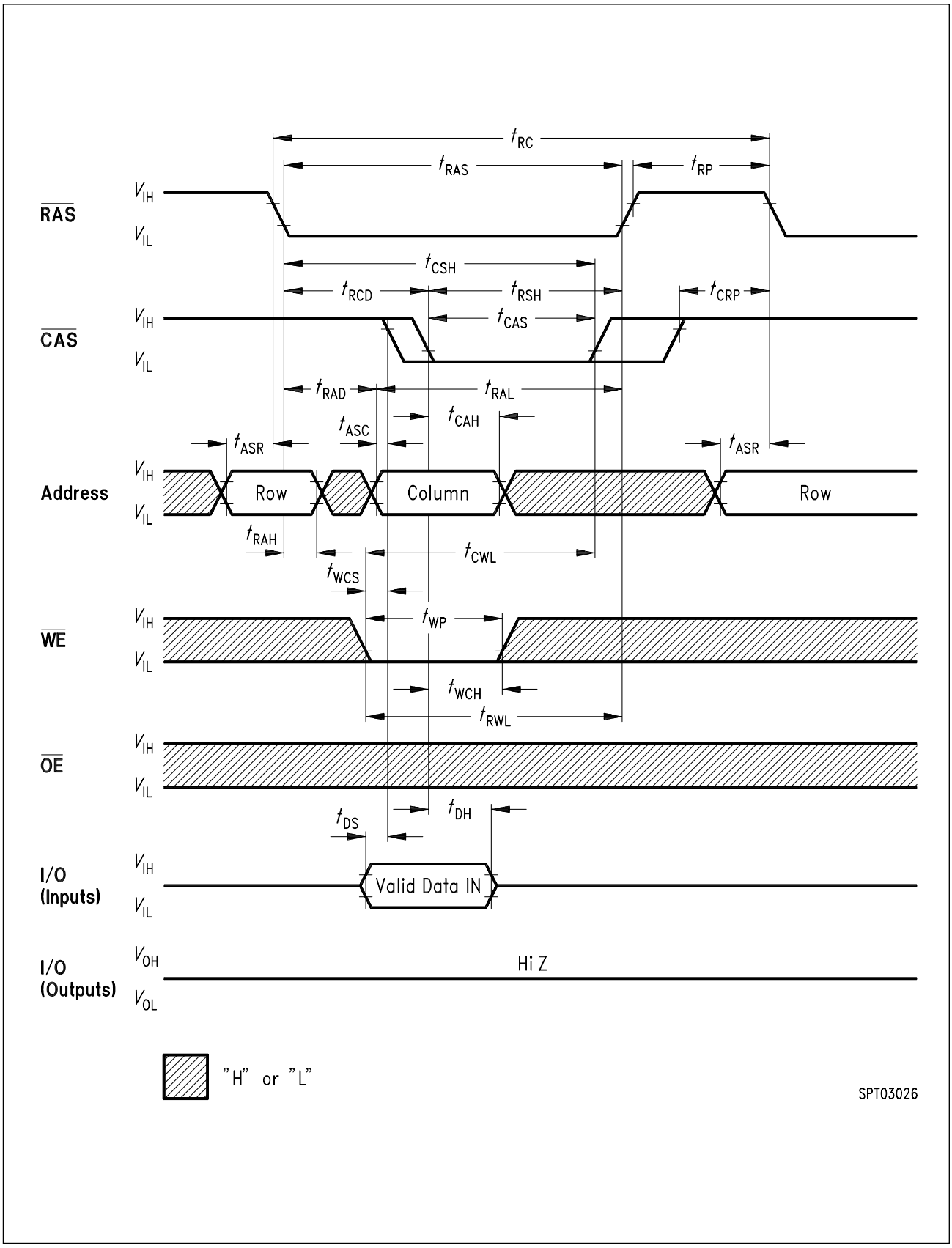
14) Either t_{CDD} or t_{ODD} must be satisfied.

15) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} > t_{AWD\ (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.

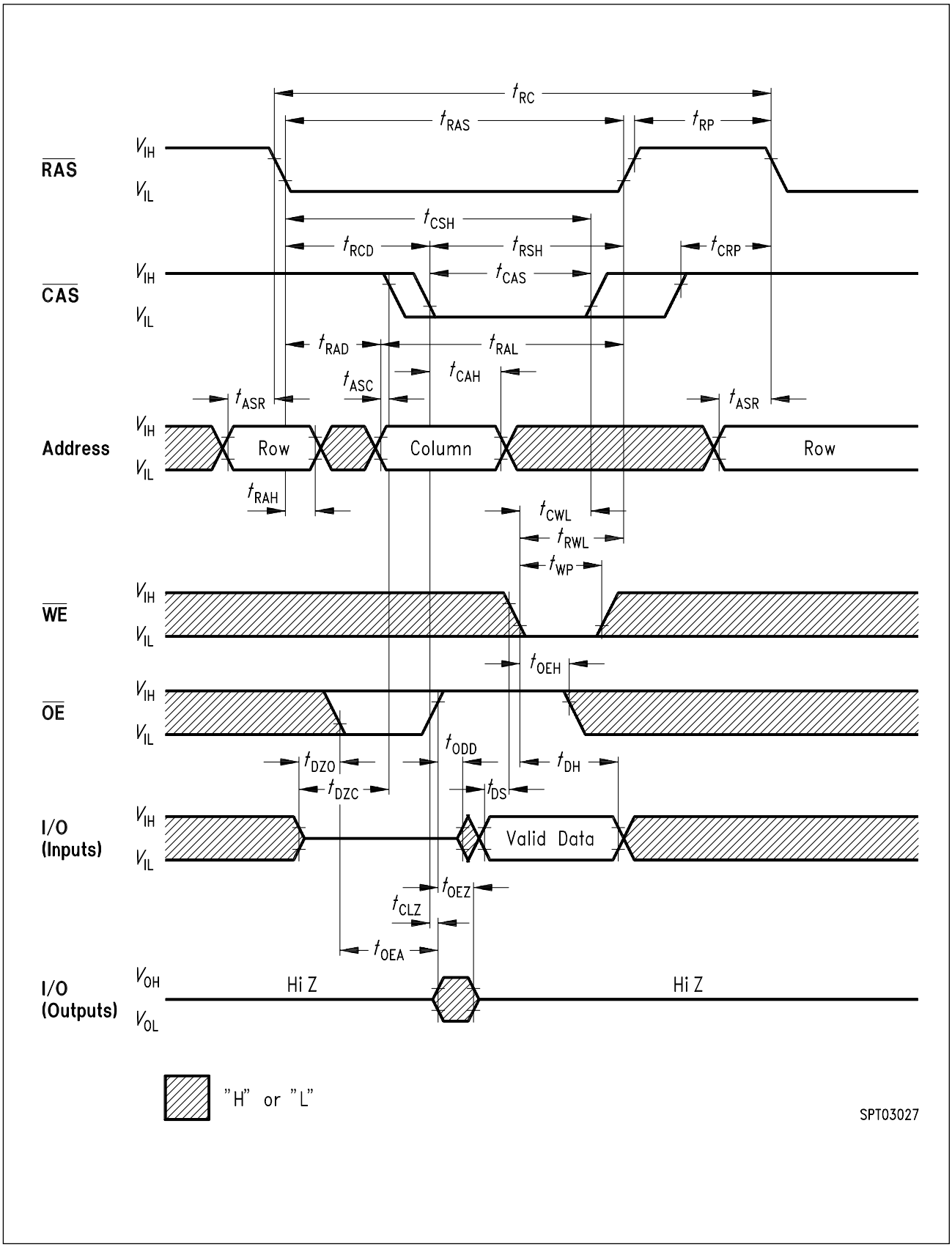
16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.


t_{RC}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
CAS
t_{RAD}
t_{RAL}
t_{CAH}
t_{ASC}
t_{ASR}
Address
Row
Column
Row
t_{RAH}
t_{RCH}
t_{RCS}
t_{RRH}
WE
t_{AA}
t_{OEA}
OE
t_{DZC}
t_{CDD}
t_{DZO}
t_{ODD}
I/O
(Inputs)
t_{OFF}
t_{CAC}
t_{CLZ}
t_{OEZ}
V_{OH}
V_{OL}
I/O
(Outputs)
Hi Z
Valid Data OUT
Hi Z
t_{RAC}
"H" or "L"
SPT03025

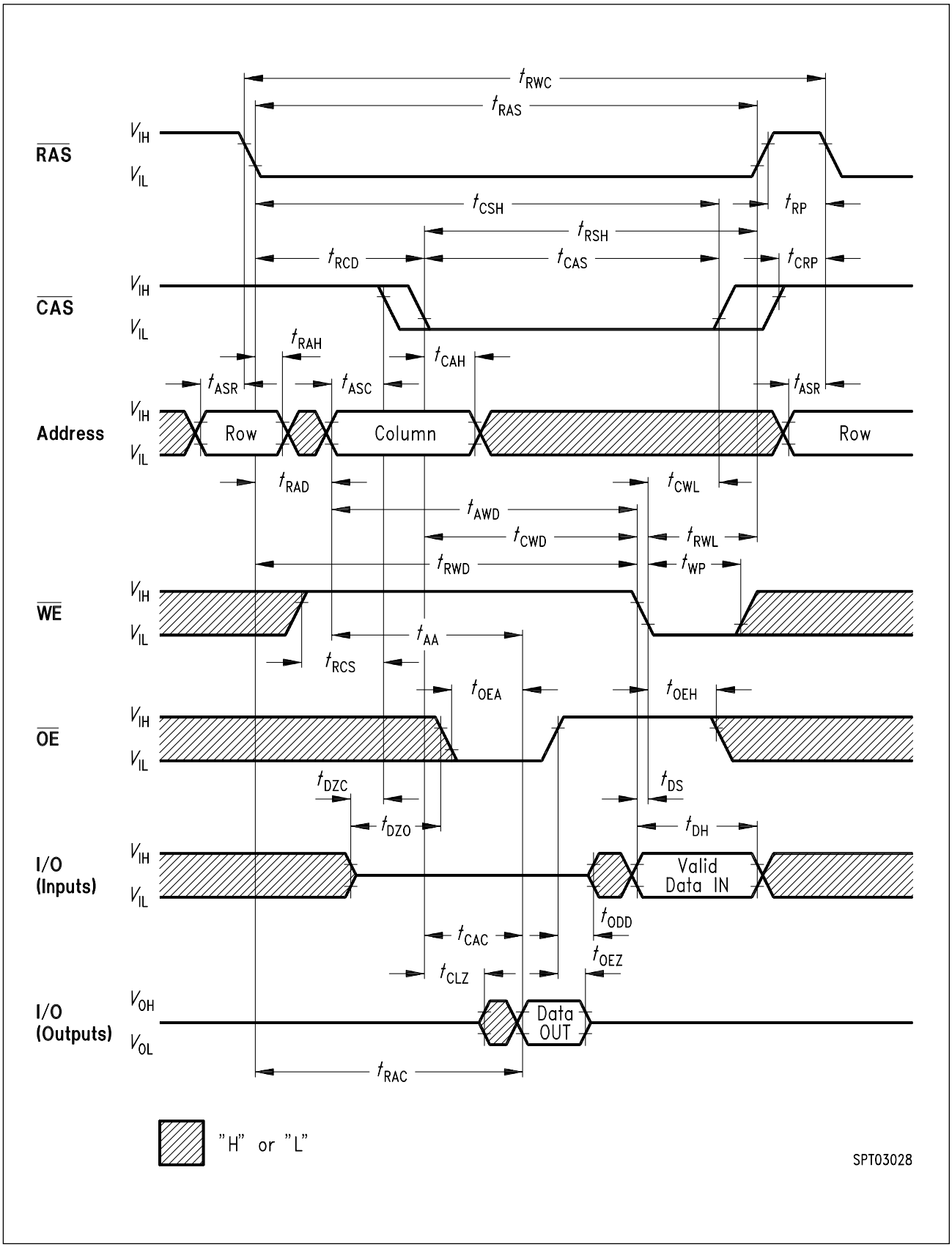
Read Cycle



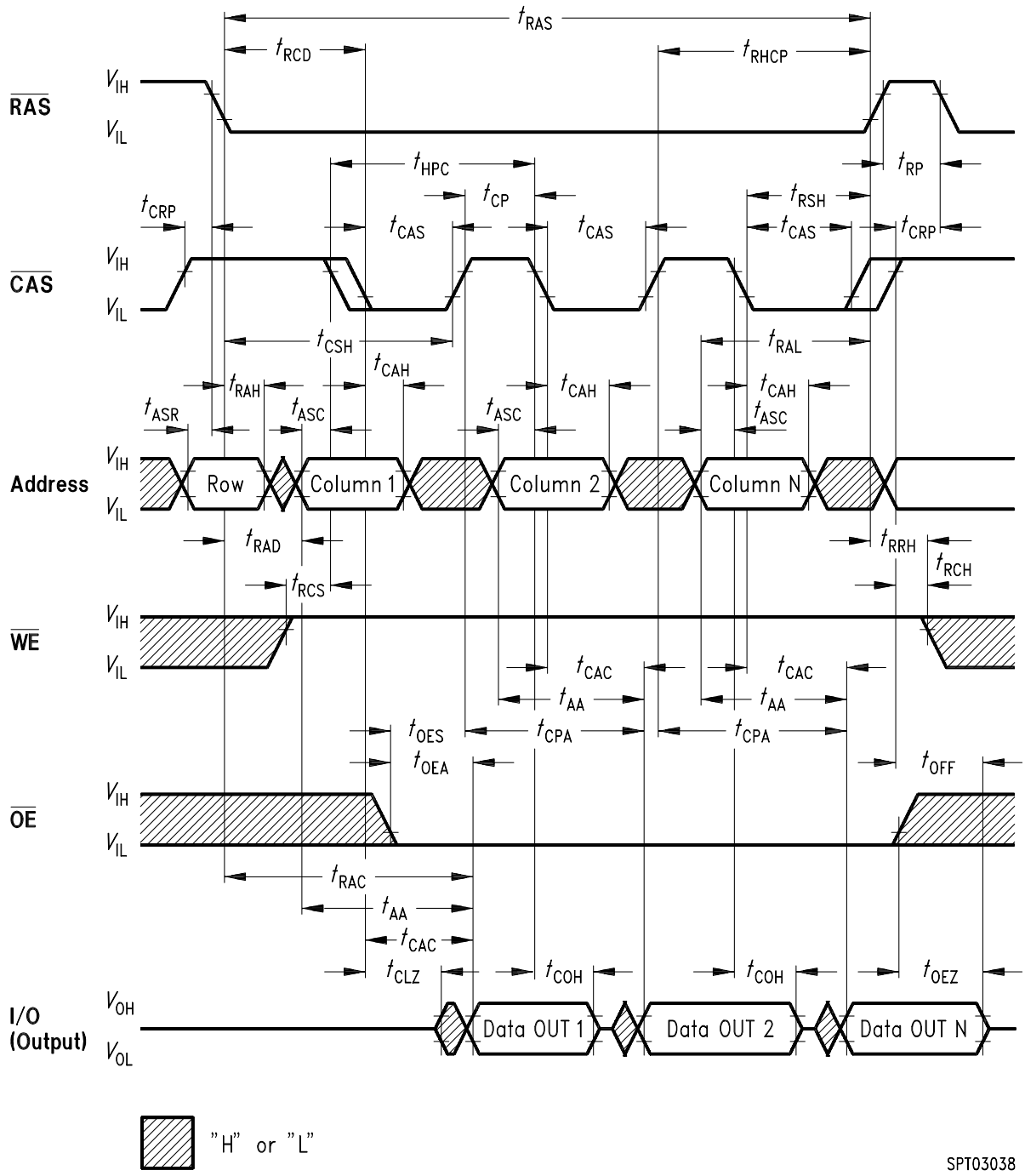
Write Cycle (Early Write)



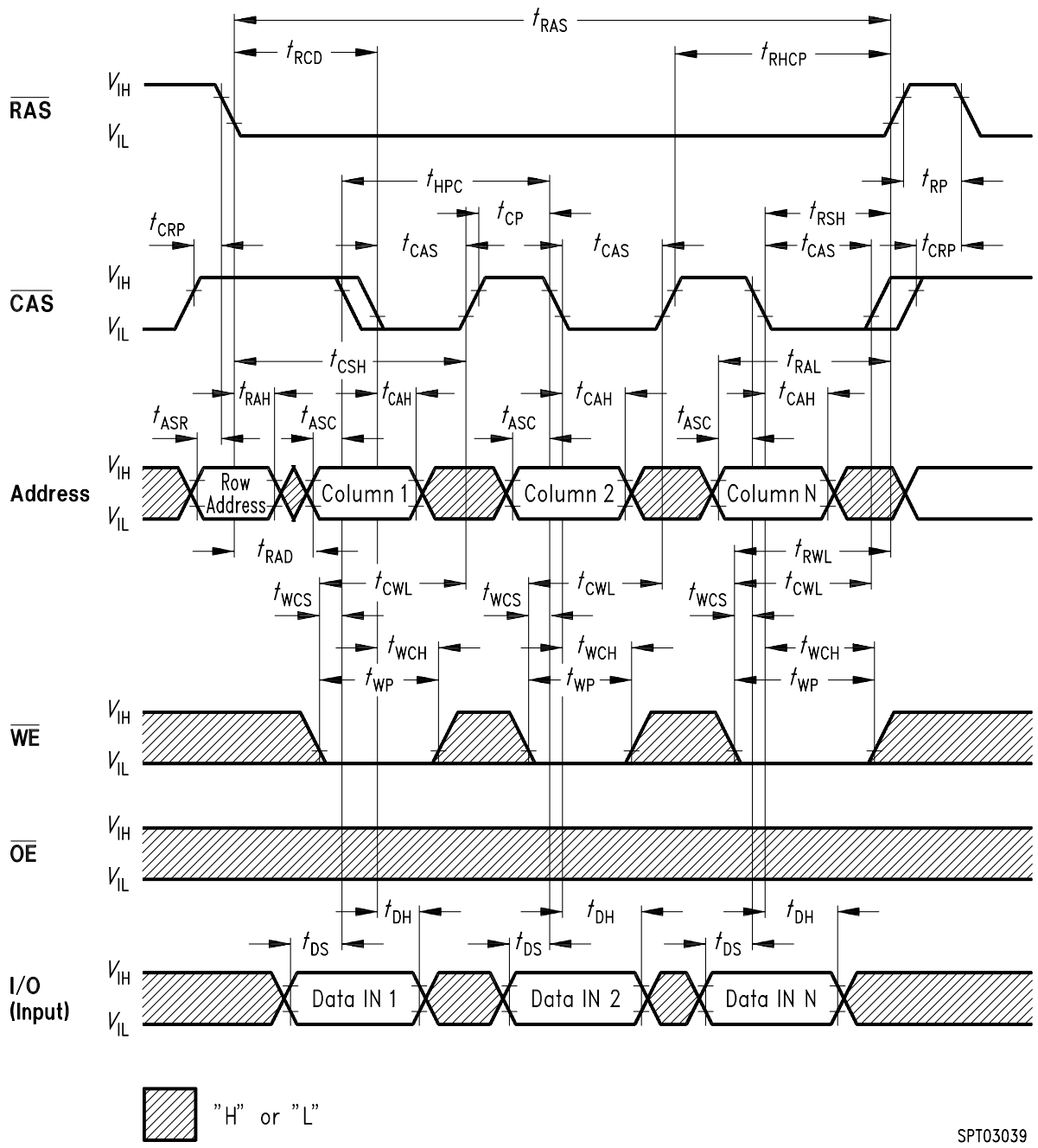
Write Cycle ($\overline{OE}$ Controlled Write)



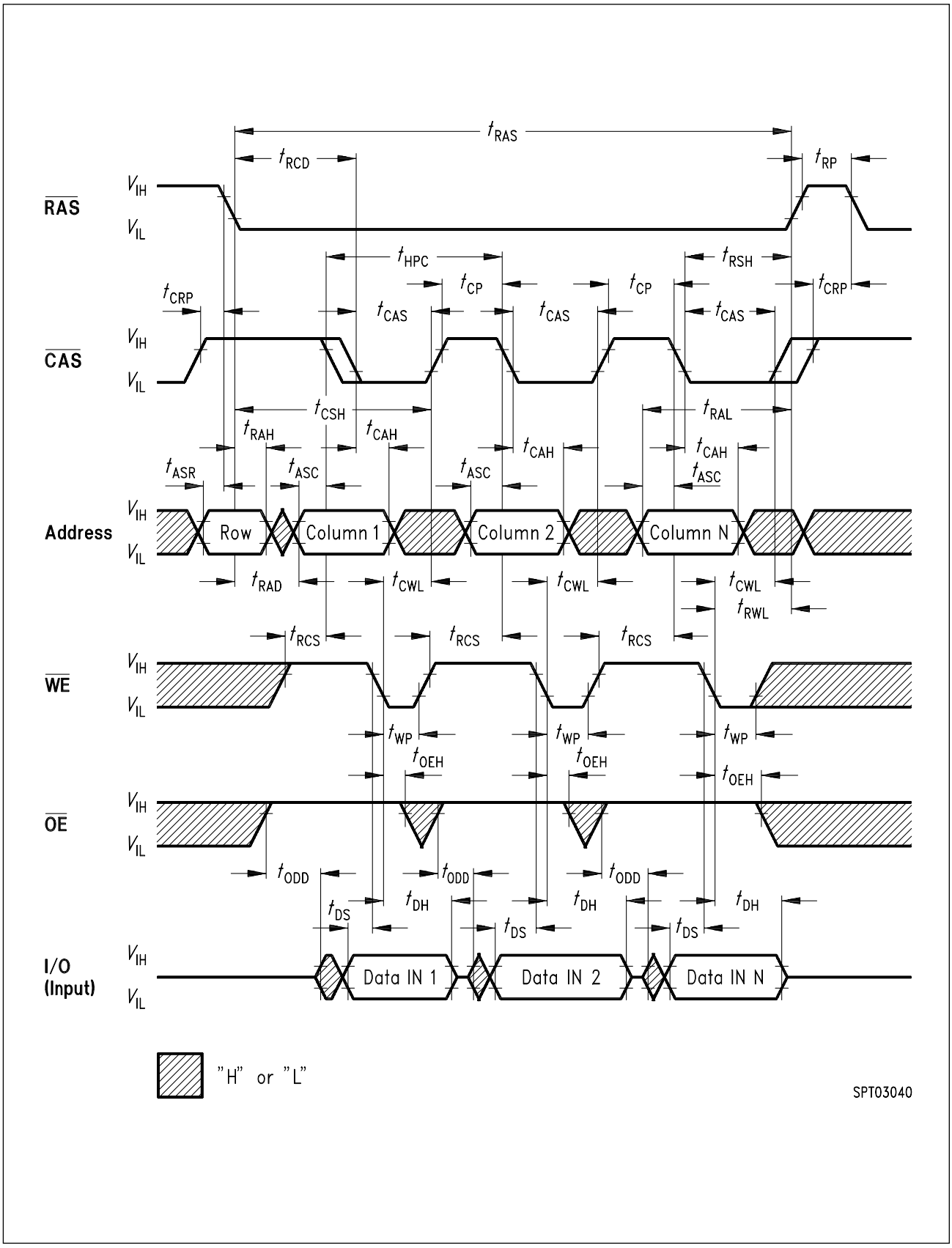
Read-Write (Read-Modify-Write) Cycle



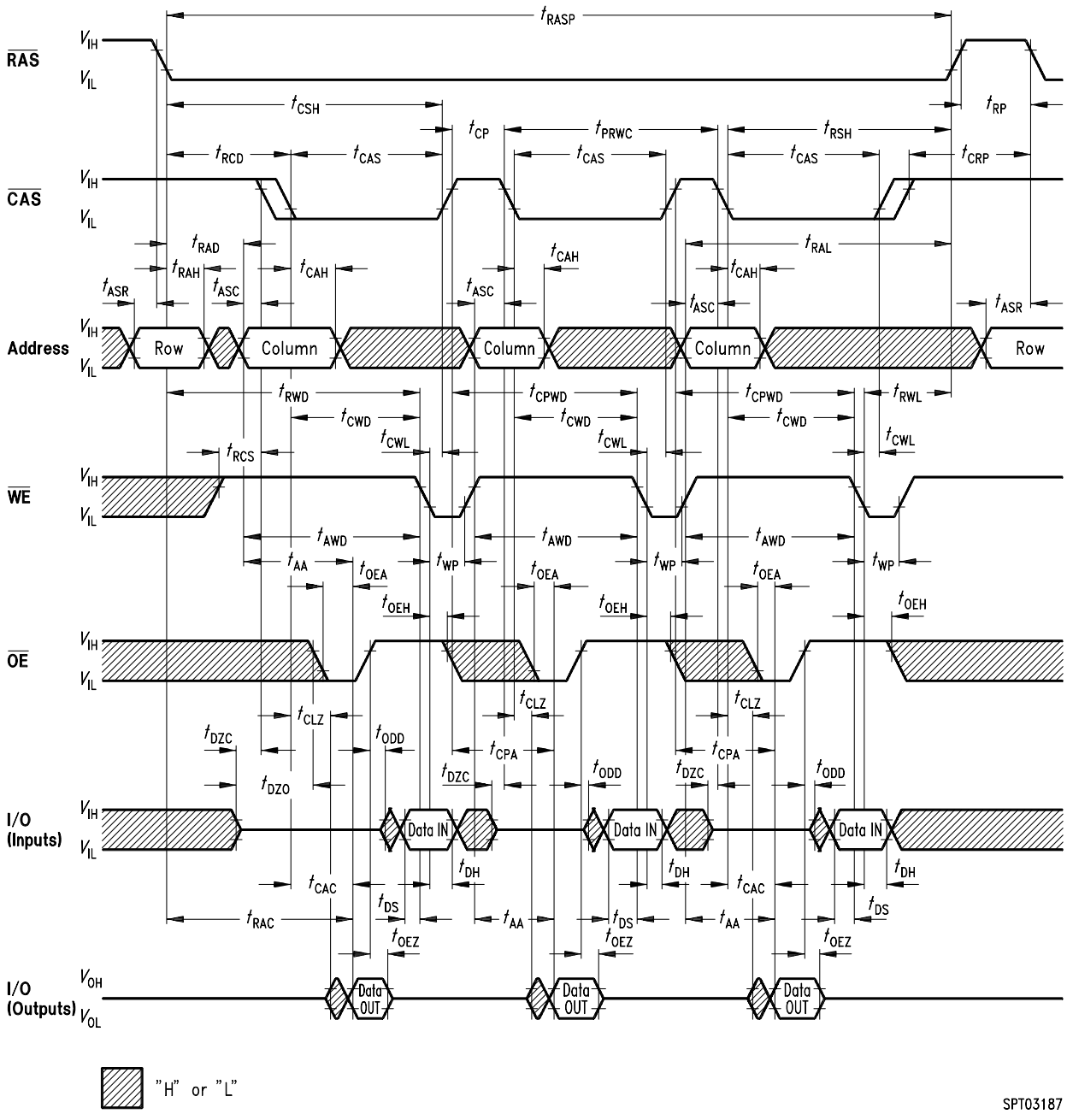
Hyper Page Mode (EDO) Read Cycle



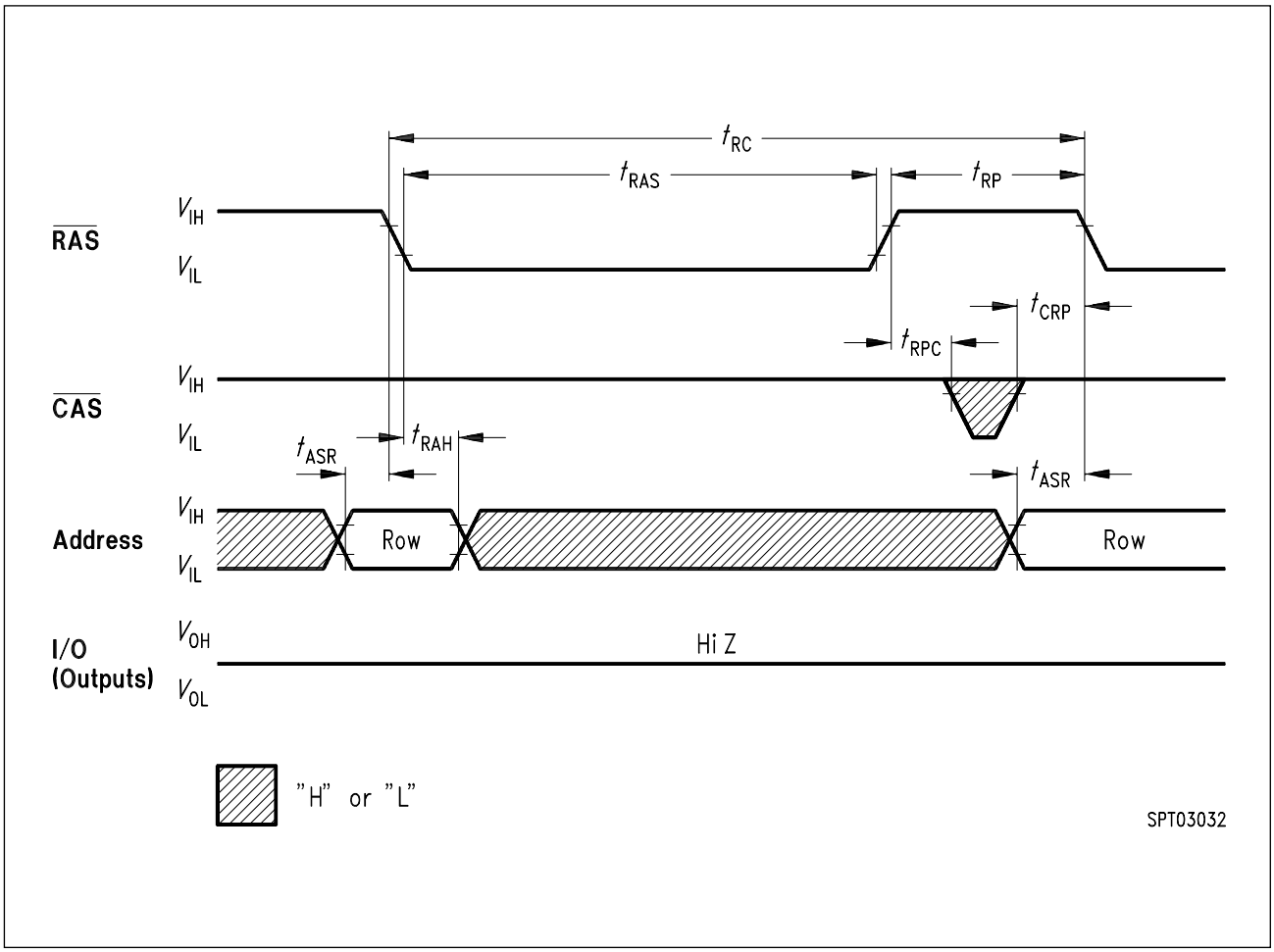
Hyper Page Mode (EDO) Early Write Cycle



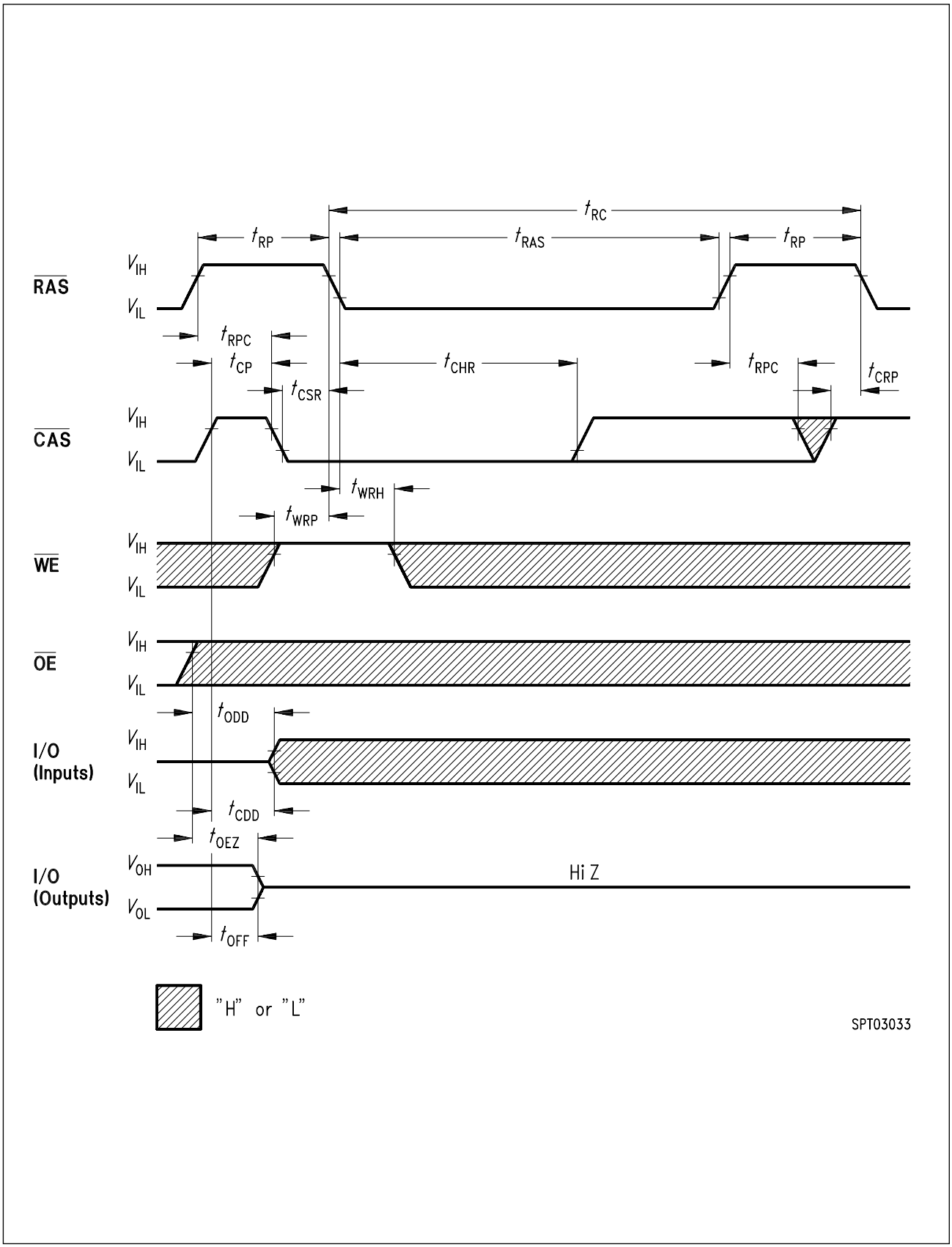
Hyper Page Mode (EDO) Late Write Cycle



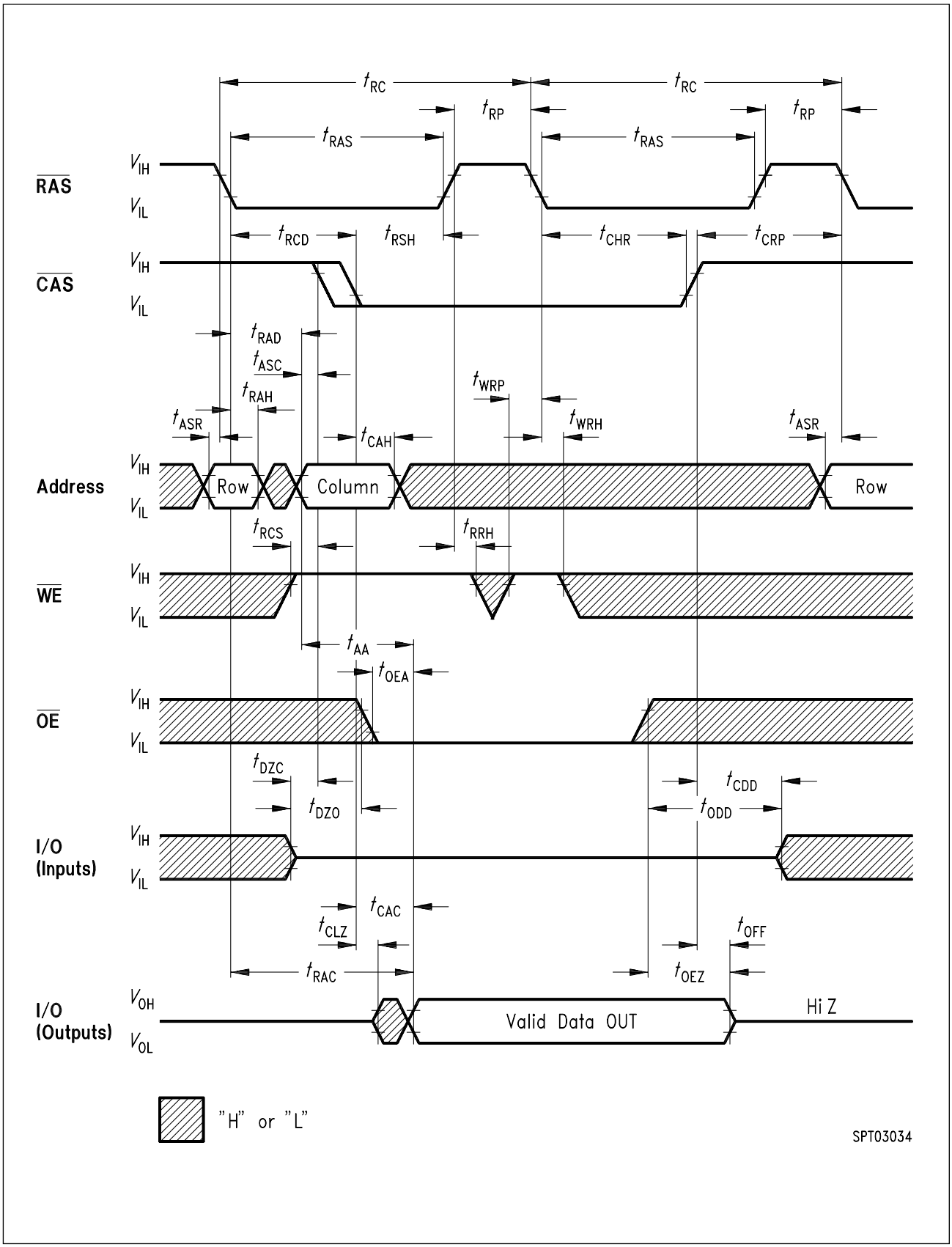
Hyper Page Mode (EDO) Read-Modify-Write Cycle



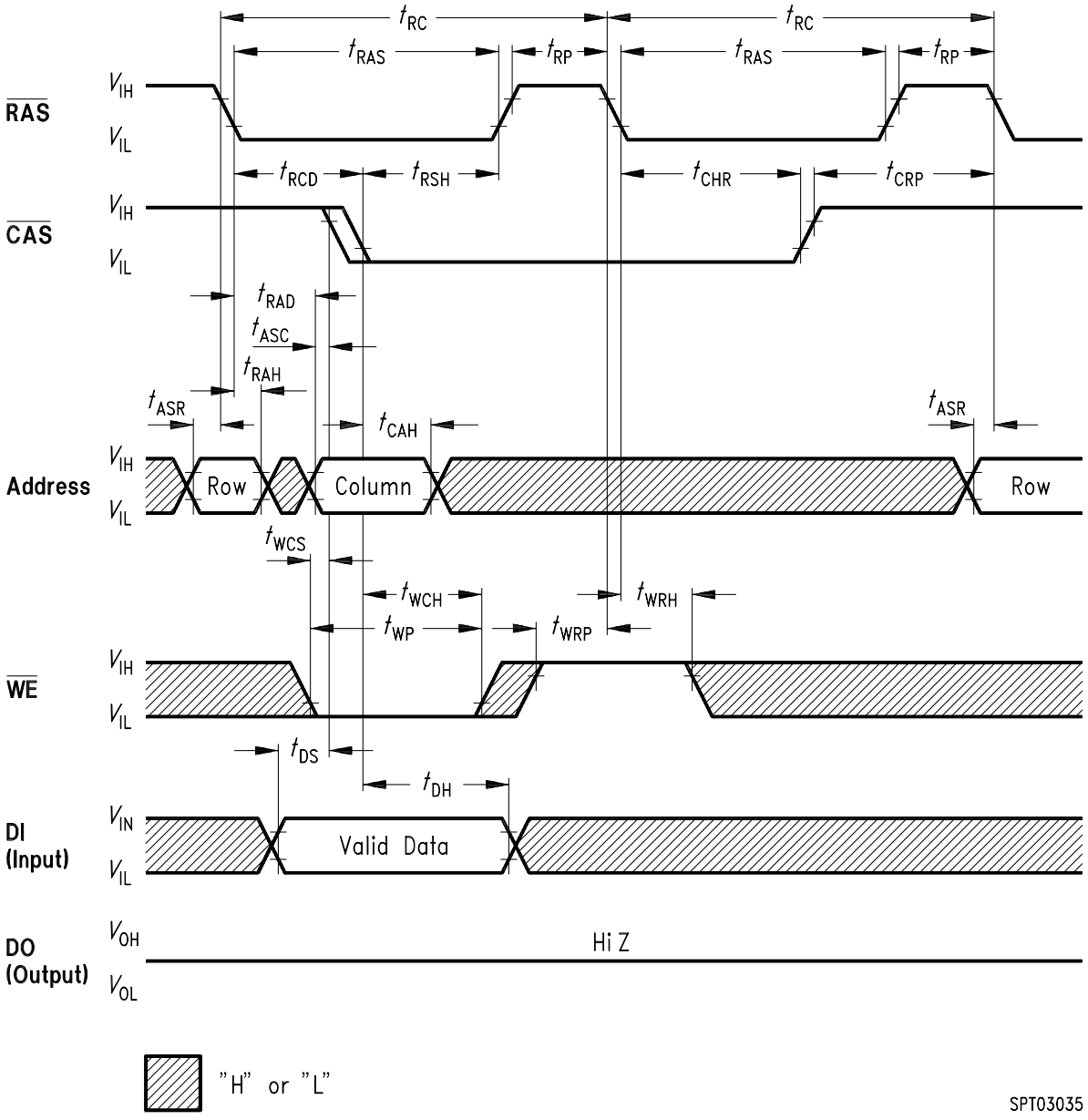
$\overline{RAS}$-Only Refresh Cycle



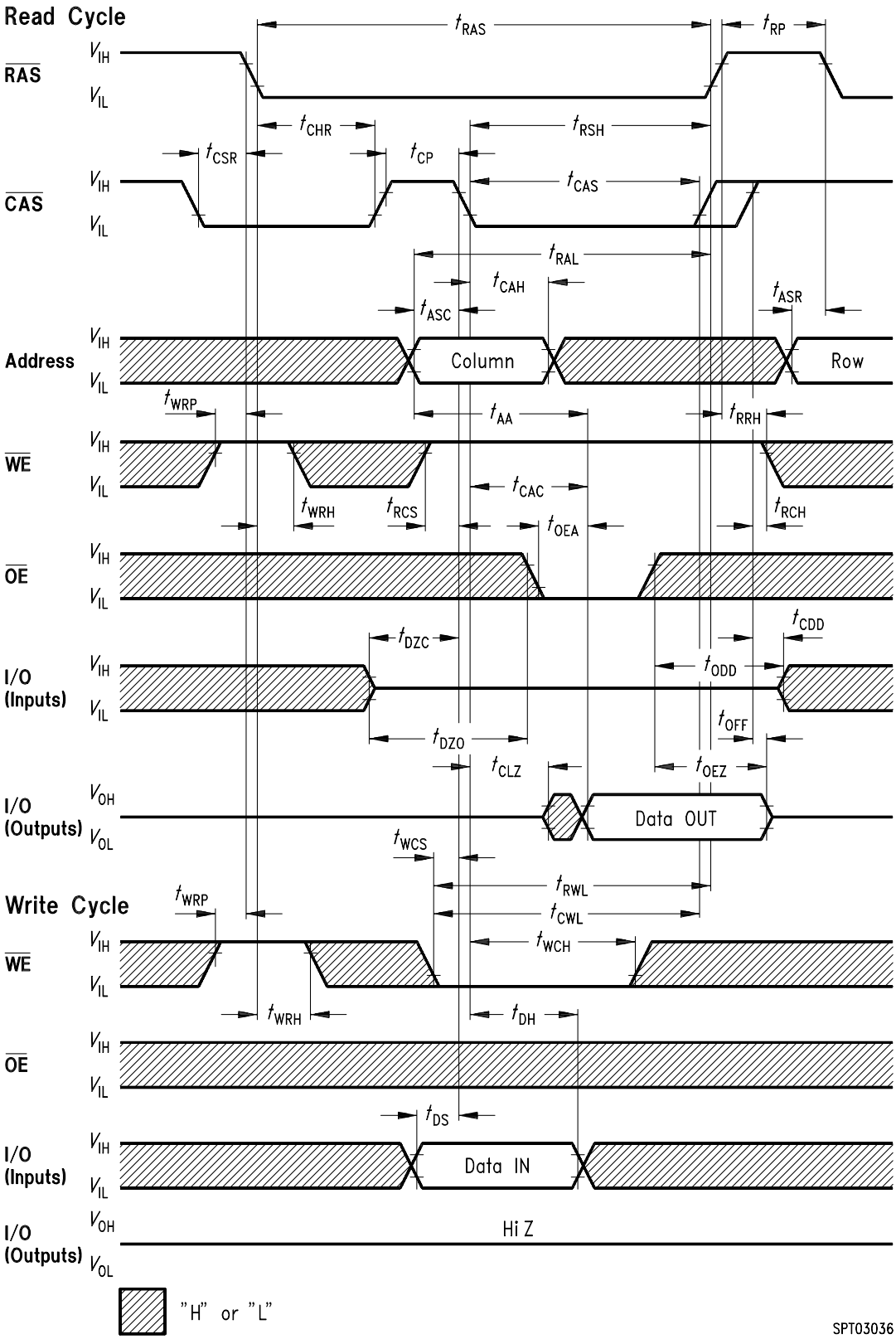
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



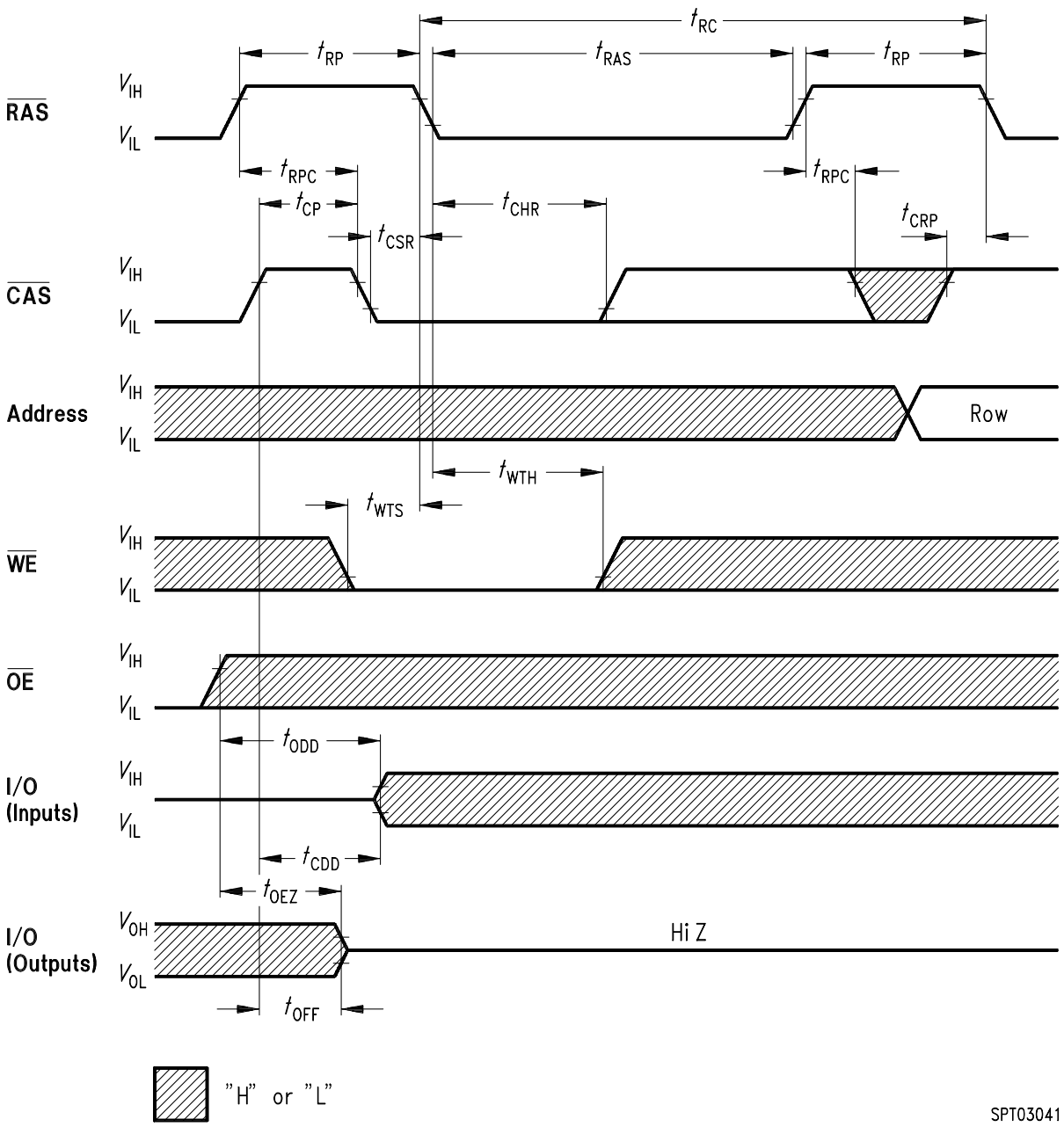
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

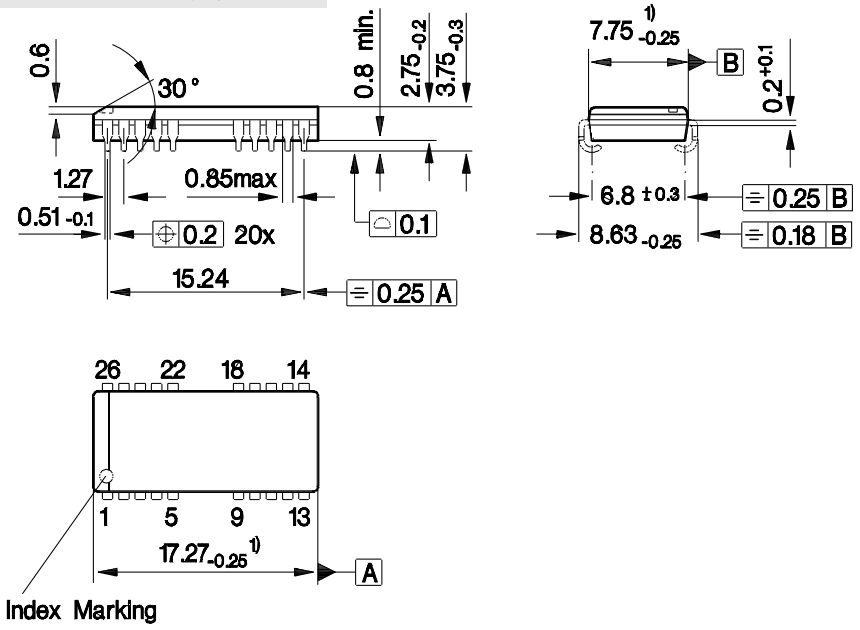
As the HYB 314405BJ/BT is organized internally as 512 K x 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note that in the 1 M x 4 version the test time is reduced by 1/2 for a linear test pattern.

In a test mode “write” the data from each I/O1 pin is written into eight bits simultaneously (all “1” s or all “0” s). The I/O2-I/O4 inputs are not used for writing in test mode. In test mode “read” each I/O output is used for indicating the test mode result. If the internal eight bits are equal, the I/O would indicate a “1”. If they were not equal, the I/O would indicate a “0”. Note that in test mode „read“ I/O1-I/O3 are always driven to „ones“, i.e. all outputs will be „1“s for a test mode „pass“. The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a “$\overline{CAS}$ before $\overline{RAS}$ refresh”, “$\overline{RAS}$ only refresh” or “Hidden refresh” can be used.

Addresses A10R, A10C and A0C are don‘t care during test mode.

Package Outlines

P-SOJ-26/20-5
(Small Outline J-Leaded Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPJ05627

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm