

LH5324P00A

PRELIMINARY

**CMOS 24M (3M × 8/1.5M × 16)
Mask-Programmable ROM**

FEATURES

- 3,145,728 words × 8 bit organization (Byte mode)
1,572,864 words × 16 bit organization (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
Operating: 440 mW (MAX.)
Standby: 1650 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package: 44-pin, 600-mil SOP

DESCRIPTION

The LH5324P00A is a 24M-bit mask-programmable ROM organized as 3,145,728 × 8 bits (Byte mode) or 1,572,864 × 16 bits (Word mode) that can be selected by a $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

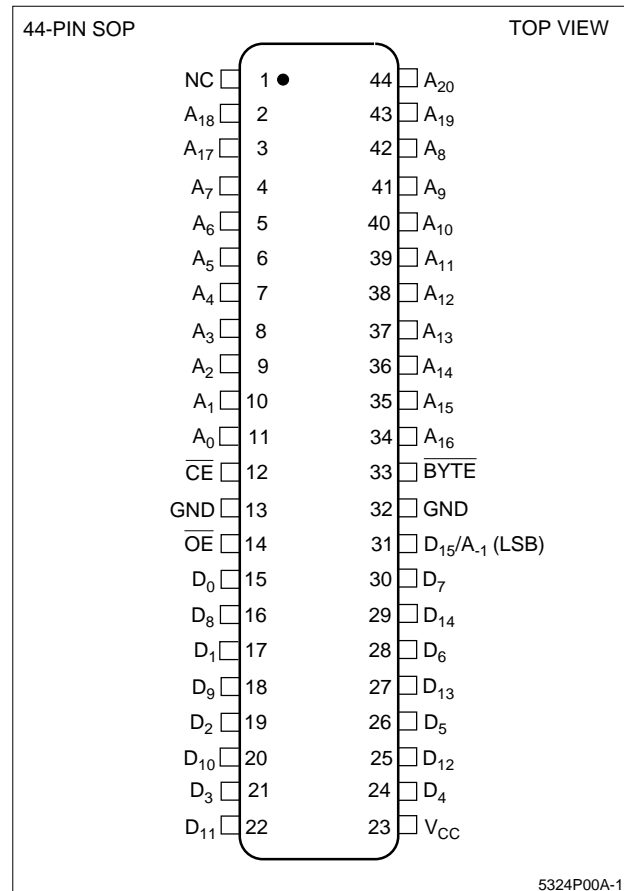
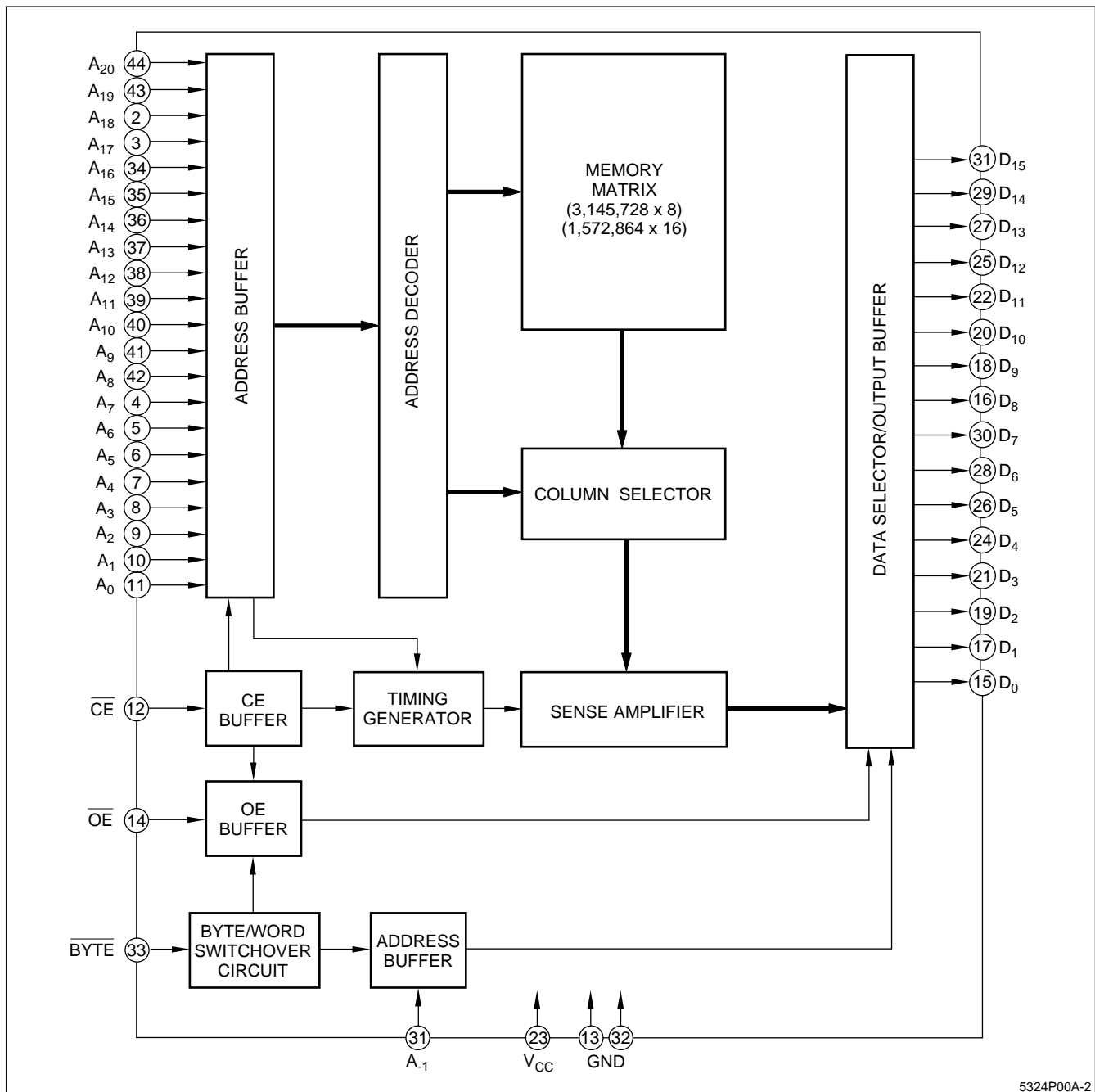


Figure 1. Pin Connections for SOP Package



5324P00A-2

Figure 2. LH5324P00A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₋₁ – A ₂₀	Address input	1
D ₀ – D ₁₅	Data output	1
$\overline{\text{BYTE}}$	Byte/word mode switch	1
$\overline{\text{CE}}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{\text{OE}}$	Output Enable input	
V _{CC}	Power supply (+5 V)	
GND	Ground	
NC	No connection	

NOTE:

- The D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the $\overline{\text{BYTE}}$ pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.

TRUTH TABLE

\overline{CE}	\overline{OE}	BYTE	A ₋₁ (D ₁₅)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT	NOTE
				D ₀ – D ₇	D ₈ – D ₁₅	LSB	MSB		
H	X	X	X	High-Z	High-Z	–	–	Standby (I _{SB})	1
L	H	X	X	High-Z	High-Z	–	–	Operating (I _{CC})	1
L	L	H	–	D ₀ – D ₇	D ₈ – D ₁₅	A ₀	A ₂₀	Operating (I _{CC})	
L	L	L	L	D ₀ – D ₇	High-Z	A ₋₁	A ₂₀	Operating (I _{CC})	
L	L	L	H	D ₈ – D ₁₅	High-Z	A ₋₁	A ₂₀	Operating (I _{CC})	

NOTE:

1. X = H or L; High-Z = High-impedance

When the address inputs become 'High' to both A₁₉ and A₂₀, the data outputs become 'Unspecified' since the data does not exist in this address area.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}		2.2	V _{CC} + 0.3	V	
Input 'Low' voltage	V _{IL}		–0.3	0.8	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4		V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA		0.4	V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 150 ns		80	mA	2
	I _{CC2}	t _{RC} = 1 μs		70		
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$		300		
Input capacitance	C _{IN}	f = 1 MHz		10	pF	
Output capacitance	C _{OUT}	T _A = 25°C		10	pF	

NOTES:

1. $\overline{CE}/\overline{OE} = V_{IH}$

2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable access time	t_{ACE}		120	ns	
Output enable delay time	t_{OE}		60	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		50	ns	1
OE to output in High-Z	t_{OHZ}		50	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

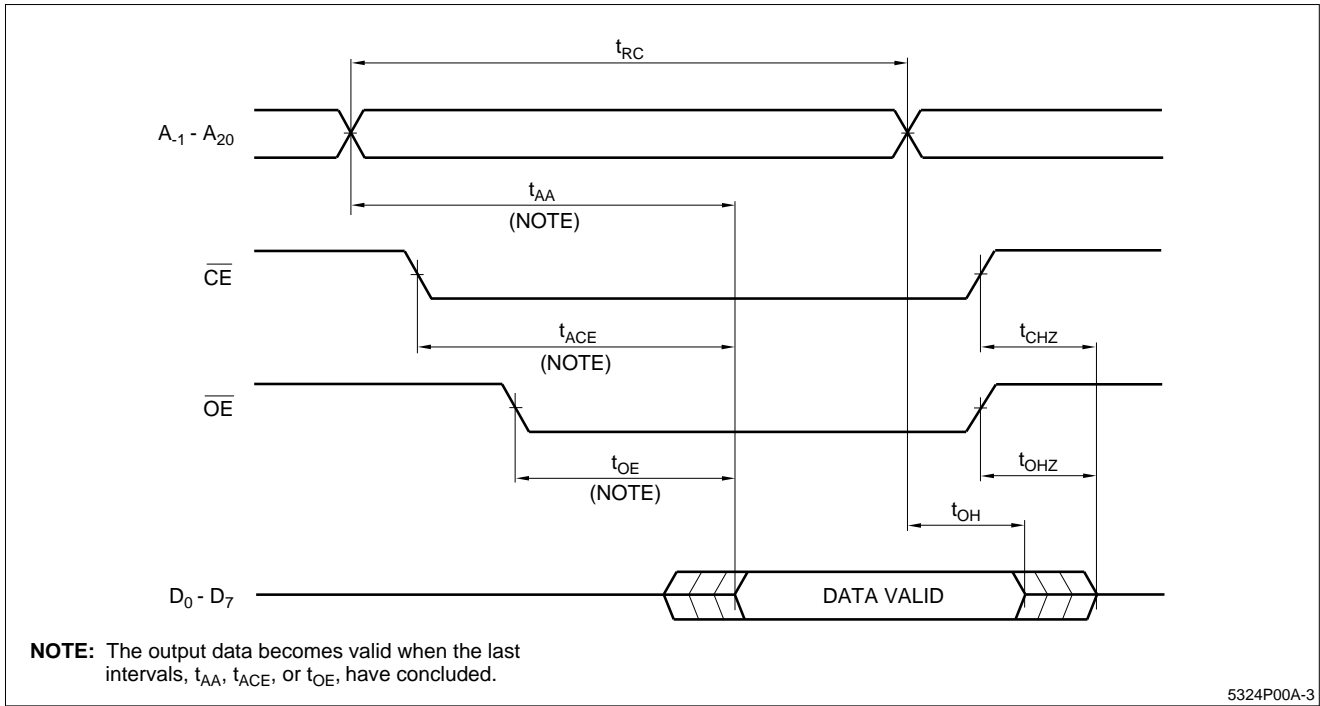


Figure 3. Byte Mode ($\overline{BYTE} = V_{IL}$)

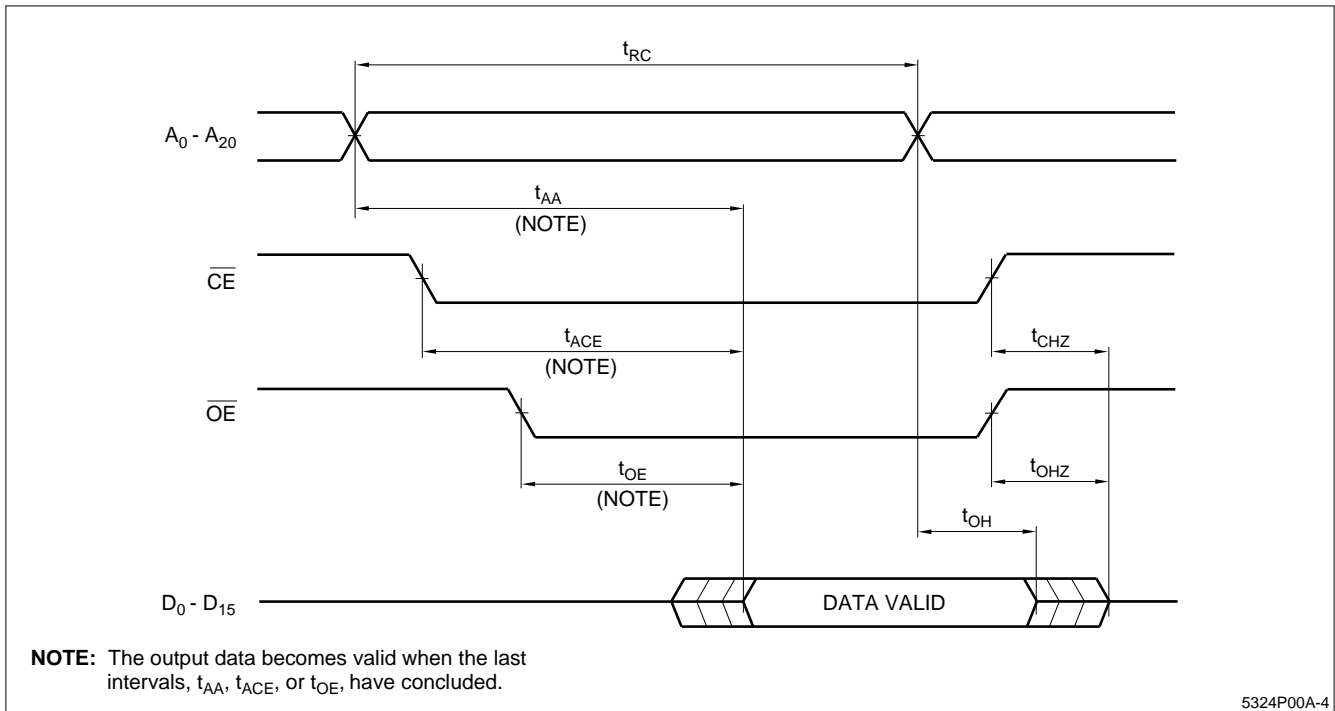
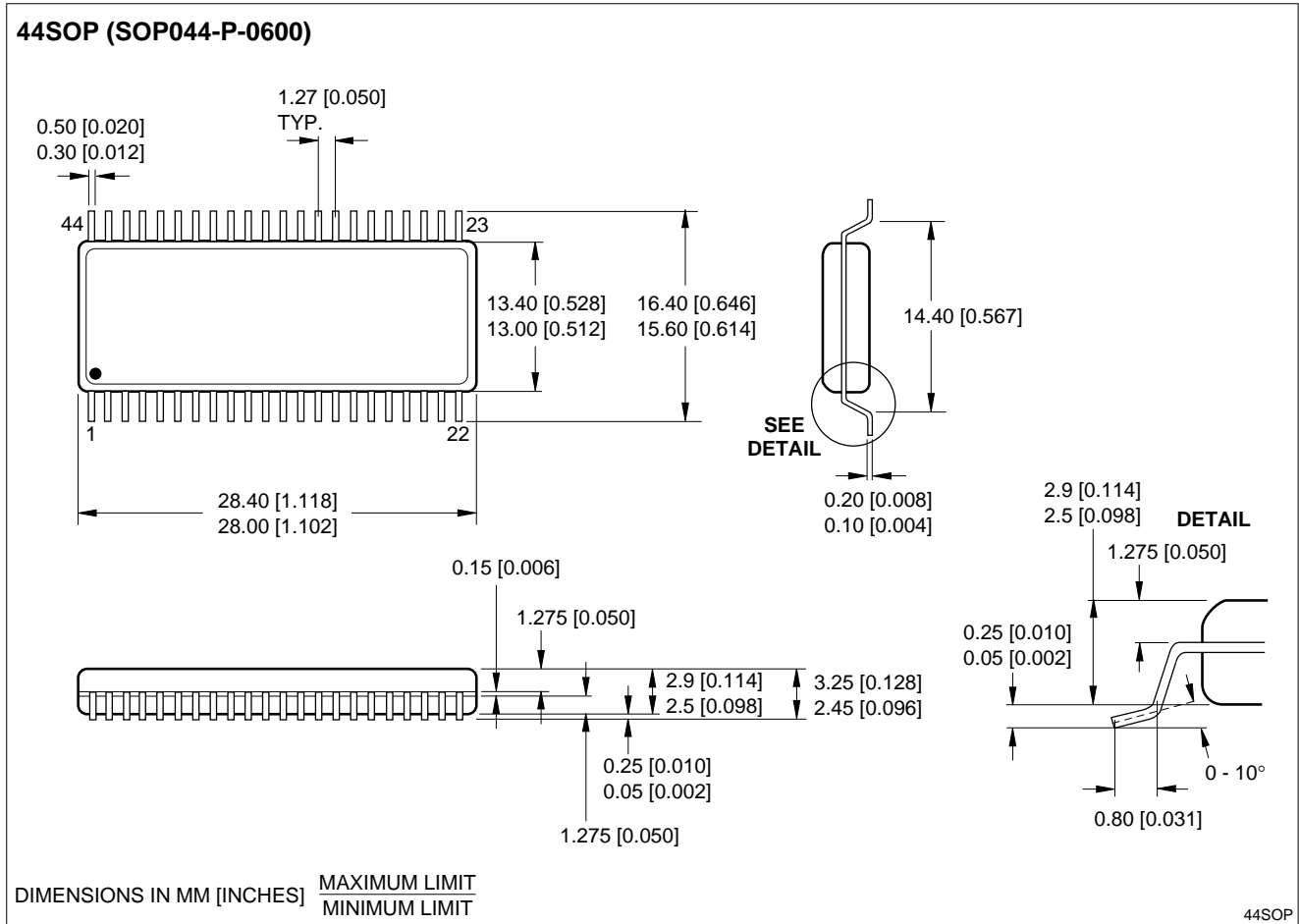


Figure 4. Word Mode ($\overline{BYTE} = V_{IH}$)

PACKAGE DIAGRAM



44-pin, 600-mil SOP

ORDERING INFORMATION

