



## M1725

CMOS IC

### 16-BIT, 96KHZ STEREO AUDIO D/A CONVERTER

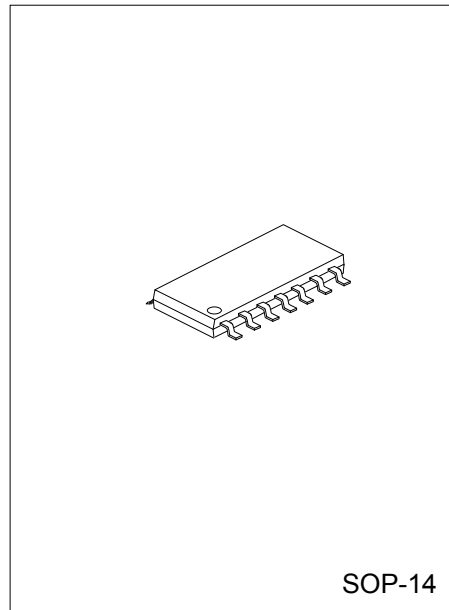
#### DESCRIPTION

The UTC **M1725** is a complete stereo digital-to-analog output system including a 16-bit D/A conversion, a 5-level 3rd-order  $\Delta\Sigma$  modulator, a digital interpolation filter, and an analog output amplifier in a small 14-pin package.

The UTC **M1725** can be operating with from a single 5V power supply and requires minimal support circuitry. These features are ideal for set-top boxes, DVD players and A/V receivers, etc.

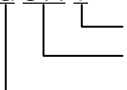
#### FEATURES

- \* Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- \* 16-Bit Conversion
- \* 95dB Dynamic Range
- \* Single +5V Power Supply
- \* 16kHz to 96kHz Multiple Sampling Frequencies
- \* 8X Oversampling Digital Filter
- \*  $256 f_s / 384 f_s$  System Clock
- \* Normal or I<sup>2</sup>S Data Input Formats

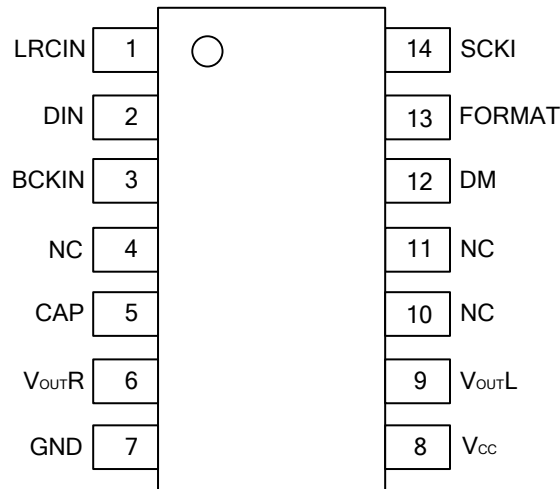


#### ORDERING INFORMATION

Ordering Number	Package	Packing
M1725G-S14-R	SOP-14	Tape Reel

<p>M1725G-S14-T</p>  <p>(1)Packing Type (2)Package Type (3)Halogen Free</p>	<p>(1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free</p>
--	---

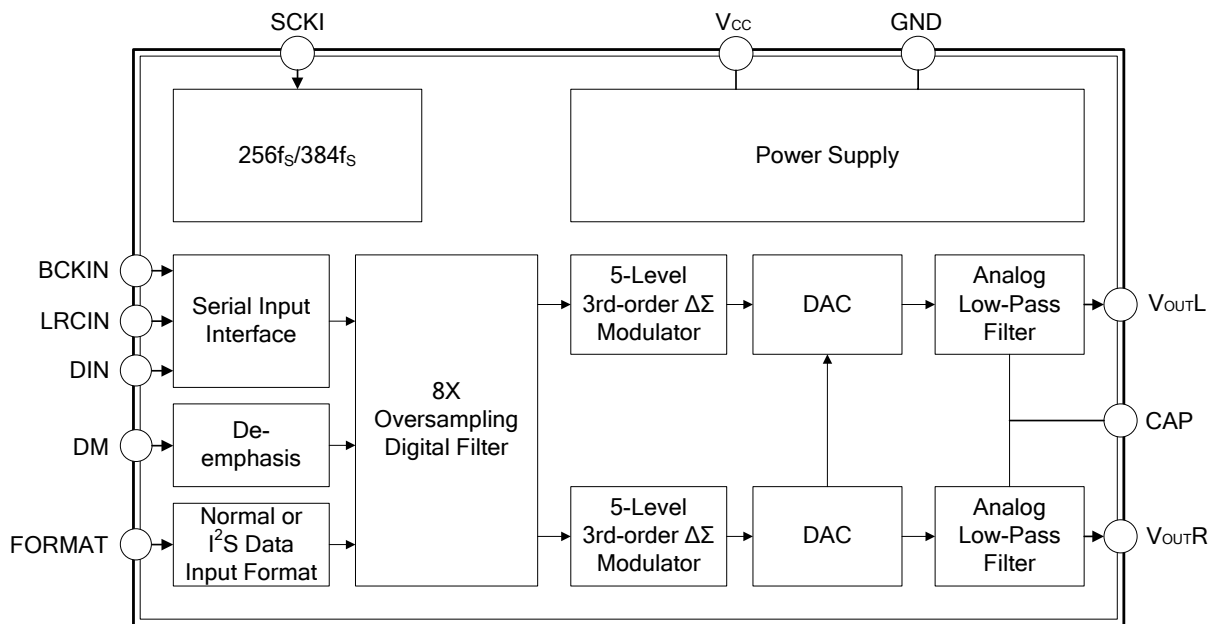
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NO	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	LRCIN	I	Left/Right Clock Input
2	DIN	I	Serial Audio Data Input
3	BCKIN	I	Bit Clock Input for Audio Data
4	NC	--	No Connection
5	CAP	I/O	Common Pin of Analog Output Amp
6	VoutR	O	Right-Channel Analog Output
7	GND	I/O	Ground
8	Vcc	I/O	Power Supply
9	VoutL	O	Left-Channel Analog Output
10	NC	--	No Connection
11	NC	--	No Connection
12	DM	I	De-emphasis Control High: De-emphasis OFF Low: De-emphasis ON(44.1kHz)
13	FORMAT	I	Audio Data Format Select High: I <sup>2</sup> S Data Format Low: Standard Data Format
14	SCKI	I	System Clock Input (256 f <sub>S</sub> or 384 f <sub>S</sub> )

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V <sub>CC</sub>	+6.5	V
+ V <sub>CC</sub> to+ V <sub>DD</sub> Difference	V <sub>D</sub>	±0.1	V
Input Logic Voltage	V <sub>LGC</sub>	-0.3V to (V <sub>DD</sub> +0.3V)	V
Power Dissipation	P <sub>D</sub>	300	mW
Operating Temperature Range	T <sub>OPR</sub>	-25 ~ +85	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V <sub>CC</sub>	4.5 ~ 5.5	V
Junction Temperature	T <sub>J</sub>	-25 ~ +85	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ +100	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ <sub>JA</sub>	70	°C/W

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V<sub>CC</sub>=+5V, f<sub>s</sub>=44.1kHz, CAP=10uF, 16-Bit Input Data, SCKI=384 f<sub>s</sub>, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DATA FORMAT</b>						
Data Bit Length					16	Bits
Input sample Rate	f <sub>s</sub>		16		96	kHz
Internal System Clock Frequency	SCKI			256/384		f <sub>s</sub>
<b>DIGITAL INPUT/OUTPUT</b>						
Logic Level				TTL		
Input Logic Level (Note1)	V <sub>IH</sub>		2			V
	V <sub>IL</sub>				0.8	V
Input Logic Current (Note1)	I <sub>IN</sub>				±0.8	uA
<b>DYNAMIC PERFORMANCE (Note2)</b>						
THD+N at FS (0dB)		f=991kHz		-83	-78	dB
THD+N at -60dB		f=991kHz		-32		dB
Dynamic Range	DR	f=991kHz,A-weighted	90	95		dB
Signal-to-Noise Ratio	SNR	f=991kHz,A-weighted	90	97		dB
Channel Separation	CS	f=991kHz	88	95		dB
<b>DC ACCURACY</b>						
Gain Error				±1.0	±5.0	% of FSR
Gain Mis-match(Channel-to-Channel)				±1.0	±5.0	% of FSR
Bipolar Zero Error	BZE	V <sub>OUT</sub> =V <sub>CC</sub> /2 at BPZ		±20	±50	mV
<b>ANALOG OUTPUT</b>						
Output Voltage	V <sub>O</sub>	Full Scale(0dB)		0.62*V <sub>CC</sub>		V <sub>P-P</sub>
Center Voltage	V <sub>C</sub>			V <sub>CC</sub> /2		V
Load Impedance	R <sub>L</sub>	AC Load	10			kΩ

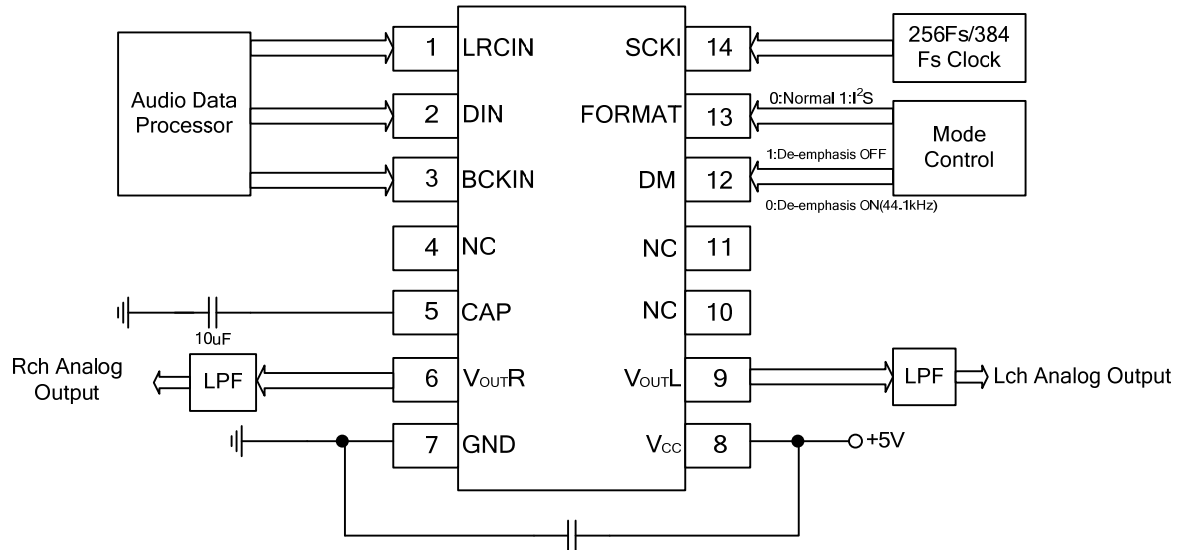
Note: 1. Pins 1, 2, 3, 12, 13: LRCIN, DIN, BCKIN, DM, FORMAT (Schmitt Trigger Input); Pin 14: SCKI.

2. Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

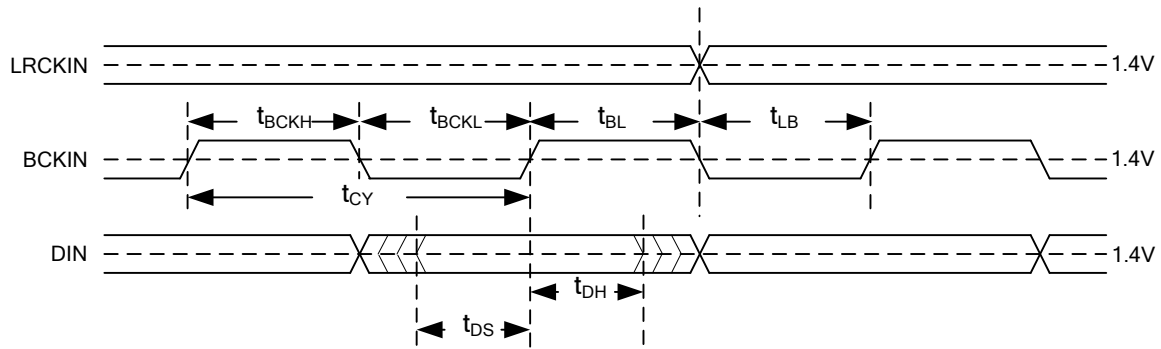
■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL FILTER PERFORMANCE</b>						
Passband					0.445	$f_s$
Stopband			0.555			$f_s$
Passband Ripple					$\pm 0.17$	dB
Stopband Attenuation			-35			dB
Delay Time	$T_D$			$11.125/f_s$		Sec
<b>INTERNAL ANALOG FILTER</b>						
-3dB Bandwidth				100		kHz
Passband Response		$f=20\text{kHz}$		-0.16		dB
<b>POWER SUPPLY REQUIREMENTS</b>						
Voltage Range	$V_{CC}$		4.5	5	5.5	V
Supply Current	$I_Q$			13	18	mA
Power Dissipation	$P_D$			65	90	mW

■ TYPICAL APPLICATIONS CIRCUIT



■ TIMING DIAGRAMS



$t_{CY}$	BCKIN Pulse Cycle Time	$\geq 100\text{ns}$
$t_{BCKH}$	BCKIN Pulse Width High	$\geq 50\text{ns}$
$t_{BCKL}$	BCKIN Pulse Width Low	$\geq 50\text{ns}$
$t_{BL}$	BCKIN Rising Edge to LRCIN Edge	$\geq 30\text{ns}$
$t_{LB}$	LRCIN Edge to BCKIN Rising Edge	$\geq 30\text{ns}$
$t_{DS}$	DIN Set Up Time	$\geq 30\text{ns}$
$t_{DH}$	DIN Hold Time	$\geq 30\text{ns}$

Figure 1.Audio Data Input Timing

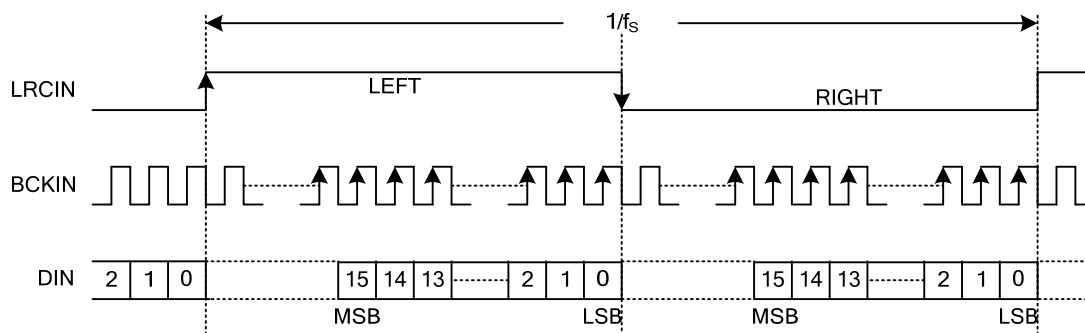


Figure 2.Normal Data Input Timing

■ TIMING DIAGRAMS (Cont.)

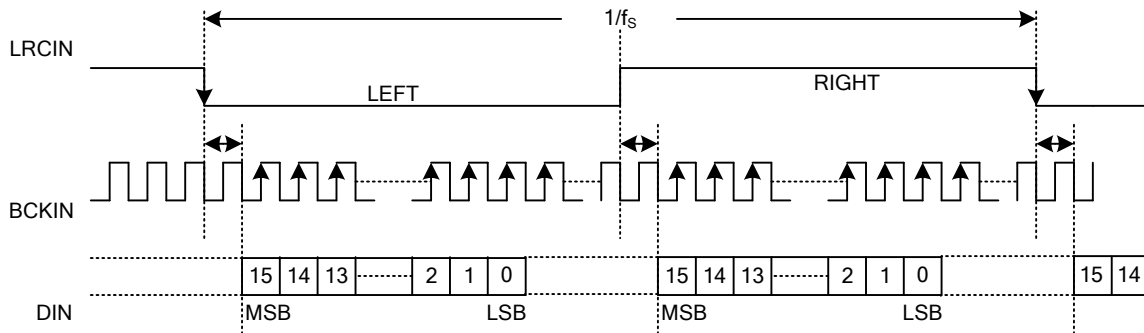
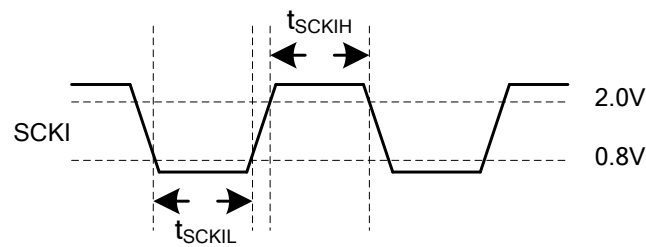


Figure 3. I²S Data Input Timing



$t_{SCKIH}$	System Clock Pulse Width High	$\geq 13\text{ns}$
$t_{SCKIL}$	System Clock Pulse Width Low	$\geq 13\text{ns}$

Figure 4. System Clock Timing



■ FUNCTIONAL DESCRIPTION

**SYSTEM CLOCK**

The system clock (SCKI) must be either  $256 f_s$  or  $384 f_s$ , where  $f_s$  is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz or 48kHz. The system clock is used to operate the digital filter and the noise shaper. Timing conditions for SCKI are shown in **Figure4**.

**M1725** includes a system clock detection circuit which auto-matically detects the frequency, either  $256 f_s$  or  $384 f_s$ . The system clock should be synchronized with LRCIN, but **M1725** can compensate for phase differences. If the phase difference between LRCIN and system clock is greater than  $\pm 6$  bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state ( $V_{CC}/2$ ) during the synchronization function. The typical system clock frequency inputs vs sampling rate for the **M1725** is shown below.

SAMPLING RATE(LRCIN)(kHz)	SYSTEM CLOCK FREQUENCY(MHz)	
	$256 f_s$	$384 f_s$
32	8.192	12.288
44.1	11.2896	16.934
48	12.288	18.432

**INPUT DATA FORMAT**

**M1725** can accept input data in either normal (MSB-first, right-justified) or I<sup>2</sup>S format by applying LOW or HIGH voltage level on FORMAT-pin.

FORMAT	INPUT DATA FORMAT SELECTED
Low	Normal Format (MSB-first, right-justified)
High	I2S Format (Philips serial data protocol)

**DE-EMPHASIS CONTROL**

DM-pin enables **M1725**'s de-emphasis function. De-emphasis operates only at 44.1kHz.

DM	DE-EMPHASIS FUNCTION SELECTED
Low	De-emphasis ON (44.1kHz)
High	De-emphasis OFF

**RESET**

**M1725** includes an internal power-on reset circuit. The power-on reset initializes and has an initialization period equal to 1024 system clock periods after  $V_{CC} > 2.2V$ . During the initialization period, the DAC outputs are invalid, and the analog outputs are forced to  $V_{CC}/2$ .

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.