TSC80251G1D

Extended 8–bit Microcontroller with Serial Communication Interfaces

1. Description

The TSC80251G1D products are derivatives of the TEMIC Microcontroller family based on the extended 8–bit C251 Architecture. This family of products is tailored to 8–bit microcontroller applications requiring an increased instruction throughput, a reduced operating frequency or a larger addressable memory space. The architecture can provide a significant code size reduction when compiling C programs while fully preserving the legacy of C51 assembly routines.

The TSC80251G1D derivatives are pin–out and software compatible with standard 80C51/Fx/Rx with extended on–chip data memory (1 Kbyte RAM) and up to 256 Kbytes of external code and data. Additionally, the TSC83251G1D provides on–chip code memory (16 Kbytes ROM).

They provide transparent enhancements to Intel's 8xC251Sx family with an additional Synchronous Serial Link Controller (SSLC supporting I^2C, µWire and SPI protocols), a Keyboard interrupt interface and Power Monitoring and Management features.

TSC80251G1D Mask ROM and ROMless derivatives are optimized both for speed and for low power consumption on a wide voltage range.

Notes:
This Datasheet provides the technical description of the TSC80251G1D derivatives. For further information on the device usage, please request the TSC80251 Programmers' Guide and the TSC80251G1D Design Guide.
For information on the EPROM/OTP devices, please refer to the TSC87251G1A Datasheet.

2. Typical Applications

- ISDN terminals
- High–Speed modems
- PABX (SOHO)
- Networking
- Line cards
- Computer peripherals
- Printers
- Plotters
- Scanners
- Banking machines
- Barcode readers
- Smart cards readers
- High–end digital monitors
- High–end joysticks

3. Features

- Pin–Out and software compatibility with standard 80C51 products and 80C51FA/FB/RA/RB
- Plug–in replacement of Intel's 80C251Sx
- C251 core: Intel's MCS® 251 step D compliance
  - 83 ns Instruction cycle time @ 24 MHz
  - 40–byte Register File
  - Registers Accessible as Bytes, Words or Dwords
  - Six–stage Instruction Pipeline
  - 16–bit Internal Code Fetch
- Enriched C51 Instruction Set
  - 16–bit and 32–bit ALU
  - Compare and Conditional Jump Instructions
  - Expanded Set of Move Instructions
- Linear Addressing
- 1 Kbyte of on–chip RAM
- External memory space (Code/Data) programmable from 64 Kbytes to 256 Kbytes
- TSC83251G1D: 16 Kbytes of on–chip masked ROM (Engineering and fast production with TSC87251G1A OTP/EPROM version)
- TSC80251G1D: ROMless version
- Four 8–bit parallel I/O Ports (Ports 0, 1, 2 and 3 of the standard 80C51)
- Serial I/O Port: full duplex UART (80C51 compatible) with independent Baud Rate Generator
- SSLC: Synchronous Serial Link Controller
  - I^2C multi–master and slave protocols
  - µWire and SPI master and slave protocols
- Three 16–bit Timers/Counters (Timers 0, 1 and 2 of the standard 80C51)
- EWC: Event and Waveform Controller
  - Compatible with Intel's Programmable Counter Array (PCA)
  - Common 16–bit Timer/Counter reference with four possible clock sources (Fosc/4, Fosc/12, Timer 1 and external input)
  - Five modules with four programmable modes:
    - 16–bit software Timer/Counter
    - 16–bit Timer/Counter Capture Input and software pulse measurement
    - High–speed output and 16–bit software Pulse Width Modulation (PWM)
    - 8–bit hardware PWM without overhead
  - 16–bit Watchdog Timer/Counter capability
- Secure 14–bit Hardware Watchdog Timer
- Power Monitoring and Management
  - Power–Fail reset
  - Power–On reset (integrated on the chip)
  - Power–Off flag (cold and warm resets)
  - Software programmable system clock
  - Idle and Power–Down modes
- Keyboard interrupt interface on Port 1
- Non Maskable Interrupt input (NMI)
- Real–time Wait states inputs (WAIT#/AWAIT#)
- On–chip Code Verify with Encryption for Mask ROM versions
- ONCE mode and full speed Real–Time In–Circuit Emulation support (Third Party Vendors)
- High speed versions:
  - 16 MHz and 24 MHz
  - 5 V ±10 %
  - Typical operating current: 34 mA @ 24 MHz
23 mA @ 16 MHz
  - Power–Down mode typical current ≤ 2 µA
- Low voltage version:
  - 2.7 V to 5.5 V
  - 12 MHz operation
  - Typical operating current: 8 mA @ 3 V
  - Power–Down mode typical current ≤ 1 µA
- Temperature ranges:
  - Commercial (0°C to +70°C)
  - Industrial (–40°C to +85°C)
  - Option: extended range (–55°C to +125°C)
- Packages:
  - PDIL 40, PLCC 44 and VQFP 44
  - Options: known good dice and ceramic packages

4. Block Diagram

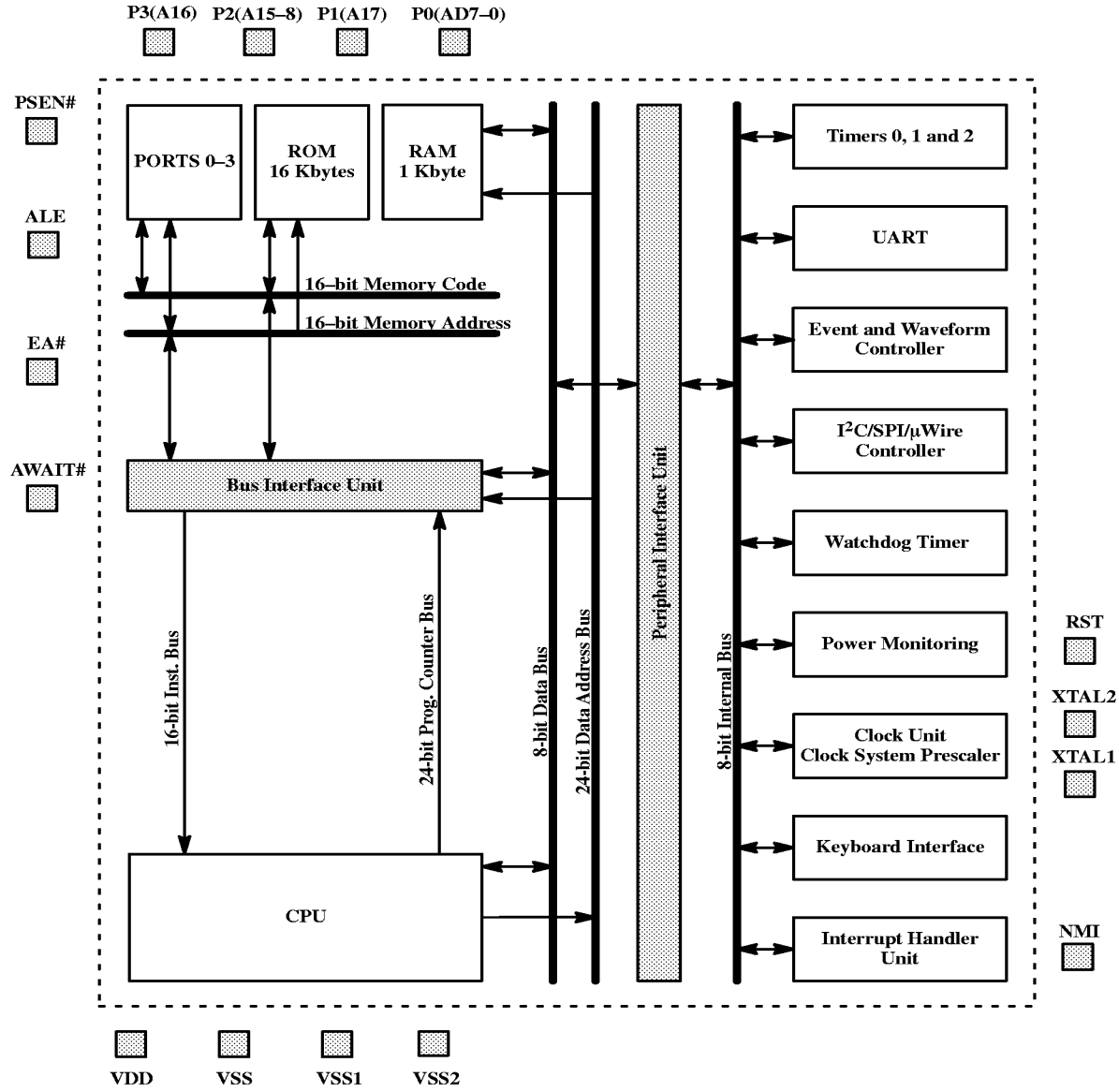


Figure 1. TSC80251G1D Block Diagram

5. Pin Description

5.1. Pinout

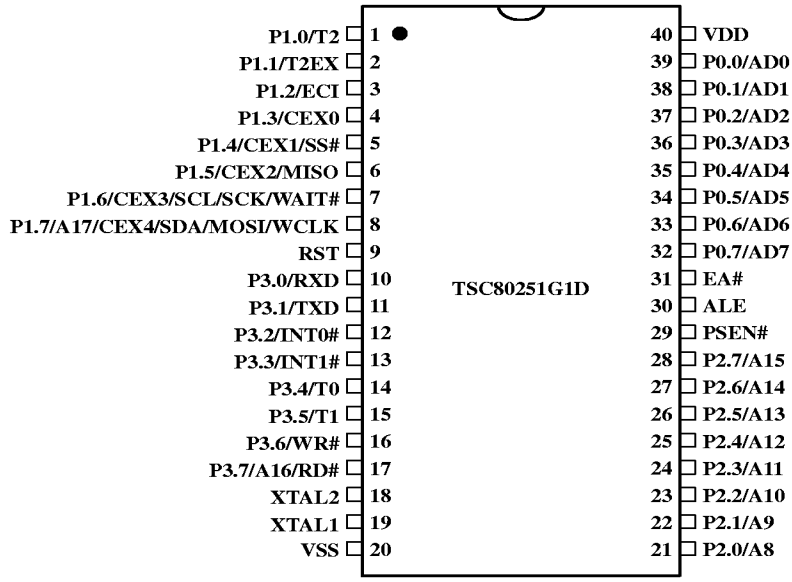


Figure 2. TSC80251G1D 40–pin DIP package

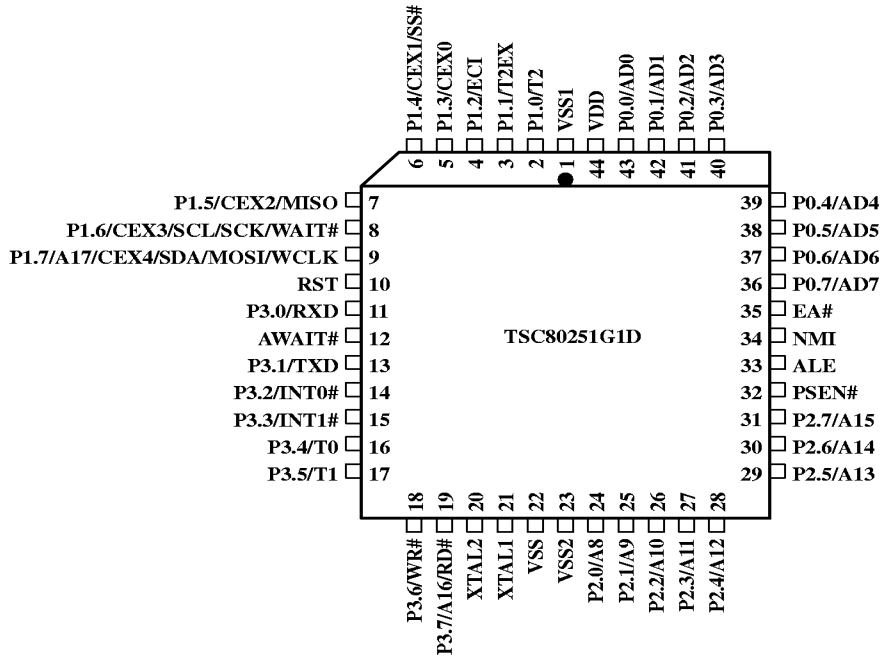


Figure 3. TSC80251G1D 44–pin PLCC Package

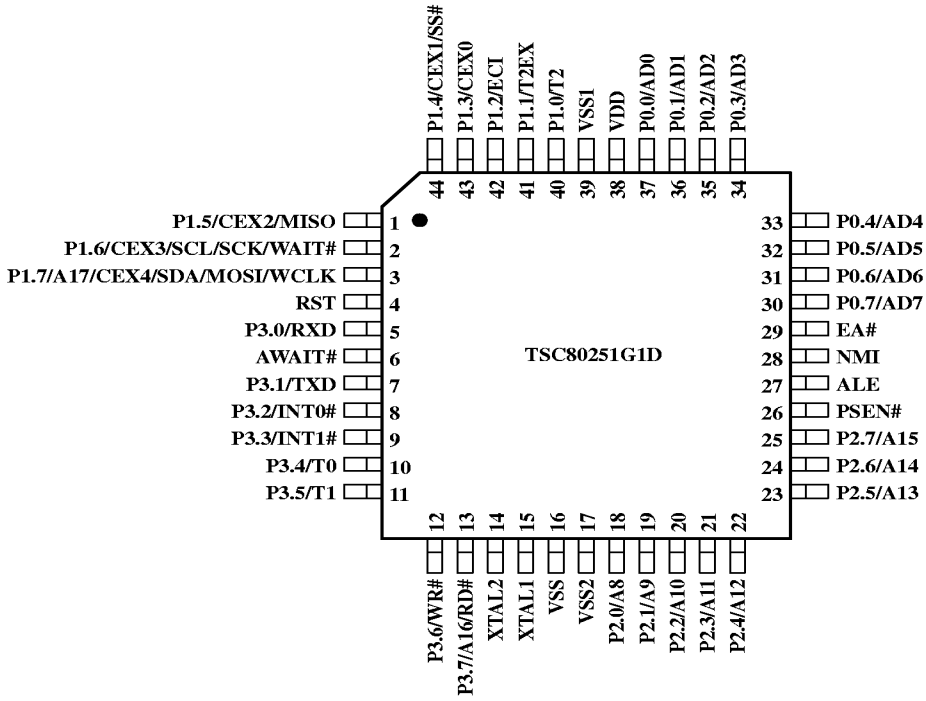


Figure 4. TSC80251G1D 44–pin VQFP Package

Table 1. TSC80251G1D Pin Assignment

DIP	PLCC	VQFP	Name	DIP	PLCC	VQFP	Name
	1	39	VSS1		23	17	VSS2
1	2	40	P1.0/T2	21	24	18	P2.0/A8
2	3	41	P1.1/T2EX	22	25	19	P2.1/A9
3	4	42	P1.2/ECI	23	26	20	P2.2/A10
4	5	43	P1.3/CEX0	24	27	21	P2.3/A11
5	6	44	P1.4/CEX1/SS#	25	28	22	P2.4/A12
6	7	1	P1.5/CEX2/MISO	26	29	23	P2.5/A13
7	8	2	P1.6/CEX3/SCL/SCK/WAIT#	27	30	24	P2.6/A14
8	9	3	P1.7/A17/CEX4/SDA/MOSI/WCLK	28	31	25	P2.7/A15
9	10	4	RST	29	32	26	PSEN#
10	11	5	P3.0/RXD	30	33	27	ALE
	12	6	AWAIT#		34	28	NMI
11	13	7	P3.1/TXD	31	35	29	EA#
12	14	8	P3.2/INT0#	32	36	30	P0.7/AD7
13	15	9	P3.3/INT1#	33	37	31	P0.6/AD6
14	16	10	P3.4/T0	34	38	32	P0.5/AD5
15	17	11	P3.5/T1	35	39	33	P0.4/AD4
16	18	12	P3.6/WR#	36	40	34	P0.3/AD3
17	19	13	P3.7/A16/RD#	37	41	35	P0.2/AD2
18	20	14	XTAL2	38	42	36	P0.1/AD1
19	21	15	XTAL1	39	43	37	P0.0/AD0
20	22	16	VSS	40	44	38	VDD

5.2. Signals

Table 2. TSC80251G1D Signal Descriptions

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see NO TAG).	P1.7
A16	O	**17th Address Bit** Output to memory as 17th external address bit (A16) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see NO TAG).	P3.7
A15:8(1)	O	**Address Lines** Upper address lines for the external bus.	P2.7:0
AD7:0(1)	I/O	**Address/Data Lines** Multiplexed lower address lines and data for the external memory.	P0.7:0
ALE	O	**Address Latch Enable** ALE signals the start of an external bus cycle and indicates that valid address information are available onlines A16/A17 and A7:0. An external latch can use ALE to demultiplex the address from address/databus.	
AWAIT#	I	**Real–time Asynchronous Wait States Input** When this pin is active (low level), the memory cycle is stretched until it becomes high. When using the TSC80251G1D as a pin–for–pin replacement for a 8xC51 product, AWAIT# can be unconnected without loss of compatibility or power consumption increase (on–chip pull–up). Not available on DIP package.	
CEX4:0	O	**PCA Input/Output pins** CEXx are input signals for the PCA capture mode and output signals for the PCA compare and PWM modes.	P1.7:3
EA#	I	**External Access Enable** EA# directs program memory accesses to on–chip or off–chip code memory. For EA#= 0, all program memory accesses are off-chip. For EA#= 1, an access is on-chip ROM if the address is within the range of the on–chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground.	
ECI	O	**PCA External Clock input** ECI is the external clock input to the 16–bit PCA timer.	P1.2
MISO	I/O	**SPI Master Input Slave Output line** When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.	P1.5
MOSI	I/O	**SPI Master Output Slave Input line** When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller.	P1.7
INT1:0#	I	**External Interrupts 0 and 1.** INT1#/INT0# inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits IT1:0 are cleared, bits IE1:0 are set by a low level on INT1#/INT0#	P3.3:2
NMI	I	**Non Maskable Interrupt** Holding this pin high for 24 oscillator periods triggers an interrupt. When using the TSC80251G1D as a pin–for–pin replacement for a 8xC51 product, NMI can be unconnected without loss of compatibility or power consumption increase (on–chip pull–down). Not available on DIP package.	
P0.0:7	I/O	**Port 0** P0 is an 8–bit open–drain bidirectional I/O port.	AD7:0

Signal Name	Type	Description	Alternate Function
P1.0:7	I/O	**Port 1** P1 is an 8–bit bidirectional I/O port with internal pull–ups. P1 provides interrupt capability for a keyboard interface.	
P2.0:7	I/O	**Port 2** P2 is an 8–bit bidirectional I/O port with internal pull–ups.	A15:8
P3.0:7	I/O	**Port 3** P3 is an 8–bit bidirectional I/O port with internal pull–ups.	
PSEN#	O	**Program Store Enable/Read signal output** PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see NO TAG).	
RD#	O	**Read or 17th Address Bit (A16)** Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see NO TAG).	P3.7
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power–Down mode returns the chip to normal operation.	
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial modes I/O 1, 2 and 3.	P3.0
SCL	I/O	**I^2C Serial Clock** When I^2C controller is in master mode, SCL outputs the serial clock to slave peripherals. When I^2C controller is in slave mode, SCL receives clock from the master controller.	P1.6
SCK	I/O	**SPI Serial Clock** When SPI is in master mode, SCK outputs clock to the slave peripheral. When SPI is in slave mode, SCK receives clock from the master controller.	P1.6
SDA	I/O	**I^2C Serial Data** SDA is the bidirectional I^2C data line.	P1.7
SS#	I	**SPI Slave Select Input** When in Slave mode, SS# enables the slave mode.	P1.4
T1:0	I/O	**Timer 1:0 External Clock Inputs** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	
T2	I/O	**Timer 2 Clock Input/Output** For the timer 2 capture mode, T2 is the external clock input. For the Timer 2 clock–out mode, T2 is the clock output.	P1.0
T2EX	I	**Timer 2 External Input** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto–reload mode, a falling edge causes the timer 2 register to be reloaded. In the up–down counter mode, this signal determines the count direction: 1= up, 0= down.	P1.1
TXD	I/O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1
VDD	PWR	**Digital Supply Voltage** Connect this pin to +5V or +3V supply voltage.	
VSS	GND	**Circuit Ground** Connect this pin to ground.	

Signal Name	Type	Description	Alternate Function
VSS1	GND	**Secondary Ground 1** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC80251G1D as a pin–for–pin replacement for a 8xC51 product, VSS1 can be unconnected without loss of compatibility. Not available on DIP package.	
VSS2	GND	**Secondary Ground 2** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC80251G1D as a pin–for–pin replacement for a 8xC51 product, VSS2 can be unconnected without loss of compatibility. Not available on DIP package.	
WAIT#	I	**Real–time Synchronous Wait States Input** The real–time WAIT# input is enabled by setting RTWE bit in WCON (S:A7h). During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal.	P1.6
WCLK	O	**Wait Clock Output** The real–time WCLK output is enabled by setting RTWCE bit in WCON (S:A7h). When enabled, the WCLK output produces a square wave signal with a period of one half the oscillator frequency.	P1.7
WR#	O	**Write** Write signal output to external memory.	P3.6
XTAL1	I	**Input to the on–chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	
XTAL2	O	**Output of the on–chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	

Note:

1. *The description of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the non–page mode chip configuration. If the chip is configured in page mode operation, port 0 carries the lower address bits (A7:0) while port 2 carries the upper address bits (A15:8) and the data (D7:0).*

6. Address Spaces

The TSC80251G1D implements four different address spaces:

- On–chip ROM program/code memory (not present in ROMless devices)
- On–chip RAM data memory
- Special Function Registers (SFRs)
- Configuration array

6.1. Program/Code Memory

The TSC83251G1D implements 16 Kbytes of on–chip program/code memory. Figure 5 shows the split of the internal and external program/code memory spaces. If EA# is tied to a high level, the 16–Kbyte on–chip program memory is mapped in the lower part of segment FF: where the C251 core jumps after reset. The rest of the program/code memory space is mapped to the external memory. If EA# is tied to a low level, the internal program/code memory is not used and all the accesses are directed to the external memory.

For the masked ROM products, the internal program/code is provided in a masked ROM. For the ROMless products, there is no possible internal program/code and EA# must be tied to a low level.

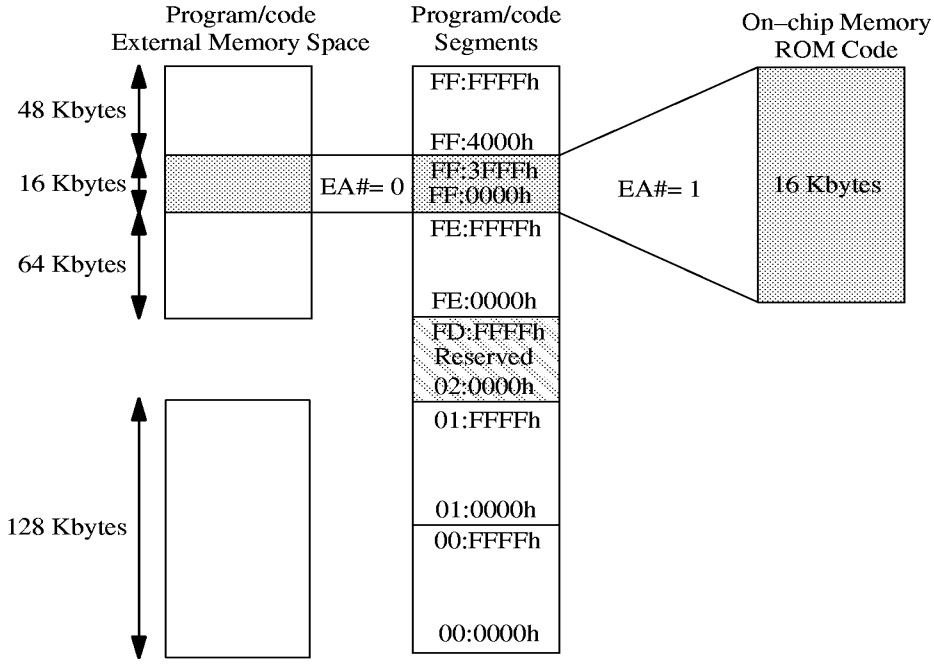


Figure 5. Program/Code Memory Mapping

Notes:
Special care should be taken when the Program Counter (PC) increments:
– *If the program executes exclusively from on–chip code memory (not from external memory), beware of executing code from the upper eight bytes of the on–chip ROM (FF:3FF8h–FF:3FFFFh). Because of its pipeline capability, the TSC80251G1D may attempt to prefetch code from external memory (at an address above FF:3FFFFh) and thereby disrupt I/O Ports 0 and 2. Fetching code constants from these 8 bytes does not affect Ports 0 and 2.*
– *When PC reaches the end of segment FF:, it loops to the reset address FF:0000h (for compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).*

6.2. Data Memory

The TSC80251G1D implements 1 Kbyte of on–chip data RAM. Figure 6 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on–chip RAM located from 20h to FFh is bit addressable. This on–chip RAM is not accessible through the program/code memory space.

For faster computation with the on–chip ROM code of the TSC83251G1D, its upper 8 Kbytes are also mapped in the upper part of the region 00: if the On–Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure 8). However, if EA# is tied to a low level, the TSC80251G1D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 8 Kbytes of the lower 16 Kbytes of the segment FF:). If EMAP# bit is set, the on–chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on–chip memory mapped onto are redirected to the external memory.

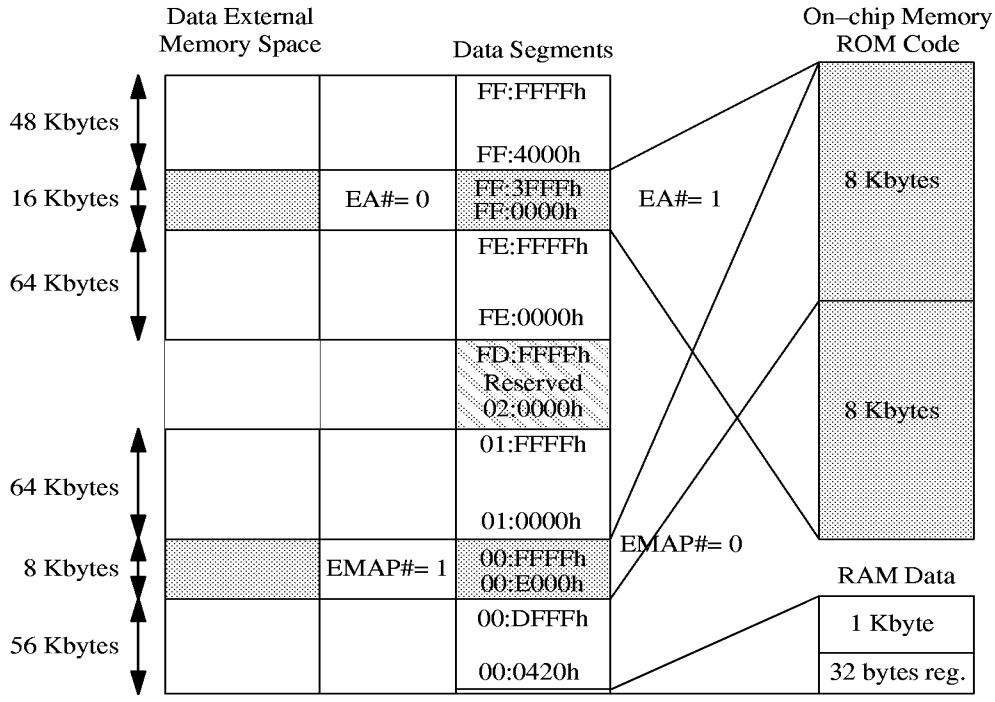


Figure 6. Data Memory Mapping

6.3. Special Function Registers

The Special Function Registers (SFRs) of the TSC80251G1D derivatives fall into the categories detailed in Table 3 to Table 11.

SFRs are placed in a reserved on–chip memory region S: which is not represented in the data memory mapping (Figure 6). The relative addresses within S: of these SFRs are provided together with their reset values in Table 12. They are upward compatible with the SFRs of the standard 80C51 and the Intel's 80C251Sx family. In this table, the C251 core registers are in italics and are described in the TSC80251 Programmer's Guide. The other SFRs are described in the TSC80251G1D Design Guide. All the SFRs are bit–addressable using the C251 instruction set.

Table 3. C251 Core SFRs

Mnemonic	Name	Mnemonic	Name
ACC(1)	Accumulator	SPH(1)	Stack Pointer High – MSB of SPX
B(1)	B Register	DPL(1)	Data Pointer Low byte – LSB of DPTR
PSW	Program Status Word	DPH(1)	Data Pointer High byte – MSB of DPTR
PSW1	Program Status Word 1	DPXL(1)	Data Pointer Extended Low byte of DPX – Region number
SP(1)	Stack Pointer – LSB of SPX		

Note:
1. These SFRs can also be accessed by their corresponding registers in the register file.

Table 4. I/O Port SFRs

Mnemonic	Name	Mnemonic	Name
P 0	Port 0	P 2	Port 2
P 1	Port 1	P 3	Port 3

Table 5. Timers SFRs

Mnemonic	Name	Mnemonic	Name
TL0	Timer/Counter 0 Low Byte	TMOD	Timer/Counter 0 and 1 Modes
TH0	Timer/Counter 0 High Byte	T2CON	Timer/Counter 2 Control
TL1	Timer/Counter 1 Low Byte	T2MOD	Timer/Counter 2 Mode
TH1	Timer/Counter 1 High Byte	RCAP2L	Timer/Counter 2 Reload/Capture Low Byte
TL2	Timer/Counter 2 Low Byte	RCAP2H	Timer/Counter 2 Reload/Capture High Byte
TH2	Timer/Counter 2 High Byte	WDTRST	WatchDog Timer Reset
TCON	Timer/Counter 0 and 1 Control		

Table 6. Serial I/O Port SFRs

Mnemonic	Name	Mnemonic	Name
SCON	Serial Control	SADDR	Slave Address
SBUF	Serial Data Buffer	BRL	Baud Rate Reload
SADEN	Slave Address Mask	BDRCON	Baud Rate Control

Table 7. SSLC SFRs

Mnemonic	Name	Mnemonic	Name
SSCON	Synchronous Serial control	SSADR	Synchronous Serial Address
SSDAT	Synchronous Serial Data	SSBR	Synchronous Serial Bit Rate
SSCS	Synchronous Serial Control and Status		

Table 8. Event Waveform Control SFRs

Mnemonic	Name	Mnemonic	Name
CCON	EWC–PCA Timer/Counter Control	CCAP1L	EWC–PCA Compare Capture Module 1 Low Register
CMOD	EWC–PCA Timer/Counter Mode	CCAP2L	EWC–PCA Compare Capture Module 2 Low Register
CL	EWC–PCA Timer/Counter Low Register	CCAP3L	EWC–PCA Compare Capture Module 3 Low Register
CH	EWC–PCA Timer/Counter High Register	CCAP4L	EWC–PCA Compare Capture Module 4 Low Register
CCAPM0	EWC–PCA Timer/Counter Mode 0	CCAP0H	EWC–PCA Compare Capture Module 0 High Register
CCAPM1	EWC–PCA Timer/Counter Mode 1	CCAP1H	EWC–PCA Compare Capture Module 1 High Register
CCAPM2	EWC–PCA Timer/Counter Mode 2	CCAP2H	EWC–PCA Compare Capture Module 2 High Register
CCAPM3	EWC–PCA Timer/Counter Mode 3	CCAP3H	EWC–PCA Compare Capture Module 3 High Register
CCAPM4	EWC–PCA Timer/Counter Mode 4	CCAP4H	EWC–PCA Compare Capture Module 4 High Register
CCAP0L	EWC–PCA Compare Capture Module 0 Low Register		

Table 9. System Management SFRs

Mnemonic	Name	Mnemonic	Name
PCON	Power Control	CKRL	Clock Reload
POWM	Power Management	WCON	Synchronous Real–Time Wait State Control
PFILT	Power Filter		

Table 10. Interrupt SFRs

Mnemonic	Name	Mnemonic	Name
IE0	Interrupt Enable Control 0	IPL0	Interrupt Priority Control Low 0
IE1	Interrupt Priority Control 1	IPH1	Interrupt Priority Control High 1
IPH0	Interrupt Priority Control High 0	IPL1	Interrupt Priority Control Low 1

Table 11. Keyboard Interface SFRs

Mnemonic	Name	Mnemonic	Name
P1IE	Port 1 Input Interrupt Enable	P1LS	Port 1 Level Selection
P1F	Port 1 Flag		

Table 12. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B(1) 0000 0000								F7h
E8h		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC(1) 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW(1) 0000 0000	PSW1(1) 0000 0000							D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IPL0 X000 0000	SADEN 0000 0000					SPH(1) 0000 0000		BFh
B0h	P3 1111 1111	IE1 XX0X XXX0	IPL1 XX0X XXX0	IPH1 XX0X XXX0				IPH0 X000 0000	B7h
A8h	IE0 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111						WDTRST 1111 1111	WCON XXXX XX00	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	P1LS 0000 0000	P1IE 0000 0000	P1F 0000 0000		9Fh
90h	P1 1111 1111		SSBR 0000 0000	SSCON (2)	SSCS (3)	SSDAT 0000 0000	SSADR 0000 0000		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	CKRL 0000 1000	POWM 0XXX 0XXX	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL(1) 0000 0000	DPH(1) 0000 0000	DPXL(1) 0000 0001		PFILT XXXX XXXX	PCON 0000 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

Notes:

1. *These registers are described in the TSC80251 Programmer's Guide (C251 core registers).*
2. *In I^2C and SPI modes, SSCON is splitted in two separate registers. SSCON reset value is 0000 0000 in I^2C mode and 0000 0100 in SPI mode.*
3. *In read and write modes, SSCS is splitted in two separate registers. SSCS reset value is 1111 1000 in read mode and 0000 0000 in write mode.*

6.4. Configuration Bytes

The TSC80251G1D derivatives provide user design flexibility by configuring certain operating features at device reset. These features fall into the following categories:

- external memory interface (page mode, address bits, programmed wait states and the address range for RD#, WR#, and PSEN#)
- source mode/binary mode opcodes
- selection of bytes stored on the stack by an interrupt
- mapping of the upper portion of on–chip code memory to region 00:

Two user configuration bytes UCONFIG0 (see Figure 7) and UCONFIG1 (see Figure 8) provide the information.

When EA# is tied to a low level, the configuration bytes are fetched from the external address space. The TSC80251G1D derivatives reserve the top eight bytes of the memory address space (FF:FFF8h-FF:FFFFh) for an external 8–byte configuration array. Only two bytes are actually used: UCONFIG0 at FF:FFF8h and UCONFIG1 at FF:FFF9h.

For the mask ROM devices, configuration information is stored in on–chip memory (see ROM Verifying). When EA# is tied to a high level, the configuration information is retrieved from the on–chip memory instead of the external address space and there is no restriction in the usage of the external memory.

UCONFIG0
Configuration Byte 0

7	6	5	4	3	2	1	0
–	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Description
7	–	**Reserved** Set this bit when writing to UCONFIG0.
6	WSA1#	**Wait State A bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (all regions except 01:). WSA1# WSA0# Number of wait states 0 0 3 0 1 2 1 0 1 1 1 0
5	WSA0#	
4	XALE#	**Extend ALE bit** Clear to extend the duration of the ALE pulse from T_{OSC} to $3 \times T_{OSC}$. Set to minimize the duration of the ALE pulse to $1 \times T_{OSC}$.
3	RD1	**Memory Signal Select bits** Specify a 18–bit, 17–bit or 16–bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13).
2	RD0	
1	PAGE#	**Page Mode Select bit**(1) Clear to select the faster page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0. Set to select the non–page mode(2) with A15:8 on Port 2 and A7:0/D7:0 on Port 0.
0	SRC	**Source Mode/Binary Mode Select bit** Clear to select the binary mode. Set to select the source mode.

Notes:
1. *UCONFIG0 is fetched twice so it can be properly read both in Page or Non–Page modes. If P2.1 is cleared during the first data phase, a page mode configuration is used, otherwise the subsequent fetches are performed in Non–Page mode.*
2. *This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.*

Figure 7. Configuration Byte 0

UCONFIG1
Configuration Byte 1

7	6	5	4	3	2	1	0
–	–	–	INTR	WSB	WSB1#	WSB0#	EMAP#

Bit Number	Bit Mnemonic	Description
7	–	**Reserved** Set this bit when writing to UCONFIG1.
6	–	**Reserved** Set this bit when writing to UCONFIG1.
5	–	**Reserved** Set this bit when writing to UCONFIG1.
4	INTR	**Interrupt Mode bit**(1) Clear so that the interrupts push two bytes onto the stack (the two lower bytes of the PC register). Set so that the interrupts push four bytes onto the stack (the three bytes of the PC register and the PSW1 register).
3	WSB	**Wait State B bit**(2) Clear to generate one wait state for memory region 01:. Set for no wait states for memory region 01:.
2	WSB1#	**Wait State B bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (only region 01:). WSB1# WSB0# Number of wait states 0 0 3 0 1 2 1 0 1 1 1 0
1	WSB0#	
0	EMAP#	**On–Chip Code Memory Map bit** Clear to map the upper 8 Kbytes of on–chip code memory (at FF:2000h–FF:3FFFh) to the data space (at 00:E000h–00:FFFFh). Set not to map the upper 8 Kbytes of on–chip code memory (at FF:2000h–FF:3FFFh) to the data space.

Notes:
1. *Two or four bytes are transparently popped according to INTR when using the RETI instruction. INTR must be set if interrupts are used with code executing outside region FF:.*
2. *Use only for Step A compatibility; set this bit when WSB1:0# are used.*

Figure 8. Configuration Byte 1

Table 13. Address Ranges and Usage of RD#, WR# and PSEN# Signals

RD1	RD0	P1.7	P3.7/RD#	PSEN#	WR#	External Memory
0	0	A17	A16	Read signal for all external memory locations	Write signal for all external memory locations	256 Kbytes
0	1	I/O pin	A16	Read signal for all external memory locations	Write signal for all external memory locations	128 Kbytes
1	0	I/O pin	I/O pin	Read signal for all external memory locations	Write signal for all external memory locations	64 Kbytes
1	1	I/O pin	Read signal for regions 00: and 01:	Read signal for regions FE: and FF:	Write signal for all external memory locations	2 × 64 Kbytes(1)

Note:
1. *This selection provides compatibility with the standard 80C51 hardware which has separate external memory spaces for data and code.*

7. Instruction Set Summary

This section contains tables that summarize the instruction set. For each instruction there is a short description, its length in bytes, and its execution time in states (one state time is equal to two system clock cycles). There are two concurrent processes limiting the effective instruction throughput:

- Instruction Fetch
- Instruction Execution

Table 20 to Table 34 assume code executing from on–chip memory, then the CPU is fetching 16–bit at a time and this is never limiting the execution speed.

If the code is fetched from external memory, a pre–fetch queue will store instructions ahead of execution to optimize the memory bandwidth usage when slower instructions are executed. However, the effective speed may be limited depending on the average size of instructions (for the considered section of the program flow). The maximum average instruction throughput is provided by Table 14 depending on the external memory configuration (from Page Mode to Non–Page Mode and the maximum number of wait states). If the average size of instructions is not an integer, the maximum effective throughput is found by pondering the number of states for the neighbor integer values.

Table 14. Minimum Number of States per Instruction for given Average Sizes

Average size of Instructions (bytes)	Page Mode (states)	Non–Page Mode (states)				
		0 Wait State	1 Wait State	2 Wait States	3 Wait States	4 Wait States
1	1	2	3	4	5	6
2	2	4	6	8	10	12
3	3	6	9	12	15	18
4	4	8	12	16	20	24
5	5	10	15	20	25	30

If the average execution time of the considered instructions is larger than the number of states given by Table 14, this larger value will prevail as the limiting factor. Otherwise, the value from Table 14 must be taken. This is providing a fair estimation of the execution speed but only the actual code execution can provide the final value.

7.1. Notation for Instruction Operands

Table 15 to Table 19 provide Notation for Instruction Operands.

Table 15. Notation for Direct Addressing

Direct Address	Description	C251	C51
dir8	A direct 8-bit address. This can be a memory address (00h-7Fh) or a SFR address (80h-FFh). It is a byte (default), word or double word depending on the other operand.	✓	✓
dir16	A 16-bit memory address (00:0000h-00:FFFFh) used in direct addressing.	✓	

Table 16. Notation for Immediate Addressing

Immediate Address	Description	C251	C51
#data	An 8-bit constant that is immediately addressed in an instruction	✓	✓
#data16	A 16-bit constant that is immediately addressed in an instruction	✓	
#0data16 #1data16	A 32-bit constant that is immediately addressed in an instruction. The upper word is filled with zeros (#0data16) or ones (#1data16).	✓	
#short	A constant, equal to 1, 2, or 4, that is immediately addressed in an instruction.	✓	

Table 17. Notation for Bit Addressing

Direct Address	Description	C251	C51
bit51	A directly addressed bit (bit number= 00h-FFh) in memory or an SFR. Bits 00h-7Fh are the 128 bits in byte locations 20h-2Fh in the on-chip RAM. Bits 80h-FFh are the 128 bits in the 16 SFRs with addresses that end in 0h or 8h, S:80h, S:88h, S:90h,..., S:F0h, S:F8h.		✓
bit	A directly addressed bit in memory locations 00:0020h-00:007Fh or in any defined SFR.	✓	

Table 18. Notation for Destination in Control Instructions

Direct Address	Description	C251	C51
rel	A signed (two's complement) 8-bit relative address. The destination is –128 to +127 bytes relative to the next instruction's first byte.	✓	✓
addr11	An 11-bit target address. The target is in the same 2-Kbyte block of memory as the next instruction's first byte.		✓
addr16	A 16-bit target address. The target can be anywhere within the same 64-Kbyte region as the next instruction's first byte.		✓
addr24	A 24-bit target address. The target can be anywhere within the 16–Mbyte address space.	✓	

Table 19. Notation for Register Operands

Register	Description	C251	C51
@Ri	A memory location (00h-FFh) addressed indirectly via byte registers R0 or R1		✓
Rn n	Byte register R0-R7 of the currently selected register bank Byte register index: n= 0-7		✓
Rm Rmd Rms m, md, ms	Byte register R0-R15 of the currently selected register file Destination register Source register Byte register index: m, md, ms= 0-15	✓	
WRj WRjd WRjs @WRj @WRj +dis16 j, jd, js	Word register WR0, WR2, ..., WR30 of the currently selected register file Destination register Source register A memory location (00:0000h-00:FFFFh) addressed indirectly through word register WR0-WR30, is the target address for jump instructions. A memory location (00:0000h-00:FFFFh) addressed indirectly through word register (WR0-WR30) + 16–bit signed (two's complement) displacement value Word register index: j, jd, js= 0-30	✓	
DRk DRkd DRks @DRk @DRk +dis16 k, kd, ks	Dword register DR0, DR4, ..., DR28, DR56, DR60 of the currently selected register file Destination register Source register A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register DR0-DR28, DR56 and DR60, is the target address for jump instruction A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register (DR0-DR28, DR56, DR60) + 16–bit (two's complement) signed displacement value Dword register index: k, kd, ks= 0, 4, 8..., 28, 56, 60	✓	

7.2. Size and Execution Time for Instruction Families

Table 20. Summary of Add and Subtract Instructions

Add	ADD <dest>, <src>	dest opnd ← dest opnd + src opnd
Subtract	SUB <dest>, <src>	dest opnd ← dest opnd – src opnd
Add with Carry	ADDC <dest>, <src>	(A) ← (A) + src opnd + (CY)
Subtract with Borrow	SUBB <dest>, <src>	(A) ← (A) – src opnd – (CY)

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ADD	A, Rn	Register to ACC	1	1	2	2
	A, dir8	Direct address to ACC	2	1[2]	2	1[2]
	A, @Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
ADD / SUB	Rmd, Rms	Byte register to/from byte register	3	2	2	1
	WRjd, WRjs	Word register to/from word register	3	3	2	2
	DRkd, DRks	Dword register to/from dword register	3	5	2	4
	Rm, #data	Immediate 8-bit data to/from byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to/from word register	5	4	4	3
	DRk, #0data16	16-bit unsigned immediate data to/from dword register	5	6	4	5
	Rm, dir8	Direct address (on–chip RAM or SFR) to/from byte register	4	3[2]	3	2[2]
	WRj, dir8	Direct address (on–chip RAM or SFR) to/from word register	4	4	3	3
	Rm, dir16	Direct address (64K) to/from byte register	5	3[3]	4	2[3]
	WRj, dir16	Direct address (64K) to/from word register	5	4[4]	4	3[4]
	Rm, @WRj	Indirect address (64K) to/from byte register	4	3[3]	3	2[3]
	Rm, @DRk	Indirect address (16M) to/from byte register	4	4[3]	3	3[3]
ADDC / SUBB	A, Rn	Register to/from ACC with carry	1	1	2	2
	A, dir8	Direct address (on–chip RAM or SFR) to/from ACC with carry	2	1[2]	2	1[2]
	A, @Ri	Indirect address to/from ACC with carry	1	2	2	3
	A, #data	Immediate data to/from ACC with carry	2	1	2	1

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
3. *If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).*
4. *If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).*

Table 21. Summary of Increment and Decrement Instructions

Increment	INC <dest>	dest opnd ← dest opnd + 1
Increment	INC <dest>, <src>	dest opnd ← dest opnd + src opnd
Decrement	DEC <dest>	dest opnd ← dest opnd – 1
Decrement	DEC <dest>, <src>	dest opnd ← dest opnd – src opnd

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
INC DEC	A	ACC by 1	1	1	1	1
	Rn	Register by 1	1	1	2	2
	dir8	Direct address (on–chip RAM or SFR) by 1	2	2(2)	2	2(2)
	@Ri	Indirect address by 1	1	3	2	4
INC DEC	Rm, #short	Byte register by 1, 2, or 4	3	2	2	1
	WRj, #short	Word register by 1, 2, or 4	3	2	2	1
INC	DRk, #short	Double word register by 1, 2, or 4	3	4	2	3
DEC	DRk, #short	Double word register by 1, 2, or 4	3	5	2	4
INC	DPTR	Data pointer by 1	1	1	1	1

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.*

Table 22. Summary of Compare Instructions

Compare	CMP <dest>, <src>	dest opnd – src opnd

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
CMP	Rmd, Rms	Register with register	3	2	2	1
	WRjd, WRjs	Word register with word register	3	3	2	2
	DRkd, DRks	Dword register with dword register	3	5	2	4
	Rm, #data	Register with immediate data	4	3	3	2
	WRj, #data16	Word register with immediate 16-bit data	5	4	4	3
	DRk, #0data16	Dword register with zero-extended 16-bit immediate data	5	6	4	5
	DRk, #1data16	Dword register with one-extended 16-bit immediate data	5	6	4	5
	Rm, dir8	Direct address (on–chip RAM or SFR) with byte register	4	3(1)	3	2(1)
	WRj, dir8	Direct address (on–chip RAM or SFR) with word register	4	4	3	3
	Rm, dir16	Direct address (64K) with byte register	5	3(2)	4	2(2)
	WRj, dir16	Direct address (64K) with word register	5	4(3)	4	3(3)
	Rm, @WRj	Indirect address (64K) with byte register	4	3(2)	3	2(2)
	Rm, @DRk	Indirect address (16M) with byte register	4	4(2)	3	3(2)

Notes:
1. *If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
2. *If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).*
3. *If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).*

Table 23. Summary of Logical Instructions (1/2)

Logical AND[1]	ANL <dest>, <src>	dest opnd ← dest opnd Λ src opnd
Logical OR[1]	ORL <dest>, <src>	dest opnd ← dest opnd V src opnd
Logical Exclusive OR[1]	XRL <dest>, <src>	dest opnd ← dest opnd ∀ src opnd
Clear[1]	CLR A	(A) ← 0
Complement[1]	CPL A	(A) ← ∅ (A)
Rotate Left	RL A	$(A)_{n+1} \leftarrow (A)_n$, n= 0..6 $(A)_0 \leftarrow (A)_7$
Rotate Left Carry	RLC A	$(A)_{n+1} \leftarrow (A)_n$, n= 0..6 $(CY) \leftarrow (A)_7$ $(A)_0 \leftarrow (CY)$
Rotate Right	RR A	$(A)_{n-1} \leftarrow (A)_n$, n= 7..1 $(A)_7 \leftarrow (A)_0$
Rotate Right Carry	RRC A	$(A)_{n-1} \leftarrow (A)_n$, n= 7..1 $(CY) \leftarrow (A)_0$ $(A)_7 \leftarrow (CY)$

Mnemonic	<dest>, <src>[2]	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ANL ORL XRL	A, Rn	register to ACC	1	1	2	2
	A, dir8	Direct address (on–chip RAM or SFR) to ACC	2	1[3]	2	1[3]
	A, @Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
	dir8, A	ACC to direct address	2	2[4]	2	2[4]
	dir8, #data	Immediate 8–bit data to direct address	3	3[4]	3	3[4]
	Rmd, Rms	Byte register to byte register	3	2	2	1
	WRjd, WRjs	Word register to word register	3	3	2	2
	Rm, #data	Immediate 8-bit data to byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to word register	5	4	4	3
	Rm, dir8	Direct address to byte register	4	3[3]	3	2[3]
	WRj, dir8	Direct address to word register	4	4	3	3
	Rm, dir16	Direct address (64K) to byte register	5	3[5]	4	2[5]
	WRj, dir16	Direct address (64K) to word register	5	4[6]	4	3[6]
	Rm, @WRj	Indirect address (64K) to byte register	4	3[5]	3	2[5]
	Rm, @DRk	Indirect address (16M) to byte register	4	4[5]	3	3[5]
CLR	A	Clear ACC	1	1	1	1
CPL	A	Complement ACC	1	1	1	1
RL	A	Rotate ACC left	1	1	1	1
RLC	A	Rotate ACC left through CY	1	1	1	1
RR	A	Rotate ACC right	1	1	1	1
RRC	A	Rotate ACC right through CY	1	1	1	1

Notes:

1. *Logical instructions that affect a bit are in Table 29.*
2. *A shaded cell denotes an instruction in the C51 Architecture.*
3. *If this instruction addresses an I/O Port (Px, x= 0–3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
4. *If this instruction addresses an I/O Port (Px, x= 0–3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.*
5. *If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).*
6. *If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).*

Table 24. Summary of Logical Instructions (2/2)

Shift Left Logical	SLL <dest>	$<dest>_0 \leftarrow 0$ $<dest>_{n+1} \leftarrow <dest>_n$, n= 0..msb–1 (CY) ← $<dest>_{msb}$
Shift Right Arithmetic	SRA <dest>	$<dest>_{msb} \leftarrow <dest>_{msb}$ $<dest>_{n-1} \leftarrow <dest>_n$, n= msb..1 (CY) ← $<dest>_0$
Shift Right Logical	SRL <dest>	$<dest>_{msb} \leftarrow 0$ $<dest>_{n-1} \leftarrow <dest>_n$, n= msb..1 (CY) ← $<dest>_0$
Swap	SWAP A	$A_{3:0} \leftrightarrow A_{7:4}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
SLL	Rm	Shift byte register left through the MSB	3	2	2	1
	WRj	Shift word register left through the MSB	3	2	2	1
SRA	Rm	Shift byte register right	3	2	2	1
	WRj	Shift word register right	3	2	2	1
SRL	Rm	Shift byte register left	3	2	2	1
	WRj	Shift word register left	3	2	2	1
SWAP	A	Swap nibbles within ACC	1	2	1	2

Note:
1. A shaded cell denotes an instruction in the C51 Architecture.

Table 25. Summary of Multiply, Divide and Decimal-adjust Instructions

Multiply	MUL AB MUL <dest>, <src>	(B:A) ← (A)×(B) extended dest opnd ← dest opnd × src opnd
Divide	DIV AB	(A) ← Quotient ((A)/(B)) (B) ← Remainder ((A)/(B))
Divide	DIV <dest>, <src>	ext. dest opnd high ← Quotient (dest opnd/src opnd) ext. dest opnd low ← Remainder (dest opnd/src opnd)
Decimal-adjust ACC for Addition (BCD)	DA A	IF [[$(A)_{3:0} > 9$] ∨ [(AC)= 1]] THEN $(A)_{3:0} \leftarrow (A)_{3:0} + 6$!affects CY; IF [[$(A)_{7:4} > 9$] ∨ [(CY)= 1]] THEN $(A)_{7:4} \leftarrow (A)_{7:4} + 6$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MUL	AB	Multiply A and B	1	5	1	5
	Rmd, Rms	Multiply byte register and byte register	3	6	2	5
	WRjd, WRjs	Multiply word register and word register	3	12	2	11
DIV	AB	Divide A and B	1	10	1	10
	Rmd, Rms	Divide byte register and byte register	3	11	2	10
	WRjd, WRjs	Divide word register and word register	3	21	2	20
DA	A	Decimal adjust ACC	1	1	1	1

Note:
1. A shaded cell denotes an instruction in the C51 Architecture.

Table 26. Summary of Move Instructions (1/3)

Move to High word	MOVH <dest>, <src>	dest opnd$_{31:16}$ ← src opnd
Move with Sign extension	MOVS <dest>, <src>	dest opnd ← src opnd with sign extend
Move with Zero extension	MOVZ <dest>, <src>	dest opnd ← src opnd with zero extend
Move Code	MOVC A, <src>	(A) ← src opnd
Move eXtended	MOVX <dest>, <src>	dest opnd ← src opnd

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MOVH	DRk, #data16	16-bit immediate data into upper word of dword register	5	3	4	2
MOVS	WRj, Rm	Byte register to word register with sign extension	3	2	2	1
MOVZ	WRj, Rm	Byte register to word register with zeros extension	3	2	2	1
MOVC	A, @A +DPTR	Code byte relative to DPTR to ACC	1	6(3)	1	6(3)
	A, @A +PC	Code byte relative to PC to ACC	1	6(3)	1	6(3)
MOVX	A, @Ri	Extended memory (8-bit address) to ACC(2)	1	4	1	5
	A, @DPTR	Extended memory (16-bit address) to ACC(2)	1	3(4)	1	3(4)
	@Ri, A	ACC to extended memory (8-bit address)(2)	1	4	1	4
	@DPTR, A	ACC to extended memory (16-bit address)(2)	1	4(3)	1	4(3)

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *Extended memory addressed is in the region specified by DPXL (reset value= 01h).*
3. *If this instruction addresses external memory location, add N+1 to the number of states (N: number of wait states).*
4. *If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).*

Table 27. Summary of Move Instructions (2/3)

Move(1)	MOV <dest>, <src>	dest opnd ← src opnd

Mnemonic	<dest>, <src>(2)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MOV	A, Rn	Register to ACC	1	1	2	2
	A, dir8	Direct address (on–chip RAM or SFR) to ACC	2	1(3)	2	1(3)
	A, @Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
	Rn, A	ACC to register	1	1	2	2
	Rn, dir8	Direct address (on–chip RAM or SFR) to register	2	1(3)	3	2(3)
	Rn, #data	Immediate data to register	2	1	3	2
	dir8, A	ACC to direct address	2	2(3)	2	2(3)
	dir8, Rn	Register to direct address	2	2(3)	3	3(3)
	dir8, dir8	Direct address to direct address	3	3(4)	3	3(4)
	dir8, @Ri	Indirect address to direct address	2	3(3)	3	4(3)
	dir8, #data	Immediate data to direct address	3	3(3)	3	3(3)
	@Ri, A	ACC to indirect address	1	3	2	4
	@Ri, dir8	Direct address to indirect address	2	3(3)	3	4(3)
	@Ri, #data	Immediate data to indirect address	2	3	3	4
	DPTR, #data16	Load Data Pointer with a 16-bit constant	3	2	3	2

Notes:
1. *Instructions that move bits are in Table 29.*
2. *Move instructions from the C51 Architecture.*
3. *If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
4. *Apply note 3 for each dir8 operand.*

Table 28. Summary of Move Instructions (3/3)

Move[1]	MOV <dest>, <src>	dest opnd ← src opnd				
Mnemonic	**<dest>, <src>[2]**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
MOV	Rmd, Rms	Byte register to byte register	3	2	2	1
	WRjd, WRjs	Word register to word register	3	2	2	1
	DRkd, DRks	Dword register to dword register	3	3	2	2
	Rm, #data	Immediate 8-bit data to byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to word register	5	3	4	2
	DRk, #0data16	zero-ext 16bit immediate data to dword register	5	5	4	4
	DRk, #1data16	one-ext 16bit immediate data to dword register	5	5	4	4
	Rm, dir8	Direct address to byte register	4	3[3]	3	2[3]
	WRj, dir8	Direct address to word register	4	4	3	3
	DRk, dir8	Direct address to dword register	4	6	3	5
	Rm, dir16	Direct address (64K) to byte register	5	3[4]	4	2[4]
	WRj, dir16	Direct address (64K) to word register	5	4[5]	4	3[5]
	DRk, dir16	Direct address (64K) to dword register	5	6[6]	4	5[6]
	Rm, @WRj	Indirect address (64K) to byte register	4	3[4]	3	2[4]
	Rm, @DRk	Indirect address (16M) to byte register	4	4[4]	3	3[4]
	WRjd, @WRjs	Indirect address (64K) to word register	4	4[5]	3	3[5]
	WRj, @DRk	Indirect address (16M) to word register	4	5[5]	3	4[5]
	dir8, Rm	Byte register to direct address	4	4[3]	3	3[3]
	dir8, WRj	Word register to direct address	4	5	3	4
	dir8, DRk	Dword register to direct address	4	7	3	6
	dir16, Rm	Byte register to direct address (64K)	5	4[4]	4	3[4]
	dir16, WRj	Word register to direct address (64K)	5	5[5]	4	4[5]
	dir16, DRk	Dword register to direct address (64K)	5	7[6]	4	6[6]
	@WRj, Rm	Byte register to indirect address (64K)	4	4[4]	3	3[4]
	@DRk, Rm	Byte register to indirect address (16M)	4	5[4]	3	4[4]
	@WRjd, WRjs	Word register to indirect address (64K)	4	5[5]	3	4[5]
	@DRk, WRj	Word register to indirect address (16M)	4	6[5]	3	5[5]
	Rm, @WRj +dis16	Indirect with 16–bit dis (64K) to byte register	5	6[4]	4	5[4]
	WRj, @WRj +dis16	Indirect with 16–bit dis (64K) to word register	5	7[5]	4	6[5]
	Rm, @DRk +dis24	Indirect with 16–bit dis (16M) to byte register	5	7[4]	4	6[4]
	WRj, @WRj +dis24	Indirect with 16–bit dis (16M) to word register	5	8[5]	4	7[5]
	@WRj +dis16, Rm	Byte register to indirect with 16–bit dis (64K)	5	6[4]	4	5[4]
	@WRj +dis16, WRj	Word register to indirect with 16–bit dis (64K)	5	7[5]	4	6[5]
	@DRk +dis24, Rm	Byte register to indirect with 16–bit dis (16M)	5	7[4]	4	6[4]
	@DRk +dis24, WRj	Word register to indirect with 16–bit dis (16M)	5	8[5]	4	7[5]

Notes:
1. *Instructions that move bits are in Table 29.*
2. *Move instructions unique to the C251 Architecture.*
3. *If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
4. *If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).*
5. *If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).*
6. *If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).*

Table 29. Summary of Bit Instructions

Clear Bit	CLR <dest>	dest opnd ← 0
Set Bit	SETB <dest>	dest opnd ← 1
Complement Bit	CPL <dest>	dest opnd ← ∅ bit
AND Carry with Bit	ANL CY, <src>	(CY) ← (CY) ∧ src opnd
AND Carry with Complement of Bit	ANL CY, /<src>	(CY) ← (CY) ∧ ∅ src opnd
OR Carry with Bit	ORL CY, <src>	(CY) ← (CY) ∨ src opnd
OR Carry with Complement of Bit	ORL CY, /<src>	(CY) ← (CY) ∨ ∅ src opnd
Move Bit to Carry	MOV CY, <src>	(CY) ← src opnd
Move Bit from Carry	MOV <dest>, CY	dest opnd ← (CY)

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
CLR	CY	Clear carry	1	1	1	1
	bit51	Clear direct bit	2	2(3)	2	2(3)
	bit	Clear direct bit	4	4(3)	3	3(3)
SETB	CY	Set carry	1	1	1	1
	bit51	Set direct bit	2	2(3)	2	2(3)
	bit	Set direct bit	4	4(3)	3	3(3)
CPL	CY	Complement carry	1	1	1	1
	bit51	Complement direct bit	2	2(3)	2	2(3)
	bit	Complement direct bit	4	4(3)	3	3(3)
ANL	CY, bit51	And direct bit to carry	2	1(2)	2	1(2)
	CY, bit	And direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	And complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	And complemented direct bit to carry	4	3(2)	3	2(2)
ORL	CY, bit51	Or direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Or direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	Or complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	Or complemented direct bit to carry	4	3(2)	3	2(2)
MOV	CY, bit51	Move direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Move direct bit to carry	4	3(2)	3	2(2)
	bit51, CY	Move carry to direct bit	2	2(3)	2	2(3)
	bit, CY	Move carry to direct bit	4	4(3)	3	3(3)

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *If this instruction addresses an I/O Port (Px, x= 0–3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
3. *If this instruction addresses an I/O Port (Px, x= 0–3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.*

Table 30. Summary of Exchange, Push and Pop Instructions

Exchange bytes	XCH A, <src>	(A) ↔ src opnd
Exchange Digit	XCHD A, <src>	$(A)_{3:0}$ ↔ src $opnd_{3:0}$
Push	PUSH <src>	(SP) ← (SP) +1; ((SP)) ← src opnd; (SP) ← (SP) + size (src opnd) – 1
Pop	POP <dest>	(SP) ← (SP) – size (dest opnd) + 1; dest opnd ← ((SP)); (SP) ← (SP) –1

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
XCH	A, Rn	ACC and register	1	3	2	4
	A, dir8	ACC and direct address (on–chip RAM or SFR)	2	3(3)	2	3(3)
	A, @Ri	ACC and indirect address	1	4	2	5
XCHD	A, @Ri	ACC low nibble and indirect address (256 bytes)	1	4	2	5
PUSH	dir8	Push direct address onto stack	2	2(2)	2	2(2)
	#data	Push immediate data onto stack	4	4	3	3
	#data16	Push 16-bit immediate data onto stack	5	5	4	5
	Rm	Push byte register onto stack	3	4	2	3
	WRj	Push word register onto stack	3	5	2	4
	DRk	Push double word register onto stack	3	9	2	8
POP	dir8	Pop direct address (on–chip RAM or SFR) from stack	2	3(2)	2	3(2)
	Rm	Pop byte register from stack	3	3	2	2
	WRj	Pop word register from stack	3	5	2	4
	DRk	Pop double word register from stack	3	9	2	8

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
3. *If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.*

Table 31. Summary of Conditional Jump Instructions (1/2)

Jump conditional on status	Jcc rel	(PC) ← (PC) + size (instr); IF [cc] THEN (PC) ← (PC) + rel

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode(2)		Source Mode(2)	
			Bytes	States	Bytes	States
JC	rel	Jump if carry	2	1/4(3)	2	1/4(3)
JNC	rel	Jump if not carry	2	1/4(3)	2	1/4(3)
JE	rel	Jump if equal	3	2/5(3)	2	1/4(3)
JNE	rel	Jump if not equal	3	2/5(3)	2	1/4(3)
JG	rel	Jump if greater than	3	2/5(3)	2	1/4(3)
JLE	rel	Jump if less than, or equal	3	2/5(3)	2	1/4(3)
JSL	rel	Jump if less than (signed)	3	2/5(3)	2	1/4(3)
JSLE	rel	Jump if less than, or equal (signed)	3	2/5(3)	2	1/4(3)
JSG	rel	Jump if greater than (signed)	3	2/5(3)	2	1/4(3)
JSGE	rel	Jump if greater than or equal (signed)	3	2/5(3)	2	1/4(3)

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *States are given as jump not-taken/taken.*
3. *In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.*

Table 32. Summary of Conditional Jump Instructions (2/2)

Jump if bit	JB <src>, rel	(PC) ← (PC) + size (instr); IF [src opnd= 1] THEN (PC) ← (PC) + rel
Jump if not bit	JNB <src>, rel	(PC) ← (PC) + size (instr); IF [src opnd= 0] THEN (PC) ← (PC) + rel
Jump if bit and clear	JBC <dest>, rel	(PC) ← (PC) + size (instr); IF [dest opnd= 1] THEN dest opnd ← 0 (PC) ← (PC) + rel
Jump if accumulator is zero	JZ rel	(PC) ← (PC) + size (instr); IF [(A)= 0] THEN (PC) ← (PC) + rel
Jump if accumulator is not zero	JNZ rel	(PC) ← (PC) + size (instr); IF [(A) ≠ 0] THEN (PC) ← (PC) + rel
Compare and jump if not equal	CJNE <src1>, <src2>, rel	(PC) ← (PC) + size (instr); IF [src opnd1 < src opnd2] THEN (CY) ← 1 IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0 IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel
Decrement and jump if not zero	DJNZ <dest>, rel	(PC) ← (PC) + size (instr); dest opnd ← dest opnd –1; IF [∅ (Z)] THEN (PC) ← (PC) + rel

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode[2]		Source Mode[2]	
			Bytes	States	Bytes	States
JB	bit51, rel	Jump if direct bit is set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is set	5	4/7[3][6]	4	3/6[3][6]
JNB	bit51, rel	Jump if direct bit is not set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is not set	5	4/7[3][6]	4	3/6[3]
JBC	bit51, rel	Jump if direct bit is set & clear bit	3	4/7[5][6]	3	4/7[5][6]
	bit, rel	Jump if direct bit of 8-bit address location is set and clear	5	7/10[5][6]	4	6/9[5][6]
JZ	rel	Jump if ACC is zero	2	2/5[6]	2	2/5[6]
JNZ	rel	Jump if ACC is not zero	2	2/5[6]	2	2/5[6]
CJNE	A, dir8, rel	Compare direct address to ACC and jump if not equal	3	2/5[3][6]	3	2/5[3][6]
	A, #data, rel	Compare immediate to ACC and jump if not equal	3	2/5[6]	3	2/5[6]
	Rn, #data, rel	Compare immediate to register and jump if not equal	3	2/5[6]	4	3/6[6]
	@Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	3/6[6]	4	4/7[6]
DJNZ	Rn, rel	Decrement register and jump if not zero	2	2/5[6]	3	3/6[6]
	dir8, rel	Decrement direct address and jump if not zero	3	3/6[4][6]	3	3/6[4][6]

Notes:

1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *States are given as jump not-taken/taken.*
3. *If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.*
4. *If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.*
5. *If this instruction addresses an I/O Port (Px, x= 0-3), add 3 to the number of states. Add 5 if it addresses a Peripheral SFR.*
6. *In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.*

Table 33. Summary of unconditional Jump Instructions

Absolute jump	AJMP <src>	(PC) ← (PC) +2; $(PC)_{10:0}$ ← src opnd
Extended jump	EJMP <src>	(PC) ← (PC) + size (instr); $(PC)_{23:0}$ ← src opnd
Long jump	LJMP <src>	(PC) ← (PC) + size (instr); $(PC)_{15:0}$ ← src opnd
Short jump	SJMP rel	(PC) ← (PC) +2; (PC) ← (PC) +rel
Jump indirect	JMP @A +DPTR	$(PC)_{23:16}$ ← FFh; $(PC)_{15:0}$ ← (A) + (DPTR)
No operation	NOP	(PC) ← (PC) +1

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
AJMP	addr11	Absolute jump	2	3(2)(3)	2	3(2)(3)
EJMP	addr24	Extended jump	5	6(2)(4)	4	5(2)(4)
	@DRk	Extended jump (indirect)	3	7(2)(4)	2	6(2)(4)
LJMP	@WRj	Long jump (indirect)	3	6(2)(4)	2	5(2)(4)
	addr16	Long jump (direct address)	3	5(2)(4)	3	5(2)(4)
SJMP	rel	Short jump (relative address)	2	4(2)(4)	2	4(2)(4)
JMP	@A +DPTR	Jump indirect relative to the DPTR	1	5(2)(4)	1	5(2)(4)
NOP		No operation (Jump never)	1	1	1	1

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *In internal execution only, add 1 to the number of states if the destination address is internal and odd.*
3. *Add 2 to the number of states if the destination address is external.*
4. *Add 3 to the number of states if the destination address is external.*

Table 34. Summary of Call and Return Instructions

Absolute call	ACALL <src>	(PC) ← (PC) +2; push $(PC)_{15:0}$; $(PC)_{10:0}$ ← src opnd
Extended call	ECALL <src>	(PC) ← (PC) + size (instr); push $(PC)_{23:0}$; $(PC)_{23:0}$ ← src opnd
Long call	LCALL <src>	(PC) ← (PC) + size (instr); push $(PC)_{15:0}$; $(PC)_{15:0}$ ← src opnd
Return from subroutine	RET	pop $(PC)_{15:0}$
Extended return from subroutine	ERET	pop $(PC)_{23:0}$
Return from interrupt	RETI	IF [INTR= 0] THEN pop $(PC)_{15:0}$ IF [INTR= 1] THEN pop $(PC)_{23:0}$; pop (PSW1)
Trap interrupt	TRAP	(PC) ← (PC) + size (instr); IF [INTR= 0] THEN push $(PC)_{15:0}$ IF [INTR= 1] THEN push (PSW1); push $(PC)_{23:0}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ACALL	addr11	Absolute subroutine call	2	9(2)(3)	2	9(2)(3)
ECALL	@DRk	Extended subroutine call (indirect)	3	14(2)(3)	2	13(2)(3)
	addr24	Extended subroutine call	5	14(2)(3)	4	13(2)(3)
LCALL	@WRj	Long subroutine call (indirect)	3	10(2)(3)	2	9(2)(3)
	addr16	Long subroutine call	3	9(2)(3)	3	9(2)(3)
RET		Return from subroutine	1	7(2)	1	7(2)
ERET		Extended subroutine return	3	9(2)	2	8(2)
RETI		Return from interrupt	1	7(2)(4)	1	7(2)(4)
TRAP		Jump to the trap interrupt vector	2	12(4)	1	11(4)

Notes:
1. *A shaded cell denotes an instruction in the C51 Architecture.*
2. *In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.*
3. *Add 2 to the number of states if the destination address is external.*
4. *Add 5 to the number of states if INTR= 1.*

8. ROM Verifying

8.1. Internal ROM Features

Mask ROM Devices

The internal ROM of the TSC83251G1D contains four different areas: Code Memory, Configuration Bytes, Encryption Array and Signature Bytes.

All the Internal ROM of TSC83251G1D products is made of Mask ROM cells. They can be verified using the same algorithm as the EPROM/OTP devices.

ROMless Devices

The TSC80251G1D products include only Signature Bytes made of Mask ROM cells. They can be verified using the same algorithm as the EPROM/OTP devices.

These products do not include on–chip Configuration Bytes, Code Memory and Encryption Array.

8.2. Encryption Features

In some microcontrollers applications, it is desirable that the user program code be secured from unauthorized access.

The TSC83251G1D products include a 128–byte Encryption Array located in non volatile memory outside the memory address space. During verification of the on–chip code memory, the seven low–order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive–NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

Note:
When a MOVC instruction is executed the content of the ROM is not encrypted. In order to fully protect the user program code, MOVC to the on–chip Code Memory can only be executed from the on–chip Code Memory when the encryption is used for mask ROM devices.

Program code in the on–chip Code Memory is encrypted when read out for verification if the Encryption Array is programmed.

Caution:
If the encryption feature is implemented, the portion of the on–chip code memory that does not contain program code should be filled with "random" byte values other than FFh to prevent the encryption key sequence from being revealed.

To preserve the secrecy of the encryption key byte sequence, the Encryption Array cannot be verified.

8.3. Signature Bytes

The TSC80251G1D derivatives contain factory–programmed Signature Bytes. These bytes are located in non–volatile memory outside the memory address space at 30h, 31h, 60h and 61h. To read the Signature Bytes, perform the procedure described in paragraph "Verify Algorithm". The values of the Signature Bytes are listed in Table 35.

Table 35. Signature Bytes (Electronic ID)

		Signature Address	Signature Data
Vendor	TEMIC	30h	58h
Architecture	C251	31h	40h
Memory	16K MaskROM or ROMless	60h	7Bh
Revision	None (TSC80251G1 derivative) First (TSC80251G1D derivative)	61h	FFh FEh

Note:
The way Configuration Bytes are used is changing from TSC80251G1 derivatives to TSC80251G1D derivatives. The verify algorithm should check the product revision to select the right model.

8.4. Verify Algorithm

Figure 9 shows the hardware setup needed to verify the internal ROM areas of the TSC80251G1D derivatives:

- The chip has to be put under reset and maintained in this state until the completion of the verify sequence.
- The voltage on the EA# pin has to be set to VDD.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a logic high level.
- Then PSEN# has to be to forced to a logic low level after two clock cycles or more and it has to be maintained in this state until the completion of the programming sequence.
- The Verify Mode is selected according to the code applied on Port 0 (see Table 36). It has to be applied until the completion of this verification.
- The verification address is applied on Ports 1 and 3 which are respectively the MSB and the LSB of the address.
- Then device is driving the data on Port 2.
- PSEN# and the other control signals have to be released to complete a sequence of verify operations.

Table 36. Verifying Modes

Verify ROM	RST	EA#	PSEN#	ALE	P0	P2	P1(MSB) P3(LSB)
On–chip code memory	1	1	0	1	28h	Data	16–bit Address: 0000h-3FFFh (16K)
Configuration Bytes	1	1	0	1	29h	Data	UCONFIG0: FFF8h UCONFIG1: FFF9h
Signature Bytes	1	1	0	1	29h	Data	30h, 31h, 60h, 61h

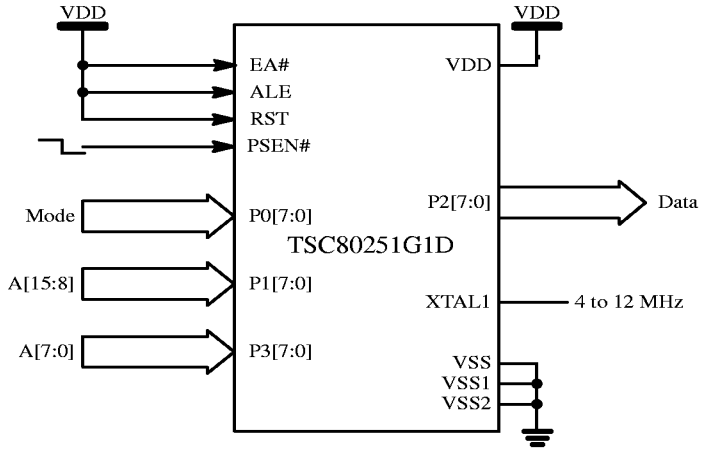


Figure 9. Setup for ROM Verifying

9. Absolute Maximum Rating and Operating Conditions

9.1. Absolute Maximum Rating

Table 37. Absolute Maximum Ratings

• Storage Temperature	–65 to +150°C
• Voltage on any other Pin to VSS	–0.5 to +6.5 V
• I_{OL} per I/O Pin	15 mA
• Power Dissipation	1.5 W

9.2. Operating Conditions

Table 38. Operating Conditions

• Ambient Temperature Under Bias	
Commercial	0 to +70°C
Industrial	–40 to +85°C
• V_{DD}	
High Speed versions	4.5 to 5.5 V
Low Voltage versions	2.7 to 5.5 V

Note:
Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "operating conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

10. DC Characteristics – Commercial & Industrial

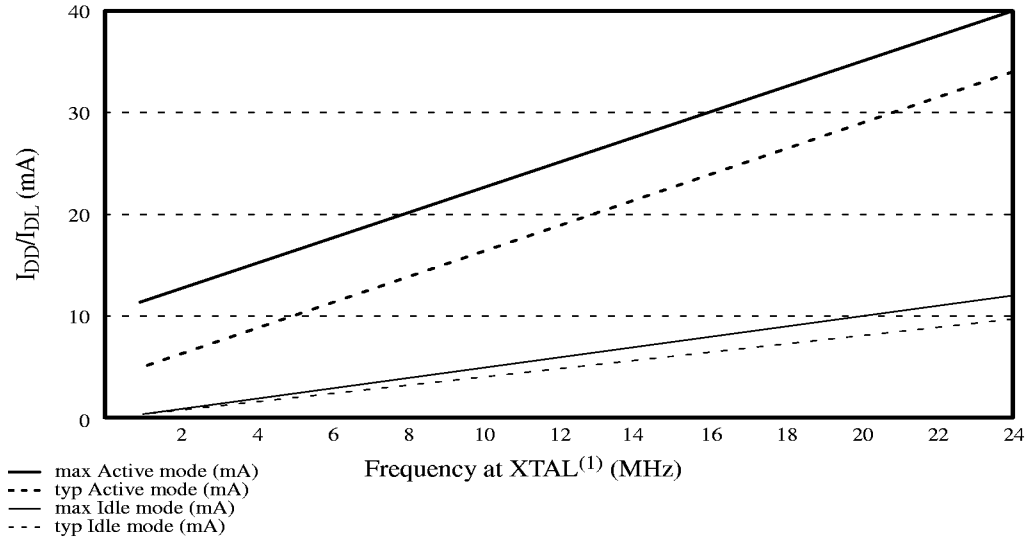
10.1. DC Characteristics: High Speed versions – Commercial & Industrial

Table 39. DC Characteristics; V_{DD}= 4.5 to 5.5 V, T_A= –40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	–0.5		0.2V_{DD} - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	–0.5		0.3V_{DD}	V	
V_{IL2}	Input Low Voltage (EA#)	0		0.2V_{DD} - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	0.2V_{DD} + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	0.7V_{DD}		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.3 0.45 1.0	V	I_{OL}= 100 µA[1][2] I_{OL}= 1.6 mA[1][2] I_{OL}= 3.5 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#,Port 2 in Page Mode during External Address)			0.3 0.45 1.0	V	I_{OL}= 200 µA[1][2] I_{OL}= 3.2 mA[1][2] I_{OL}= 7.0 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	V_{DD} –0.3 V_{DD} –0.7 V_{DD} –1.5			V	I_{OH}= –10 µA[3] I_{OH}= –30 µA[3] I_{OH}= –60 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	V_{DD} –0.3 V_{DD} –0.7 V_{DD} –1.5			V	I_{OH}= –200 µA I_{OH}= –3.2 mA I_{OH}= –7.0 mA
V_{RST}+	Reset threshold on	3.9	4.1	4.3	V	
V_{RST}–	Reset threshold off	3.4	3.6	3.8	V	
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3)			- 50	µA	V_{IN}= 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	V_{IN}= V_{DD}
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3 – AWAIT#)			- 650	µA	V_{IN}= 2.0 V
R_{RST}	RST Pull–Down Resistor	40	170	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
I_{DD}	Operating Current		18	25	mA	F_{OSC}= 12 MHz
			23	30	mA	F_{OSC}= 16 MHz
			34	40	mA	F_{OSC}= 24 MHz
I_{DL}	Idle Mode Current		5	6	mA	F_{OSC}= 12 MHz
			6.5	8	mA	F_{OSC}= 16 MHz
			9.5	12	mA	F_{OSC}= 24 MHz
I_{PD}	Power–Down Current		2	20	µA	V_{RET} < V_{DD} < 5.5 V

Notes:

1. *Under steady–state (non–transient) conditions, I_{OL} must be externally limited as follows:*
   Maximum I_{OL} per port pin: . . . . . 10 mA
   Maximum I_{OL} per 8–bit port: Port 0 . . . . . 26 mA
   Ports 1-3 . . . . . 15 mA
   Maximum Total I_{OL} for all: Output Pins . . . 71 mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. *Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low–level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS–level input logic.*
3. *Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.*
4. *Typical values are obtained using V_{DD} = 5 V and T_A = 25°C with no guarantee. They are not tested and there is not guarantee on these values.*
5. *The input threshold voltage of SCL and SDA meets the I^2C specification, so an input voltage below 0.3.V_{DD} will be recognized as a logic 0 while an input voltage above 0.7.V_{DD} will be recognized as a logic 1.*



Note:

1. *The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.*

Figure 10. I_{DD}/I_{DL} versus Frequency; V_{DD}= 4.5 to 5.5 V

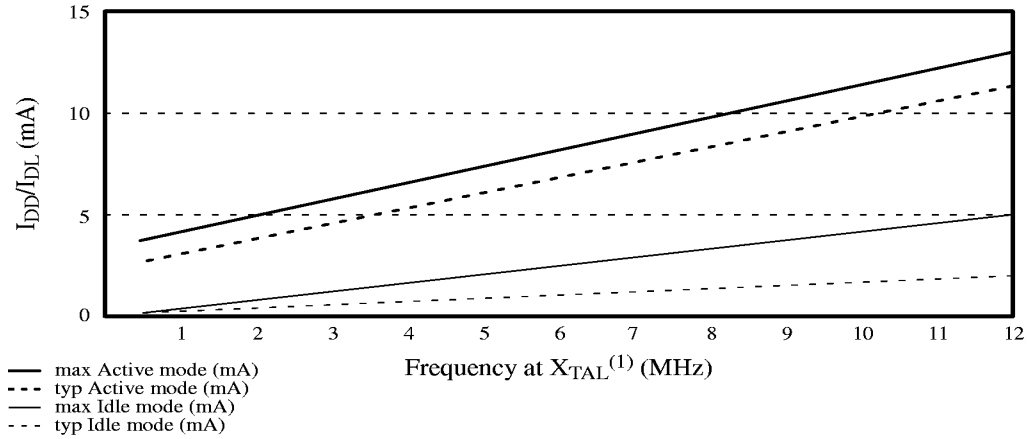
10.2. DC Characteristics: Low Voltage versions – Commercial & Industrial

Table 40. DC Characteristics from 2.7 to 5.5 V, T_A= –40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	–0.5		$0.2V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	–0.5		$0.3V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL}= 0.8 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#,Port 2 in Page Mode during External Address)			0.45	V	I_{OL}= 1.6 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	$0.9V_{DD}$			V	I_{OH}= –10 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	$0.9V_{DD}$			V	I_{OH}= –40 µA
V_{RST}+	Reset threshold on	2.1	2.3	2.4	V	
V_{RST}–	Reset threshold off	1.8	2.0	2.1	V	
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3 – AWAIT#)			- 50	µA	V_{IN}= 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	V_{IN}= V_{DD}
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	V_{IN}= 2.0 V
R_{RST}	RST Pull–Down Resistor	40	170	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
I_{DD}	Operating Current		3.5	8	mA	5 MHz, V_{DD} < 3.6 V
			7	11	mA	10 MHz, V_{DD} < 3.6V
			8	13	mA	12 MHz, V_{DD} < 3.6 V
I_{DL}	Idle Mode Current		0.5	1	mA	5 MHz, V_{DD} < 3.6 V
			1.5	4	mA	10 MHz, V_{DD} < 3.6 V
			2	5	mA	12 MHz, V_{DD} < 3.6 V
I_{PD}	Power–Down Current		2	10	µA	V_{RET} < V_{DD} < 3.6 V

Notes:

1. *Under steady–state (non–transient) conditions, I_{OL} must be externally limited as follows:*
   Maximum I_{OL} per port pin: . . . . . 10 mA
   Maximum I_{OL} per 8–bit port: Port 0 . . . . . 26 mA
   Ports 1-3 . . . . . 15 mA
   Maximum Total I_{OL} for all: Output Pins . . . 71 mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. *Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low–level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS–level input logic.*
3. *Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.*
4. *Typical values are obtained using V_{DD} = 3 V and T_A = 25°C with no guarantee. They are not tested and there is not guarantee on these values.*
5. *The input threshold voltage of SCL and SDA meets the I^2C specification, so an input voltage below 0.3.V_{DD} will be recognized as a logic 0 while an input voltage above 0.7.V_{DD} will be recognized as a logic 1.*



Note:

1. *The clock prescaler is not used: F_{OSC} = F_{XTAL}.*

Figure 11. I_{DD}/I_{DL} versus X_{TAL} Frequency; V_{DD}= 2.7 to 5.5 V

10.3. DC Characteristics: I_{DD}, I_{DL} and I_{PD} Test Conditions

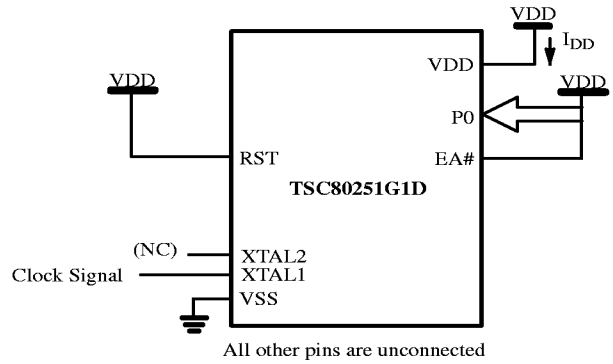


Figure 12. I_{DD} Test Condition, Active Mode

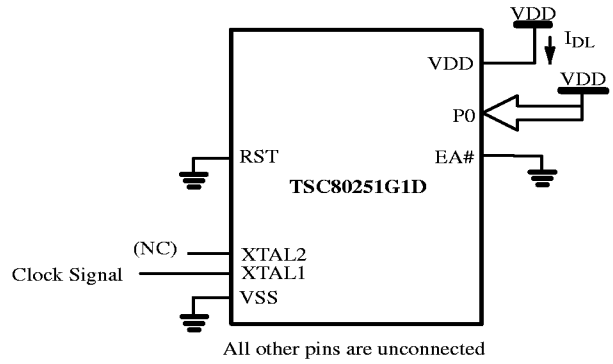


Figure 13. I_{DL} Test Condition, Idle Mode

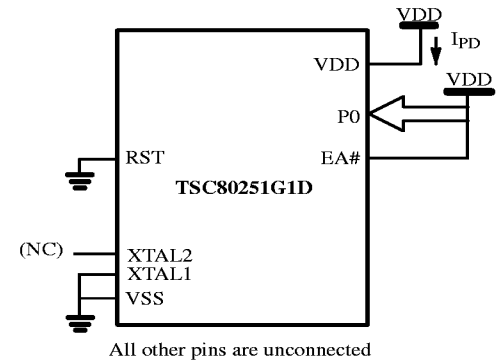


Figure 14. I_{PD} Test Condition, Power–Down Mode

11. AC Characteristics – Commercial & Industrial

11.1. AC Characteristics – External Bus Cycles

Definition of symbols

Table 41. External Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 42 and Table 43 list AC timing parameters for the TSC80251G1D with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by PSEN#/RD#/WR# wait states.

Figure 15 to Figure 20 show the bus cycles with the timing parameters.

Table 42. Bus Cycles AC Timings; V_{DD}= 4.5 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		24 MHz		Unit
		Min	Max	Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		41		ns
T_{LHLL}	ALE Pulse Width	82		61		40		ns(2)
T_{AVLL}	Address Valid to ALE Low	80		59		38		ns(2)
T_{LLAX}	Address hold after ALE Low	27		19		2.5		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	158		118		76		ns(3)
T_{WLWH}	WR# Pulse Width	160		120		78		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	41		27		14		ns
T_{LHAX}	ALE High to Address Hold	116		81		43		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		144		102		59	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		2		2		2	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		23		23		23	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		188		146		104	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	24		24		24		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	189		148		104		ns
T_{WHLH}	WR# High to ALE High	192		150		103		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		262		187		110	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		300		217		137	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		146		104		62	ns
T_{AXDX}	Data Hold after Address Hold	0		0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	125		91		57		ns (2)
T_{AVWL1}	Address (P0) Valid to WR# Low	124		90		53		ns (2)
T_{AVWL2}	Address (P2) Valid to WR# Low	162		119		75		ns (2)
T_{WHQX}	Data Hold after WR# High	81		60		37		ns
T_{QVWH}	Data Valid to WR# High	135		104		74		ns(3)
T_{WHAX}	WR# High to Address Hold	168		126		84		ns

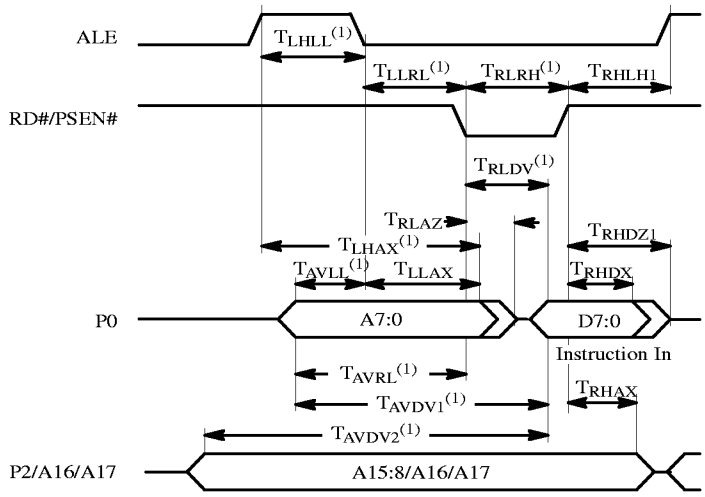
Notes:
1. *Specification for PSEN# are identical to those for RD#.*
2. *If a wait state is added by extending ALE, add $2\times T_{OSC}$.*
3. *If wait states are added by extending RD#/PSEN#/WR#, add $2N\times T_{OSC}$ (N= 1..3).*

Table 43. Bus Cycles AC Timings; V_{DD}= 2.7 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	12 MHz		Unit
		Min	Max	
T_{OSC}	$1/F_{OSC}$	83		ns
T_{LHLL}	ALE Pulse Width	81		ns(2)
T_{AVLL}	Address Valid to ALE Low	66		ns(2)
T_{LLAX}	Address hold after ALE Low	5		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	152		ns (3)
T_{WLWH}	WR# Pulse Width	155		ns (3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	34		ns
T_{LHAX}	ALE High to Address Hold	93		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		115	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		2(4)	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		35	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		199	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	24		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	189		ns
T_{WHLH}	WR# High to ALE High	192		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		214	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		271	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		131	ns
T_{AXDX}	Data Hold after Address Hold	0		ns
T_{AVRL}(1)	Address Valid to RD# Low	114		ns (2)
T_{AVWL1}	Address (P0) Valid to WR# Low	112		ns (2)
T_{AVWL2}	Address (P2) Valid to WR# Low	161		ns(2)
T_{WHQX}	Data Hold after WR# High	87		ns
T_{QVWH}	Data Valid to WR# High	135		n (3)
T_{WHAX}	WR# High to Address Hold	164		ns

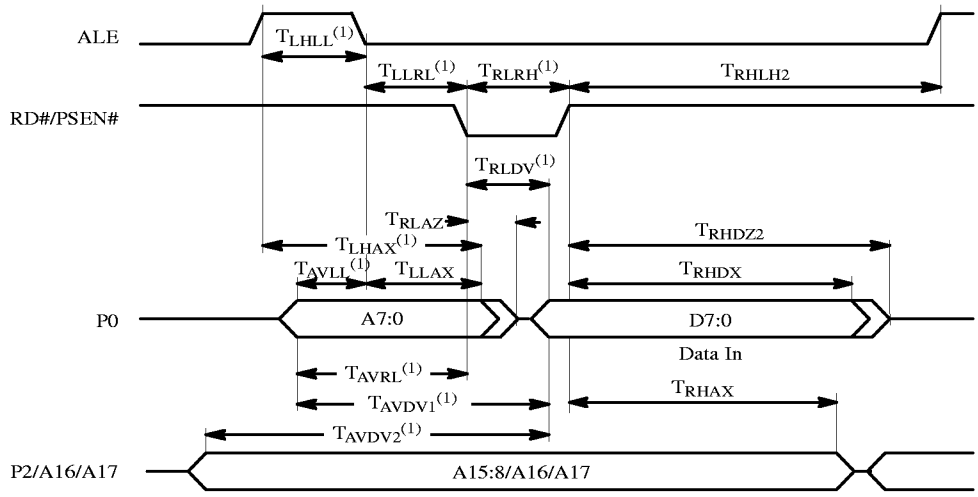
Notes:
1. *Specification for PSEN# are identical to those for RD#.*
2. *If a wait state is added by extending ALE, add $2\times T_{OSC}$.*
3. *If wait states are added by extending RD#/PSEN#/WR#, add $2N\times T_{OSC}$ (N= 1..3).*
4. *T_{RLAZ} max is 0 ns if V_{DD} < 3.6V.*

Waveforms in Non–Page Mode



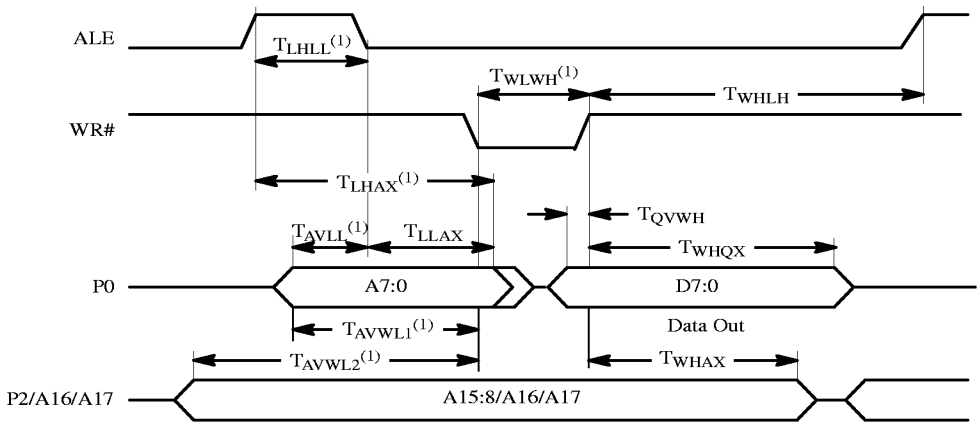
Note:
1. The value of this parameter depends on wait states. See Table 42 and Table 43.

Figure 15. External Bus Cycle: Code Fetch (Non–Page Mode)



Note:
1. The value of this parameter depends on wait states. See Table 42 and Table 43.

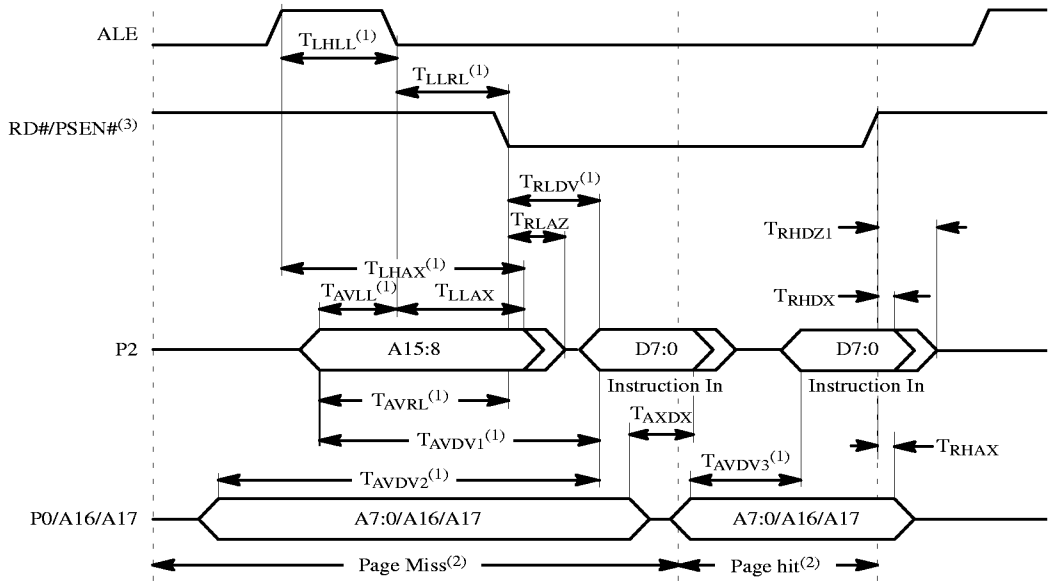
Figure 16. External Bus Cycle: Data Read (Non–Page Mode)



Note:
1. The value of this parameter depends on wait states. See Table 42 and Table 43.

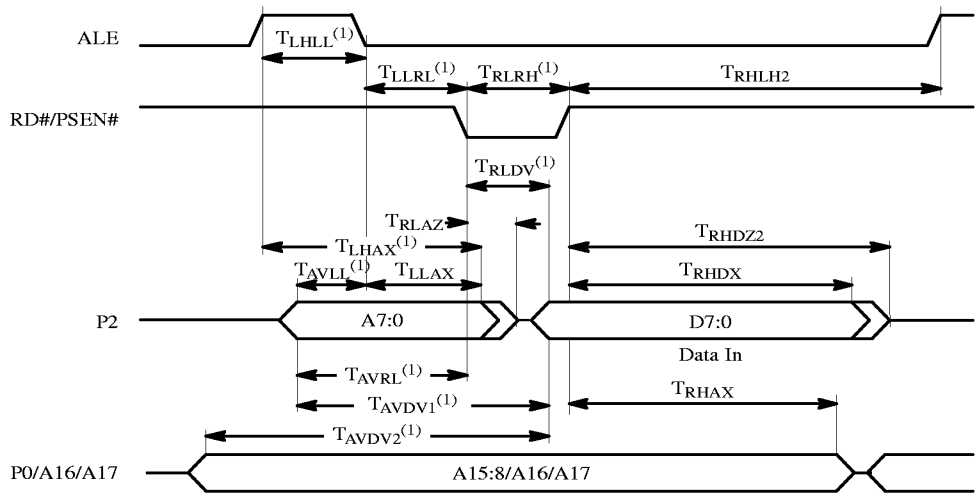
Figure 17. External Bus Cycle: DataWrite (Non–Page Mode)

Waveforms in Page Mode



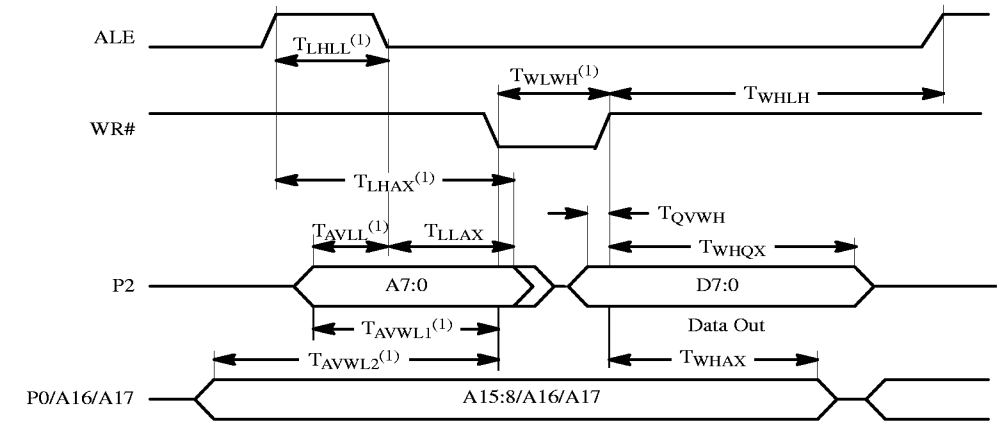
Notes:
1. The value of this parameter depends on wait states. See Table 42 and Table 43.
2. A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2\times T_{OSC}$);a page miss requires two states ($4\times T_{OSC}$).
3. During a sequence of page hits, PSEN# remains low until the end of the last page–hit cycle.

Figure 18. External Bus Cycle: Code Fetch (Page Mode)



Note:
1. The value of this parameter depends on wait states. See Table 42 and Table 43.

Figure 19. External Bus Cycle: Data Read (Page Mode)



Note:
1. The value of this parameter depends on wait states. See Table 42 and Table 43.

Figure 20. External Bus Cycle: DataWrite (Page Mode)

11.2. AC Characteristics – Real–Time Synchronous Wait State

Definition of symbols

Table 44. Real–Time Synchronous Wait Timing Symbol Definitions

Signals	
C	WCLK
R	RD#/PSEN#
W	WR#
Y	WAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

Table 45. Real–Time Synchronous Wait AC Timings; V_{DD}= 2.7 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{CLYV}	Wait Clock Low to Wait Set–up	0	T_{OSC} – 20	ns
T_{CLYX}	Wait Hold after Wait Clock Low	2W×T_{OSC} + 5	(1+2W)×T_{OSC} – 20	ns
T_{RLYV}	PSEN#/RD# Low to Wait Set–up	0	T_{OSC} – 20	ns
T_{RLYX}	Wait Hold after PSEN#/RD# Low	2W×T_{OSC} + 5	(1+2W)×T_{OSC} – 20	ns
T_{WLYV}	WR# Low to Wait Set–up	0	T_{OSC} – 20	ns
T_{WLYX}	Wait Hold after WR# Low	2W×T_{OSC} + 5	(1+2W)×T_{OSC} – 20	ns

Waveforms

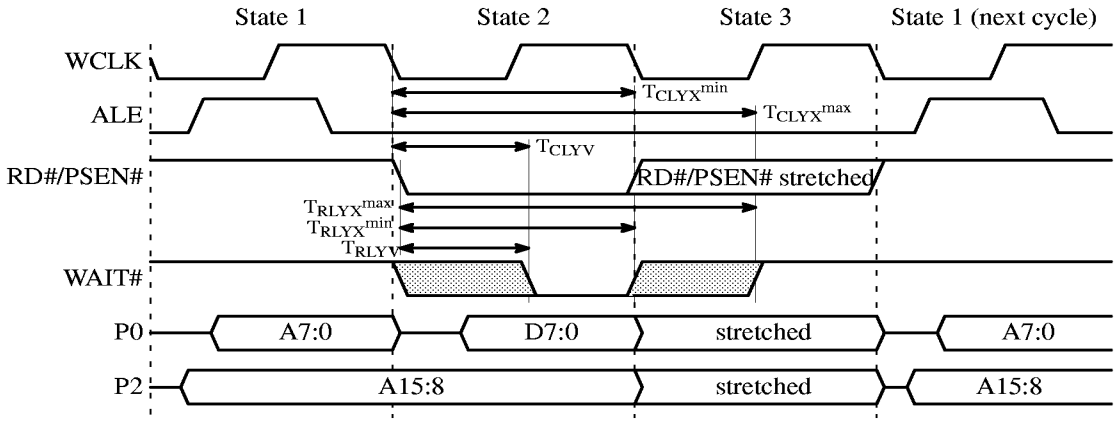


Figure 21. Real–time Synchronous Wait State: Code Fetch/Data Read

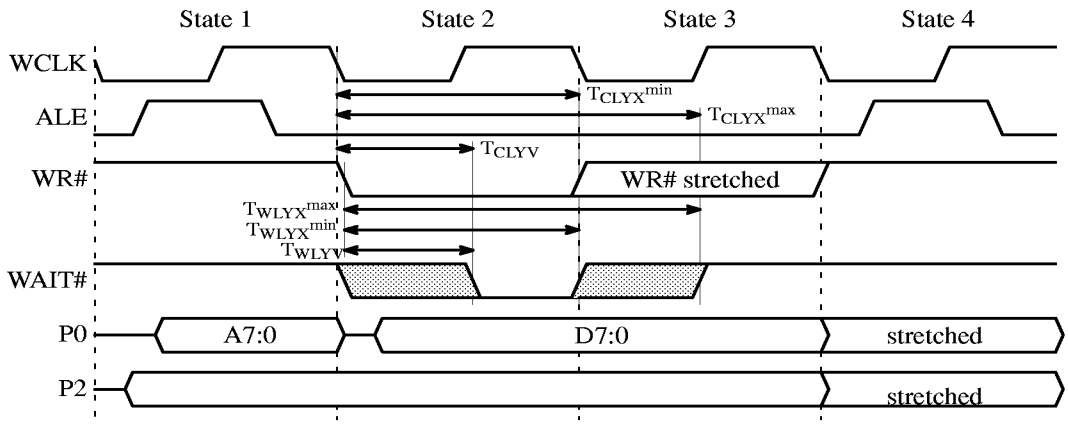


Figure 22. Real–time Synchronous Wait State: Data Write

11.3. AC Characteristics – Real–Time Asynchronous Wait State

Definition of symbols

Table 46. Real–Time Asynchronous Wait Timing Symbol Definitions

Signals	
S	PSEN#/RD#/WR#
Y	AWAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

Table 47. Real–Time Asynchronous Wait AC Timings; V_{DD}= 2.7 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{SLYV}	PSEN#/RD#/WR# Low to Wait Set–up		T_{OSC} – 10	ns
T_{SLYX}	Wait Hold after PSEN#/RD#/WR# Low	(2N–1)×T_{OSC} + 10		ns(1)

Note:
1. N is the number of wait states added (N≥ 1).

Waveforms

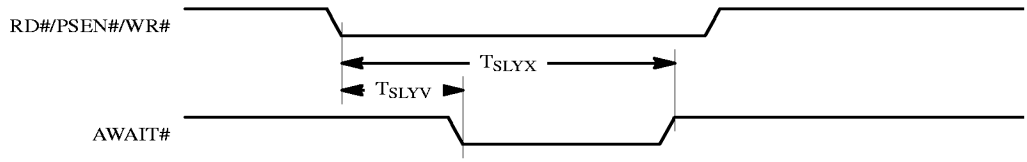


Figure 23. Real–time Asynchronous Wait State Timings

11.4. AC Characteristics – Serial Port in Shift Register Mode

Definition of symbols

Table 48. Serial Port Timing Symbol Definitions

Signals	
D	Data In
Q	Data Out
X	Clock

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

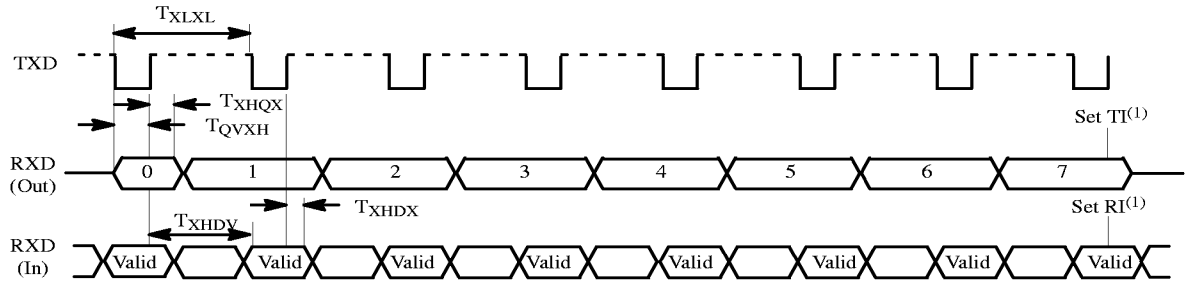
Timings

Table 49. Serial Port AC Timing –Shift Register Mode; V_{DD}= 2.7 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	12 MHz		16 MHz (1)		24 MHz (1)		Unit
		Min	Max	Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	998		749		500		ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	833		625		417		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	165		124		82		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		974		732		482	ns

Note:
1. For high speed versions only.

Waveforms



Note:
1. TI and RI are set during S1P1 of the peripheral cycle following the shift of the eight bit.

Figure 24. Serial Port Waveforms – Shift Register Mode

11.5. AC Characteristics – SSLC: I²C Interface

Timings

Table 50. I²C Interface AC Timing; V_{DD}= 2.7 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	INPUT Min	INPUT Max	OUTPUT Min	OUTPUT Max
$T_{HD;STA}$	Start condition hold time	14×T_{CLCL} (4)		4.0 µs (1)	
T_{LOW}	SCL low time	16×T_{CLCL} (4)		4.7 µs (1)	
T_{HIGH}	SCL high time	14×T_{CLCL} (4)		4.0 µs (1)	
T_{RC}	SCL rise time		1 µs		– (2)
T_{FC}	SCL fall time		0.3 µs		0.3 µs (3)
$T_{SU;DAT1}$	Data set–up time	250 ns		20×T_{CLCL} (4) – T_{RD}	
$T_{SU;DAT2}$	SDA set–up time (before repeated START condition)	250 ns		1 µs (1)	
$T_{SU;DAT3}$	SDA set–up time (before STOP condition)	250 ns		8×T_{CLCL} (4)	
$T_{HD;DAT}$	Data hold time	0 ns		8×T_{CLCL} (4) – T_{FC}	
$T_{SU;STA}$	Repeated START set–up time	14×T_{CLCL} (4)		4.7 µs (1)	
$T_{SU;STO}$	STOP condition set–up time	14×T_{CLCL} (4)		4.0 µs (1)	
T_{BUF}	Bus free time	14×T_{CLCL} (4)		4.7 µs (1)	
T_{RD}	SDA rise time		1 µs		– (2)
T_{FD}	SDA fall time		0.3 µs		0.3 µs (3)

Notes:
1. *At 100 kbit/s. At other bit–rates this value is inversely proportional to the bit–rate of 100 kbit/s.*
2. *Determined by the external bus–line capacitance and the external bus–line pull–up resistor, this must be < 1 µs.*
3. *Spikes on the SDA and SCL lines with a duration of less than 3×T_{CLCL} will be filtered out. Maximum capacitance on bus–lines SDA and SCL= 400 pF.*
4. *T_{CLCL}= T_{OSC}= one oscillator clock period.*

Waveforms

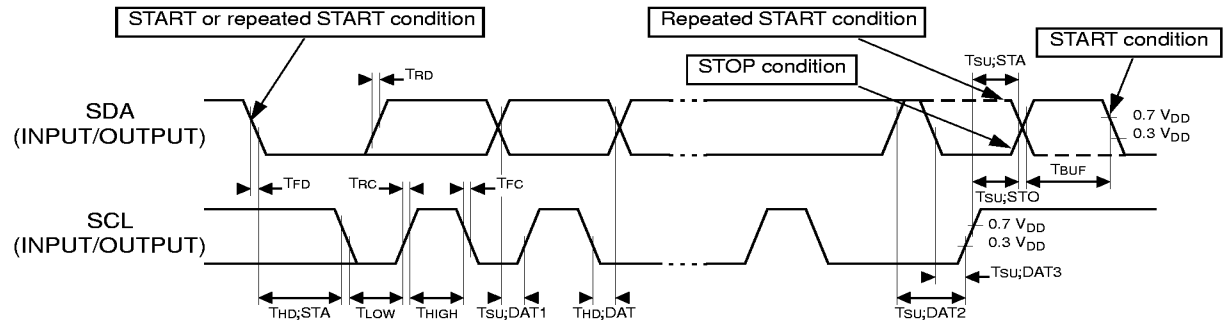


Figure 25. I²C Waveforms

11.6. AC Characteristics – SSLC: SPI Interface

Definition of symbols

Table 51. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out
S	SS#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

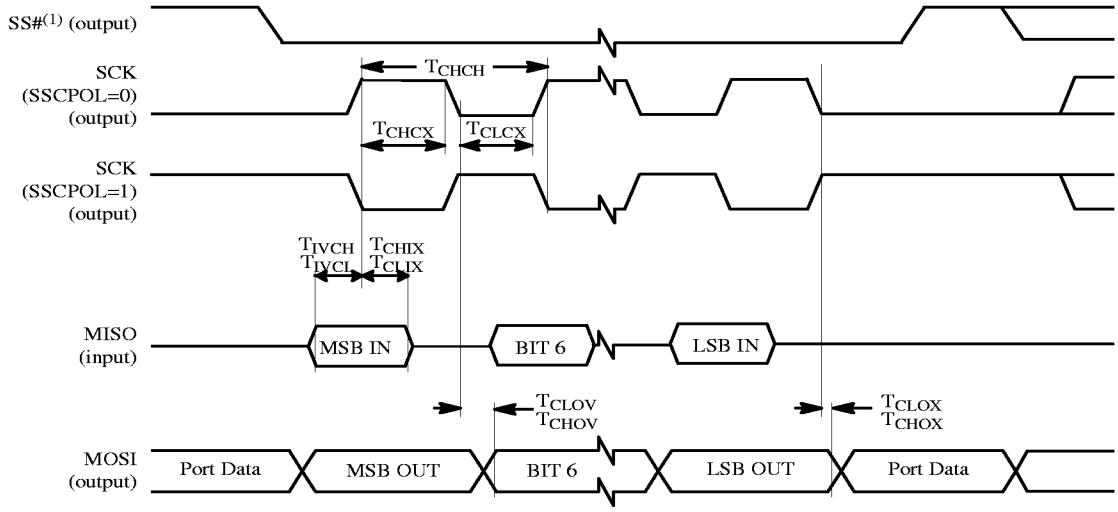
Table 52. SPI Interface AC Timing; V_{DD}= 2.7 to 5.5 V, T_A= –40 to 85°C

Symbol	Parameter	Min	Max	Unit
Slave mode(1)				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{CLOV}, T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns

Symbol	Parameter	Min	Max	Unit
Master mode(3)				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
T_{CLOV}, T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

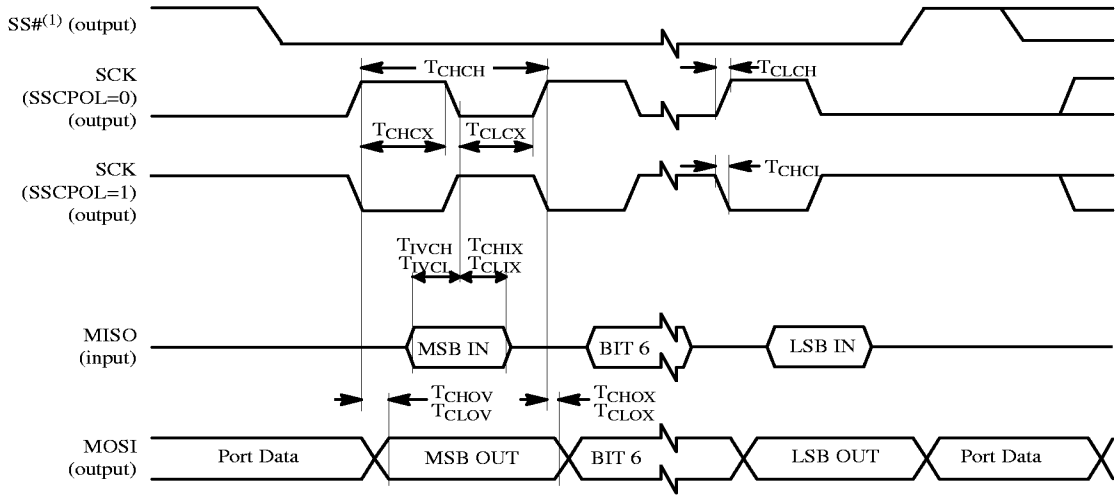
Notes:
1. *Capacitive load on all pins= 200 pF in slave mode.*
2. *The value of this parameter depends on software.*
3. *Capacitive load on all pins= 100 pF in master mode.*

Waveforms



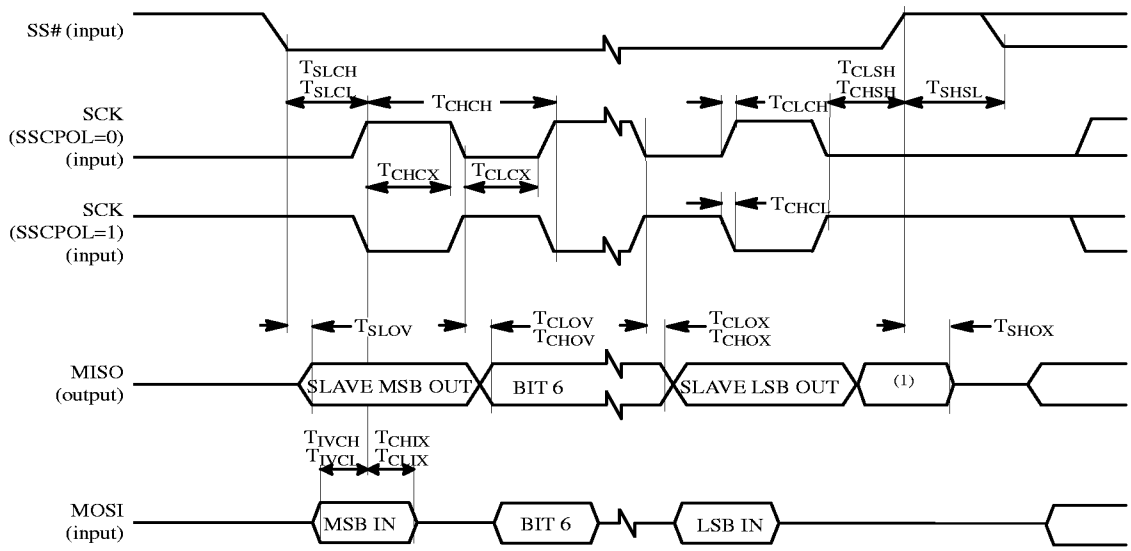
Note:
1. *SS# handled by software.*

Figure 26. SPI Master Waveforms (SSCPHA= 0)



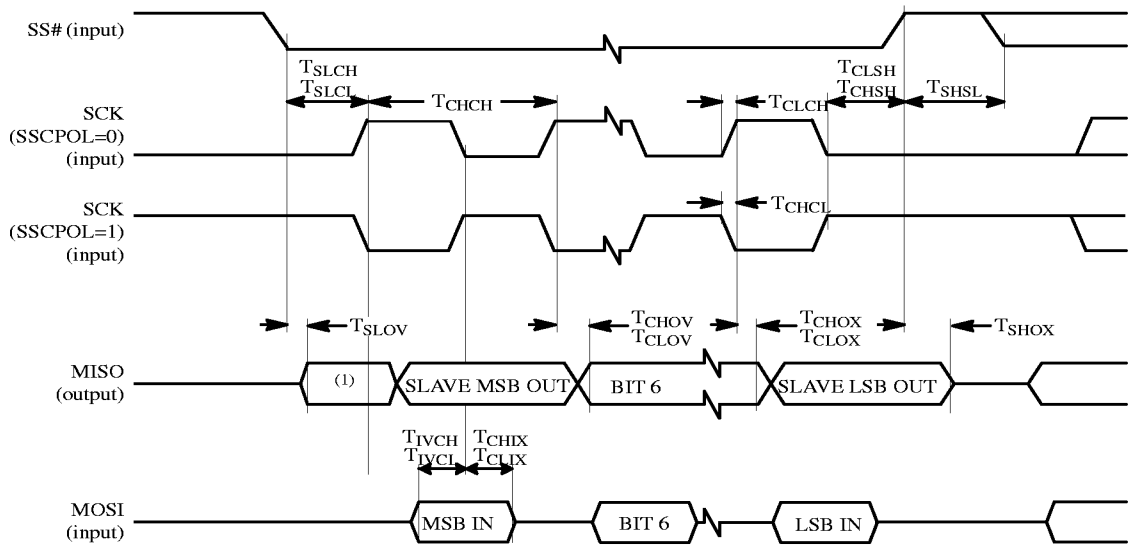
Note:
1. SS# handled by software.

Figure 27. SPI Master Waveforms (SSCPHA= 1)



Note:
1. Not Defined but normally MSB of character just received.

Figure 28. SPI Slave Waveforms (SSCPHA= 0)



Note:
1. Not Defined but generally the LSB of the character which has just been received.

Figure 29. SPI Slave Waveforms (SSCPHA= 1)

11.7. AC Characteristics – ROM Verifying

Definition of symbols

Table 53. ROM Verifying Timing Symbol Definitions

Signals	
A	Address
E	Enable: mode set on Port 0
Q	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Table 54. ROM Verifying AC timings; V_{DD}= 4.5 to 5.5 V, T_A= 0 to 40°C

Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Frequency	82.5	250	ns
T_{AVQV}	Address to Data Valid		48×T_{OSC}	ns
T_{AXQX}	Address to Data Invalid	0		ns
T_{ELQV}	ENABLE low to Data Valid	0	48×T_{OSC}	ns
T_{EHQZ}	Data Float after ENABLE	0	48×T_{OSC}	ns

Waveforms

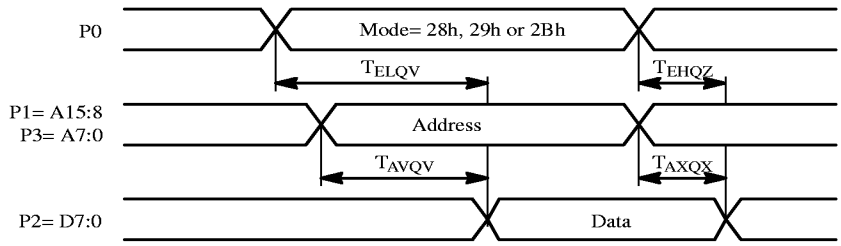


Figure 30. ROM Verifying Waveforms

11.8. AC Characteristics – External Clock Drive and Logic Level References

Definition of symbols

Table 55. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
L	Low
H	High
X	No Longer Valid

Timings

Table 56. External Clock AC Timings; V_{DD}= 4.5 to 5.5 V, T_A= –40 to +85°C

Symbol	Parameter	Min	Max	Unit
F_{OSC}	Oscillator Frequency		24	MHz
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns

Waveforms

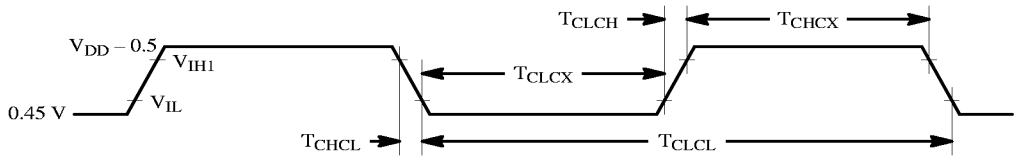
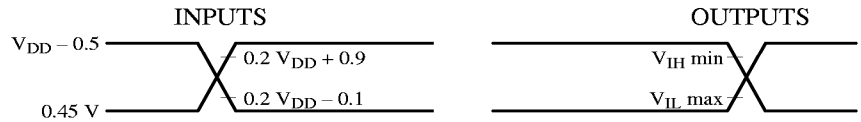
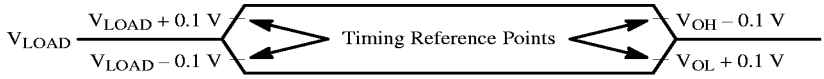


Figure 31. External Clock Waveform



Note:
During AC testing, all inputs are driven at V_{DD} –0.5 V for a logic 1 and 0.45 V for a logic 0.
Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 32. AC Testing Input/Output Waveforms



Note:
For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH}= ±20 mA.

Figure 33. Float Waveforms

12. Packages

12.1. List of Packages

- PDIL 40
- PLCC 44
- VQFP 44 (10 × 10)

12.2. PDIL 40 – Mechanical Outline

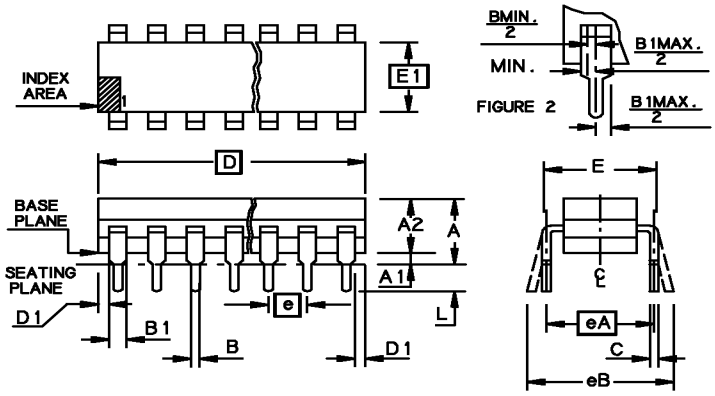


Figure 34. Plastic Dual In Line

Table 57. PDIL Package Size

	MM		INCH	
	Min	Max	Min	Max
A	–	5.08	–	.200
A1	0.38	–	.015	–
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	2.93	3.81	.115	.150
D1	0.13	–	.005	–

12.3. PLCC 44 – Mechanical Outline

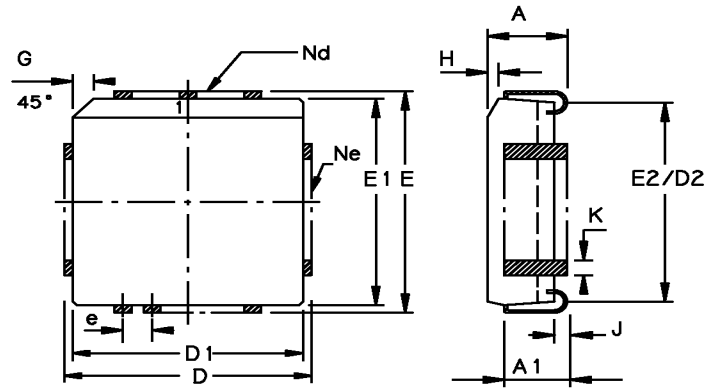


Figure 35. Plastic Lead Chip Carrier

Table 58. PLCC Package Size

	MM		INCH	
	Min	Max	Min	Max
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

12.4. VQFP 44 (10 × 10) – Mechanical Outline

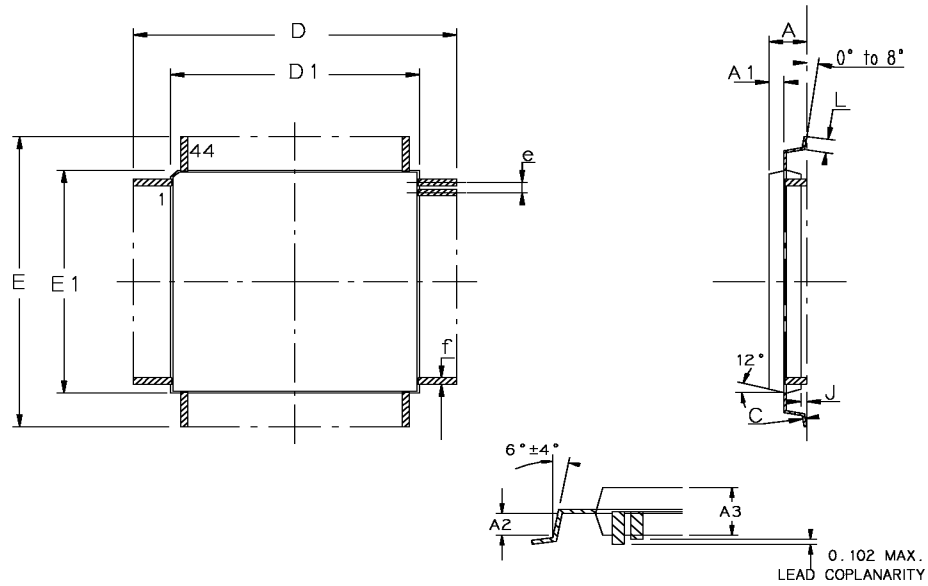


Figure 36. Shrink Quad Flat Pack (Plastic)

Table 59. VQFP Package Size

	MM		INCH	
	Min	Max	Min	Max
A	–	1.60	–	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	–	.002	6
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

13. Ordering Information

13.1. TSC80251G1D ROMless (Step D)

High Speed Versions 4.5 to 5.5 V, Commercial and Industrial

TEMIC Part Number (2)	ROM	Description
TSC80251G1D–24CA	ROMless	24 MHz, Commercial 0° to 70°C, PDIL 40
TSC80251G1D–24CB	ROMless	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G1D–24CED	ROMless	24 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack (1)
TSC80251G1D–16CA	ROMless	16 MHz, Commercial 0° to 70°C, PDIL 40
TSC80251G1D–16CB	ROMless	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G1D–16CED	ROMless	16 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack (1)
TSC80251G1D–16IA	ROMless	16 MHz, Industrial –40° to 85°C, PDIL 40
TSC80251G1D–16IB	ROMless	16 MHz, Industrial –40° to 85°C, PLCC 44

Low Voltage Versions 2.7 to 5.5 V, Commercial

TEMIC Part Number (2)	ROM	Description
TSC80251G1D–L12CB	ROMless	12 MHz, Commercial, PLCC 44
TSC80251G1D–L12CED	ROMless	12 MHz, Commercial, VQFP 44, Dry pack (1)

13.2. TSC83251G1D Mask ROM (Step D)

High Speed Versions 4.5 to 5.5 V, Commercial and Industrial

TEMIC Part Number (2)	ROM	Description
TSC251G1Dxxx–24CA	16K MaskROM	24 MHz, Commercial 0° to 70°C, PDIL 40
TSC251G1Dxxx–24CB	16K MaskROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G1Dxxx–24CED	16K MaskROM	24 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack (1)
TSC251G1Dxxx–16CA	16K MaskROM	16 MHz, Commercial 0° to 70°C, PDIL 40
TSC251G1Dxxx–16CB	16K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G1Dxxx–16CED	16K MaskROM	16 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack (1)
TSC251G1Dxxx–16IA	16K MaskROM	16 MHz, Industrial –40° to 85°C, PDIL 40
TSC251G1Dxxx–16IB	16K MaskROM	16 MHz, Industrial –40° to 85°C, PLCC 44

Low Voltage Versions 2.7 to 5.5 V, Commercial

TEMIC Part Number (2)	ROM	Description
TSC251G1Dxxx–L12CB	16K MaskROM	12 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G1Dxxx–L12CED	16K MaskROM	12 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack (1)

Notes:
1. *Dry Pack mandatory for VQFP package.*
2. *xxx: means ROM code, is Cxxx in case of encrypted code.*

13.3. TSC87251G1A OTP (Step A)

High Speed Versions 4.5 to 5.5 V, Commercial and Industrial

TEMIC Part Number	ROM	Description
TSC87251G1A–16CA	16K OTP ROM	16 MHz, Commercial 0° to 70°C, PDIL 40
TSC87251G1A–16CB	16K OTP ROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G1A–16IA	16K OTP ROM	16 MHz, Industrial –40° to 85°C, PDIL 40
TSC87251G1A–16IB	16K OTP ROM	16 MHz, Industrial –40° to 85°C, PLCC 44

13.4. TSC87251G1A EPROM – UV Window package (Step A)

High Speed Versions 4.5 to 5.5 V, Industrial

TEMIC Part Number	ROM	Description
TSC87251G1A–16IC	16K EPROM	16 MHz, Industrial –40° to 85°C, window CQPJ 44

13.5. Options (Please consult TEMIC sales)

- ROM code encryption
- Tape & Real or Dry Pack
- Known good dice
- Ceramic packages
- Extended temperature range: –55°C to +125°C

13.6. Starter Kit

TEMIC Part Number	Description
TSC80251–SK	TSC80251 Starter Kit

13.7. Product Marking

Mask ROM versions

TEMIC
Customer Part number
Temic Part number
INTEL'97
YYWW . Lot Number

ROMless versions

TEMIC
Temic Part number
INTEL'97
YYWW . Lot Number

OTP versions

TEMIC
Temic Part number
INTEL'95
YYWW . Lot Number