AM / FM - PLL

Description

The U4285BM is an integrated circuit in BICMOS technology for frequency synthesizer. It performs all the functions of a PLL radio tuning system and is controlled by I²C bus. The device is designed for all frequency synthesizer applications of radio receivers, as well as RDS (Radio Data System) applications.

Features

- Reference oscillator up to 15 MHz
- Two programmable 16 bit dividers adjustable from 2 to 65535
- Fine tuning steps:
  AM ≧ 1 kHz
  FM ≧ 2 kHz
- 4 programmable switching outputs (open drain up to 10 V)
- Few external component requirements due to integrated loop-push-pull stage for AM/FM
- High signal/noise ratio

Block Diagram

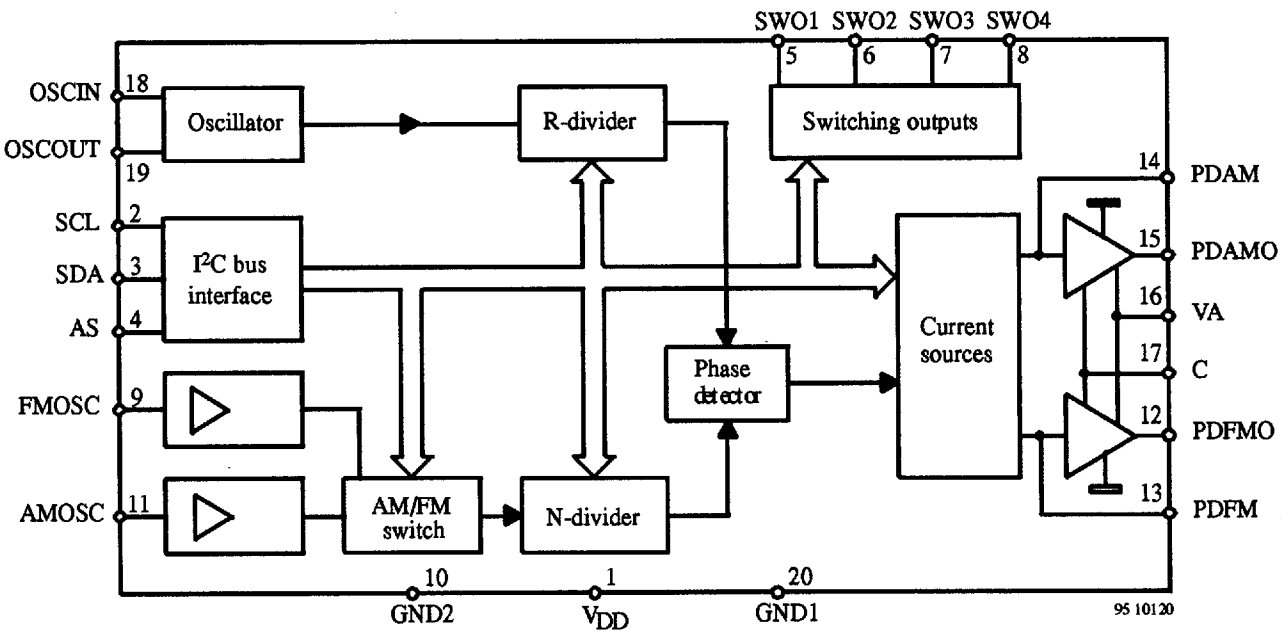
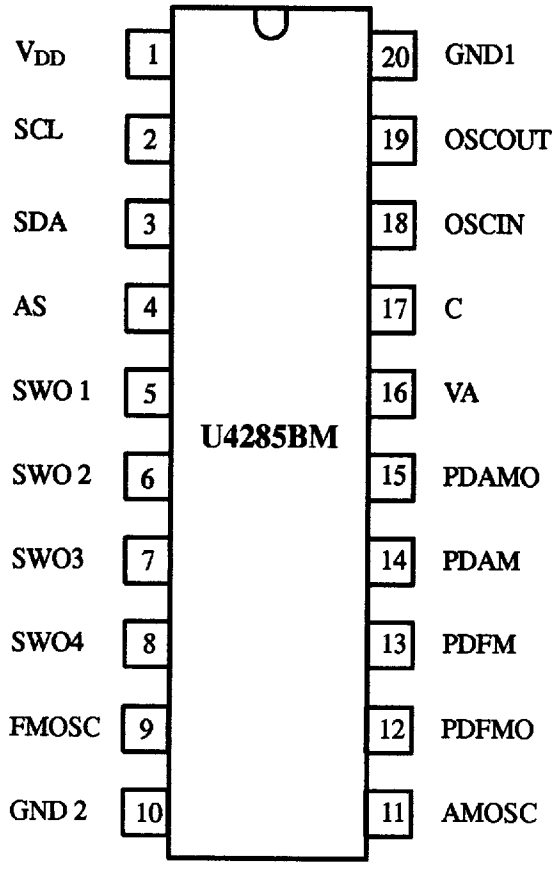


Figure 1

U4285BM

Pin Description



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Pin	Symbol	Function
1	V_{DD}	Supply voltage
2	SCL	I^2C bus clock
3	SDA	I^2C bus data
4	AS	Address selection
5	SWO 1	Switching output 1
6	SWO 2	Switching output 2
7	SWO3	Switching output 3
8	SWO4	Switching output 4
9	FMOSC	FM oscillator input
10	GND 2	Ground 2 (analogue)
11	AMOSC	AM oscillator input
12	PDFMO	FM analogue output
13	PDFM	FM current output
14	PDAM	AM current output
15	PDAMO	AM analogue output
16	VA	Analogue supply voltage
17	C	Capacitor
18	OSCIN	Oscillator input
19	OSCOUT	Oscillator output
20	GND1	Ground 1 (digital)

Functional Description

The U4285BM is controlled via the 2-wire I^2C bus. For programming there are one module address byte, two subaddress bytes and five data bytes.

The module address contains a programmable address bit A 1 which with address select input AS (Pin 4) makes it possible to operate two U4285BM in one system. If bit A 1 is identical with the status of the address select input AS, the chip is selected .

The subaddress determines which one of the data bytes is transmitted first. If subaddress of R-divider is transmitted, the sequence of the next data bytes is DB 0 (Status), DB 1 and DB 2.

If subaddress of N-divider is transmitted, the sequence of the next data bytes is DB 3 and DB 4. The bit organisation of the module address, subaddress and 5 data bytes are shown in figure 2.

Each transmission on the I^2C bus begins with the "START"- condition and has to be ended by the "STOP"- condition (see figure 3).

The integrated circuit U4285BM has two separate inputs for AM and FM oscillator. Pre-amplified AM and FM signals are fed to the 16 bit N-divider via AM/FM switch. AM/FM switch is controlled by software. Tuning steps can be selected by 16 bit R-divider. Further there is a digital memory phase detector. There are two separate current sources for AM and FM amplifier (charge pump) as given in electrical characterisitics. It allows independent adjustment of gain, whereby providing high current for high speed tuning and low current for stable tuning.

Bit Organisation

	MSB							LSB
Module address	1	1	0	0	1	0	0/1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Subaddress (R-divider)	X	X	X	X	0	1	X	X

Subaddress (N-divider)	X	X	X	X	1	1	X	X

	MSB							LSB
Data byte 0 (Status)	SWO1	SWO2	SWO3	SWO4	AM/ FM	PD ANA	PD POL	PD CUR
	D7	D6	D5	D4	D3	D2	D1	D0

Data byte 1	2^{15}	R-divider	2^{8}

Data byte 2	2^{7}	R-divider	2^{0}

Data byte 3	2^{15}	N-divider	2^{8}

Data byte 4	2^{7}	N-divider	2^{0}

	LOW	HIGH
AM/FM	FM-operation	AM-operation
PD - ANA	PD analogue	TEST
PD - POL	Negative polarity	Positive polarity
PD - CUR	Output current 2	Output current 1

Figure 2

Transmission protocol

	MSB LSB										
S	Address A7 A0	A	Subaddress R-divider	A	Data 0	A	Data 1	A	Data 2	A	P

	MSB LSB								
S	Address A7 A0	A	Subaddress N-divider	A	Data 3	A	Data 4 A	A	P

S = Start P = Stop A = Acknowledge

Figure 3

Absolute maximum ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pin 1	V_{DD}	-0.3 to +6	V
Input voltage	Pins 2, 3, 4, 9, 11, 18 and 19	V_I	-0.3 to V_{DD} + 0.3	V
Output current	Pins 3, 5, 6, 7 and 8	I_O	-1 to +5	mA
Output drain voltage	Pins 5, 6, 7 and 8	V_{OD}	10 *	V
Analogue supply voltage with 220 Ω seriell resistance 2 minutes [2]	Pin 16	V_A V_A	6 to 10 * 24	V V
Output current	Pins 12 and 15	I_{AO}	-1 to +20	mA
Ambient temperature range		T_{amb}	-30 to +85	°C
Storage temperature range		T_{stg}	-40 to +125	°C
Junction temperature		T_j	125	°C
Electrostatic handling		$\pm V_{ESD}$	tbd	V

[2] corresponding our application circuit (page 7)
* will bemodified to 15 V

Thermal resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	160	K/W

Electrical Characteristics

V_{DD} = 5 V, V_A = 10 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 1	V_{DD}	4.5	5.0	5.5	V
Quiescent supply current	AM-mode Pin 1 FM-mode	I_{DD}		4.0 4.0	7.0 7.0	mA
FM input sensitivity, R_G = 50 Ω FMOSC						
f_i = 70 to 120 MHz	Pin 9	V_{SFM}	40			mV
f_i = 160 MHz	Pin 9	V_{SFM}	150			mV
AM input sensitivity, R_G = 50 Ω AMOSC						
f_i = 0.6 to 35 MHz	Pin 11	V_{SAM}	40			mV
Oscillator input sensitivity, R_G = 50 Ω OSCIN						
f_i = 0.1 to 15 MHz	Pin 18	V_{SOSC}	100			mV
Switching output SWO 1, SWO 2, SWO 3, SWO 4 (open drain)						
Output voltage LOW Output leakage current HIGH	Pins 5, 6, 7 and 8 I_L = 1 mA Pins 5, 6, 7 and 8 V5, V6, V7, V8 = 10 V	V_{SWOL} I_{OHL}		100	400 100	mV nA
Phase detector PDFM						
Output current 1 Output current 2	Pin 13 Pin 13	$\pm I_{PDFM}$ $\pm I_{PDFM}$	400 100	500 125	600 150	µA µA
Leakage current	Pin 13	$\pm I_{PDFML}$			20	nA
Phase detector PDAM						
Output current 1 Output current 2	Pin 14 Pin 14	$\pm I_{PDAM}$ $\pm I_{PDAM}$	75 20	100 25	125 30	µA µA
Leakage current	Pin 14	$\pm I_{PDAML}$			20	nA
Analogue output PDFMO, PDAMO						
Saturation voltage LOW HIGH	Pins 12 and 15 I = 15 mA	V_{satL} V_{satH}	 9.5	200 9.95	400	mV V
I²C bus SCL, SDA, AS						
Input voltage HIGH LOW	Pins 2, 3 and 4	V_{iBUS}	3.0 0		V_{DD} 1.5	V V
Output voltage Acknowledge LOW	Pin 3 I_{SDA} = 3 mA	V_O			0.4	V
Clock frequency	Pin 2	f_{SCL}			100	kHz
Rise time SDA, SCL	Pins 2 and 3	t_r			1	µs
Fall time SDA, SCL	Pins 2 and 3	t_f			300	ns
Period of SCL HIGH LOW	Pin 2 HIGH LOW	t_H t_L	4.0 4.7			µs µs

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Setup time						
Start condition		t_{sSTA}	4.7			µs
Data		t_{sDAT}	250			ns
Stop condition		t_{sSTOP}	4.7			µs
Time the bus must be free before a new transmission can be started		t_{wSTA}	4.7			µs
Hold time						
Start condition		t_{hSTA}	4.0			µs
DATA		t_{hDAT}	0			µs

Bus Timing

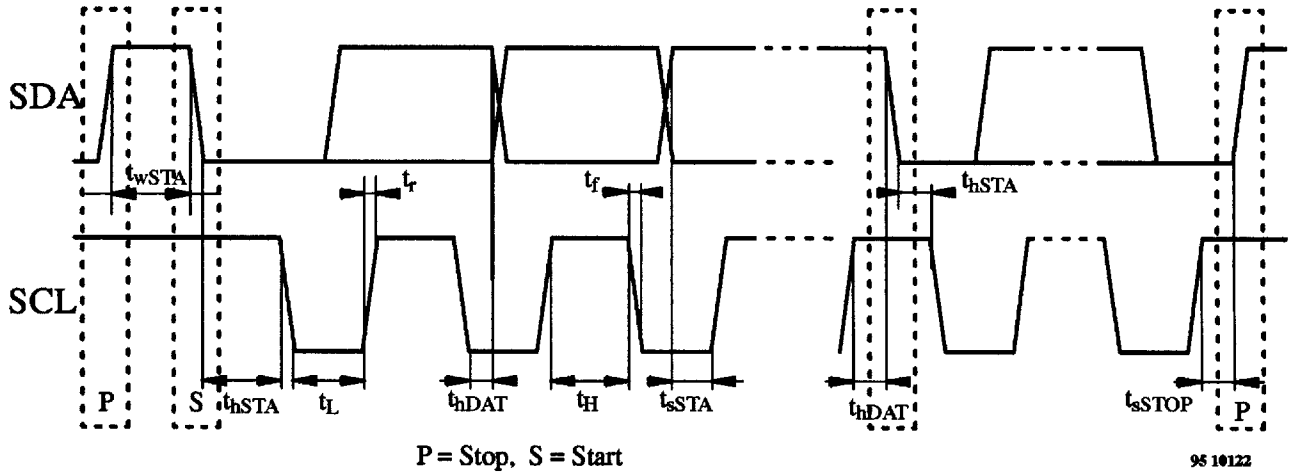


Figure 4

The Following Hints are Recommended

- C_3 = 100 nF should be very close to Pin 1 (V_{DD}) and Pin 20 (GND 1)
- GND 2 (Pin 10 - analogue ground) and GND 1 (Pin 20 - digital ground) must be connected according to figure 6
- 4 MHz quartz must be very close to Pin 18 and Pin 19
- Components of the charge pump (C_1/R_1 for AM and C_2/R_2 for FM) should be very close to Pin 14 with respect to Pin 13.

Application Circuit

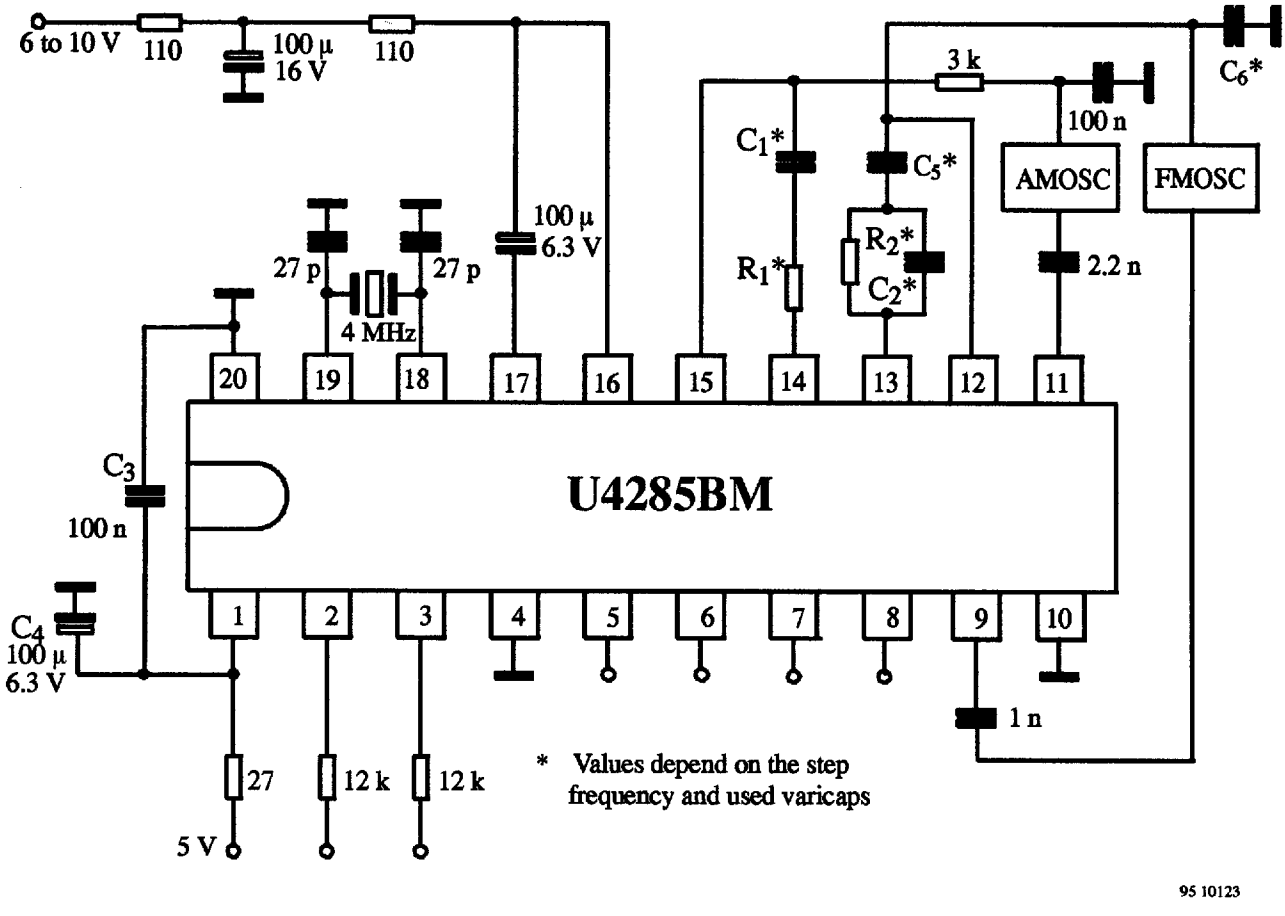


Figure 5

PCB-Layout

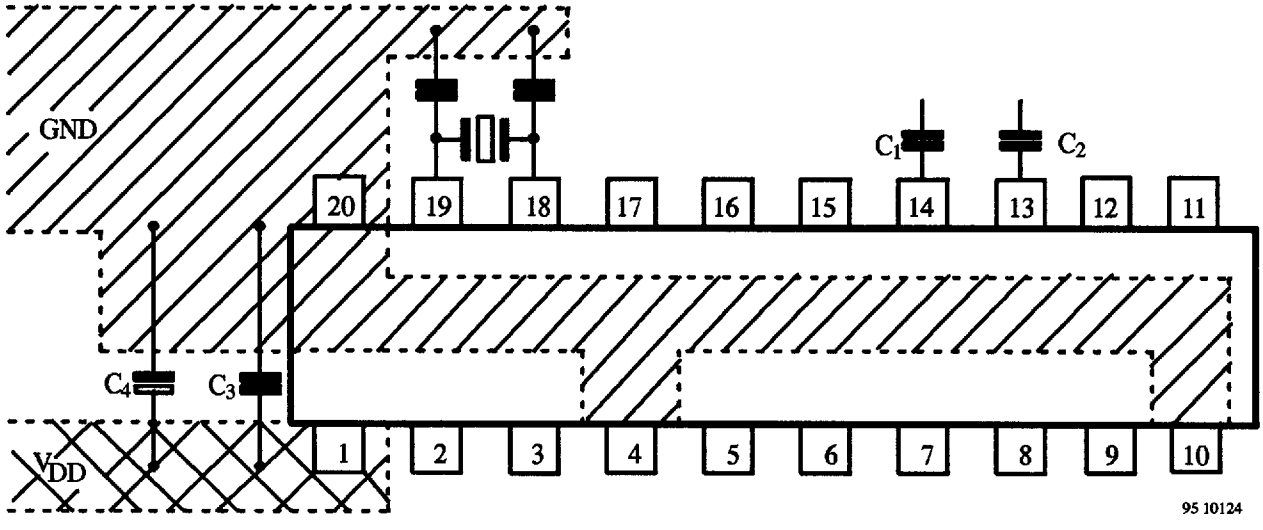


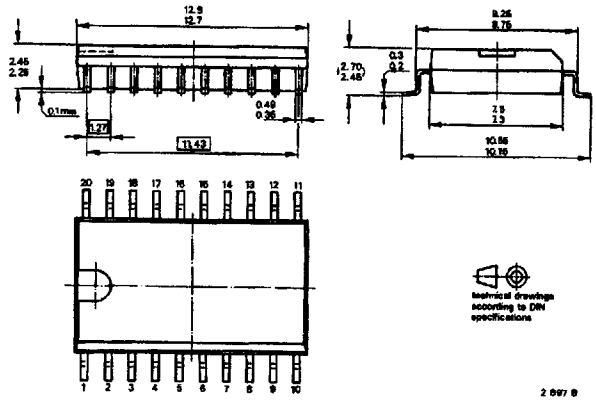
Figure 6

Ordering and Package Information

Extended Type Number	Package	Remarks
U4285BM-BFP	SO 20 plastic	
U4285BM-BFPG3	SO 20 plastic	Taping according to IEC-286-3
U4285BM-BFS	SSO 20 plastic	
U4285BM-BFSG3	SSO 20 plastic	Taping according to IEC-286-3

Dimensions in mm

Package: SO 20



Package: SSO 20