NEC

MOS FIELD EFFECT TRANSISTOR

μPA1725

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

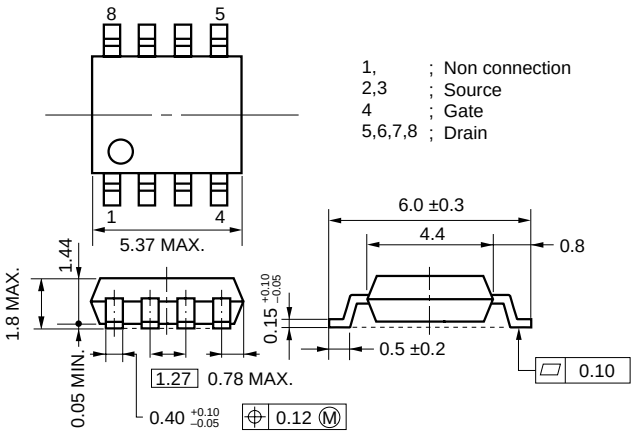
DESCRIPTION

This μPA1725 is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and so on.

FEATURES

- 2.5-V gate drive and low on-resistance
  $R_{DS(on)1}$ = 21.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 3.5 A)
  $R_{DS(on)2}$ = 22.0 mΩ MAX. (V_{GS} = 4.0 V, I_D = 3.5 A)
  $R_{DS(on)3}$ = 30.0 mΩ MAX. (V_{GS} = 2.5 V, I_D = 3.5 A)
- Low C_{iss} : C_{iss} = 950 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



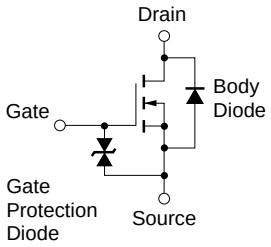
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1725G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12	V
Drain Current (DC)	$I_{D(DC)}$	±7	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±28	A
Total Power Dissipation (T_A = 25°C) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 1200 mm^2 x 2.2mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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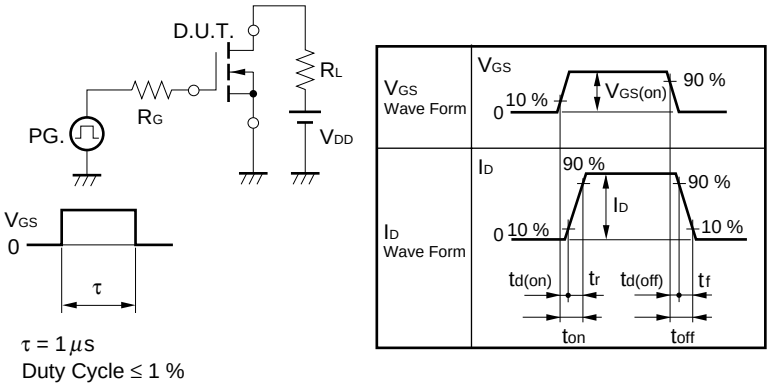
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

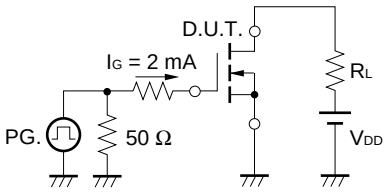
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 3.5 A		16.5	21.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 3.5 A		17.0	22.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 2.5 V, I_D = 3.5 A		22.0	30.0	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	0.5	1.0	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.5 A	5.0	11.0		S
Drain Leakage Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		950		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		310		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		160		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 3.5 A		30		ns
Rise Time	t_r	$V_{GS(on)}$ = 4.5 V		120		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 10 V		70		ns
Fall Time	t_f	R_G = 10 Ω		70		ns
Total Gate Charge	Q_G	I_D = 7 A		9.6		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 16 V		1.7		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 4.5 V		4.1		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 7 A, V_{GS} = 0 V		0.8		V
Reverse Recovery Time	t_{rr}	I_F = 7 A, V_{GS} = 0 V		40		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		27		nC

TEST CIRCUIT 2 SWITCHING TIME



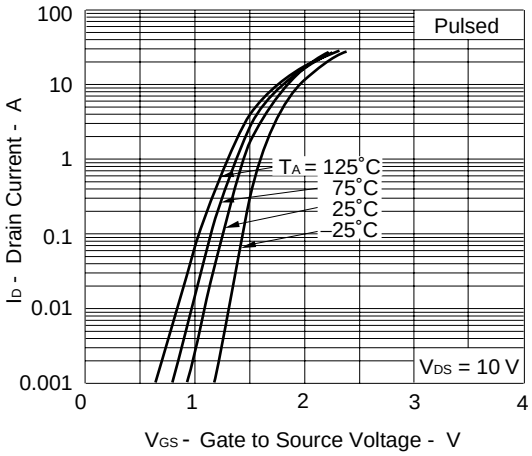
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 3 GATE CHARGE

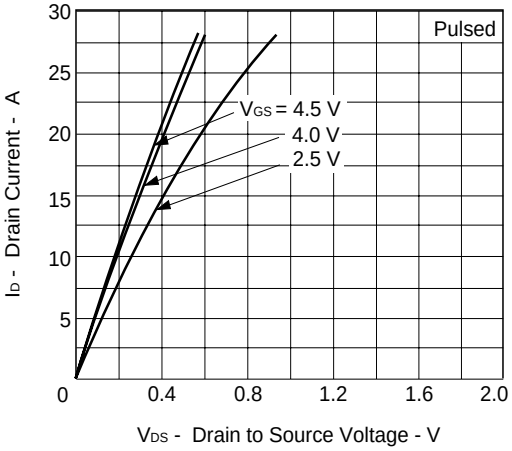


TYPICAL CHARACTERISTICS (T_A = 25 °C , All terminals are connected.)

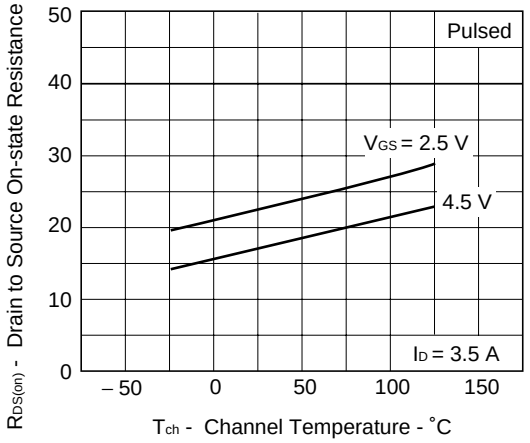
FORWARD TRANSFER CHARACTERISTICS



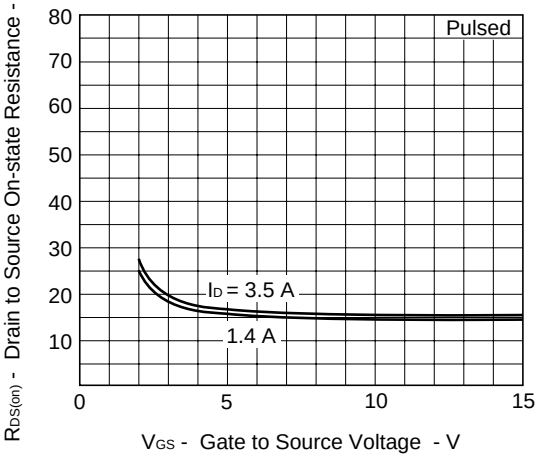
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



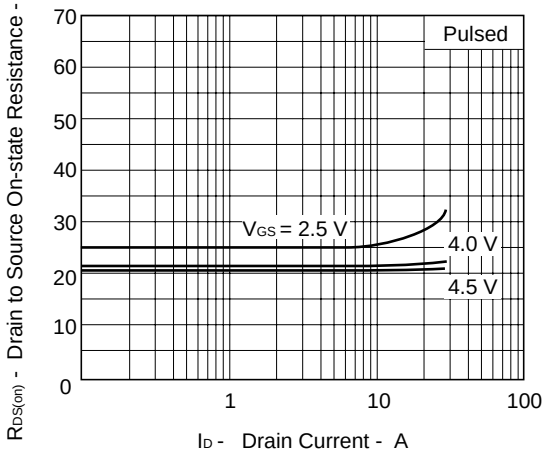
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



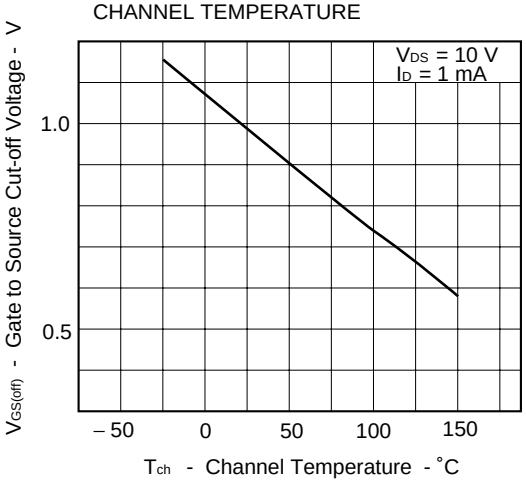
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



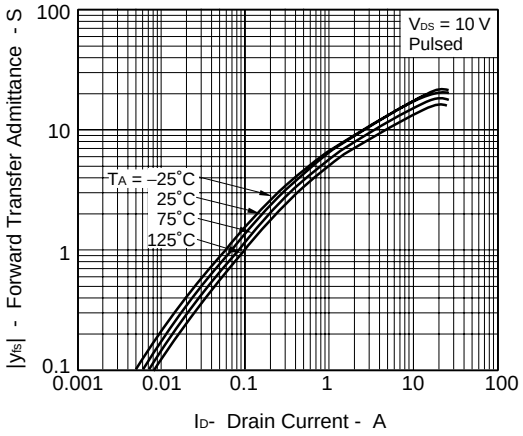
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



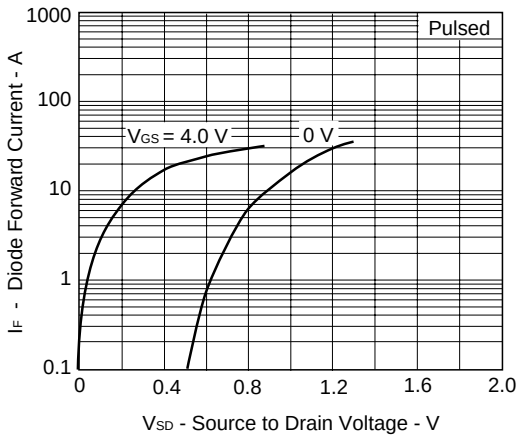
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



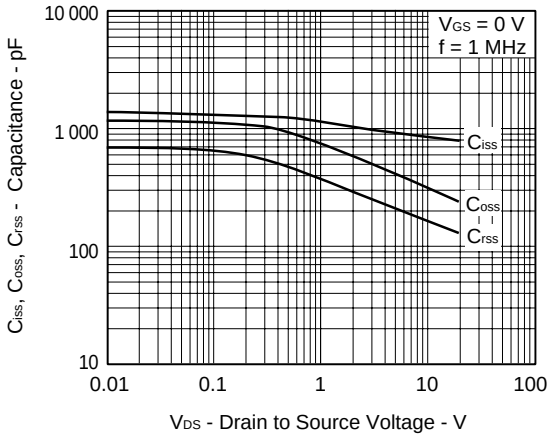
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



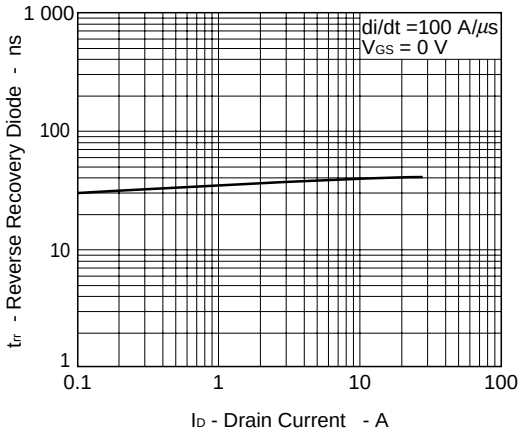
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



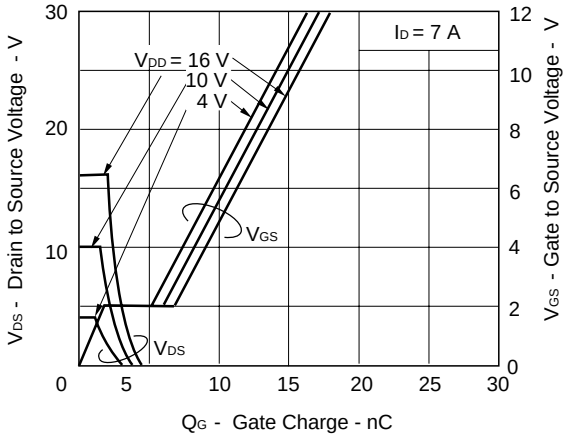
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



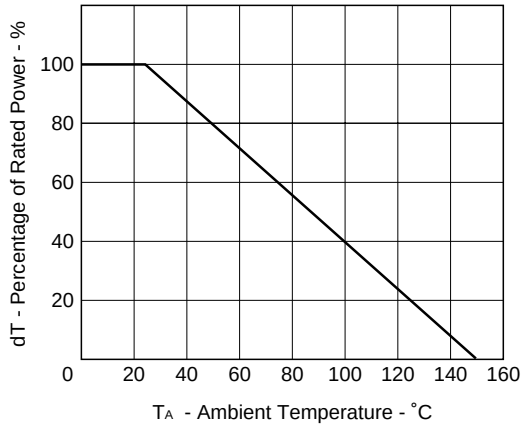
REVERSE RECOVERY TIME vs. DRAIN CURRENT



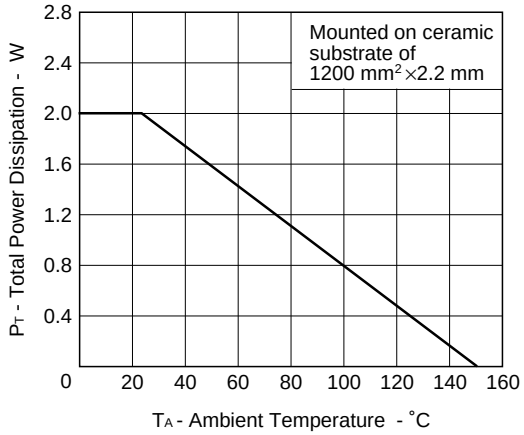
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



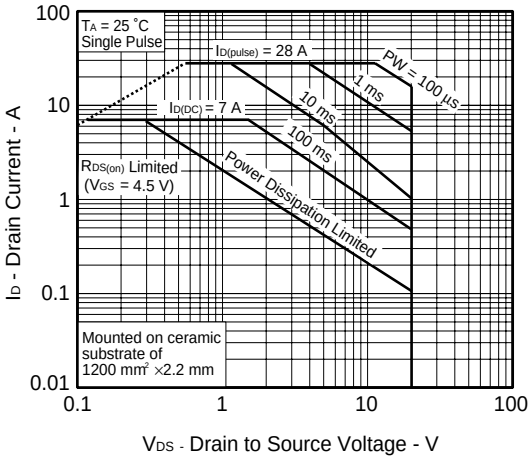
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



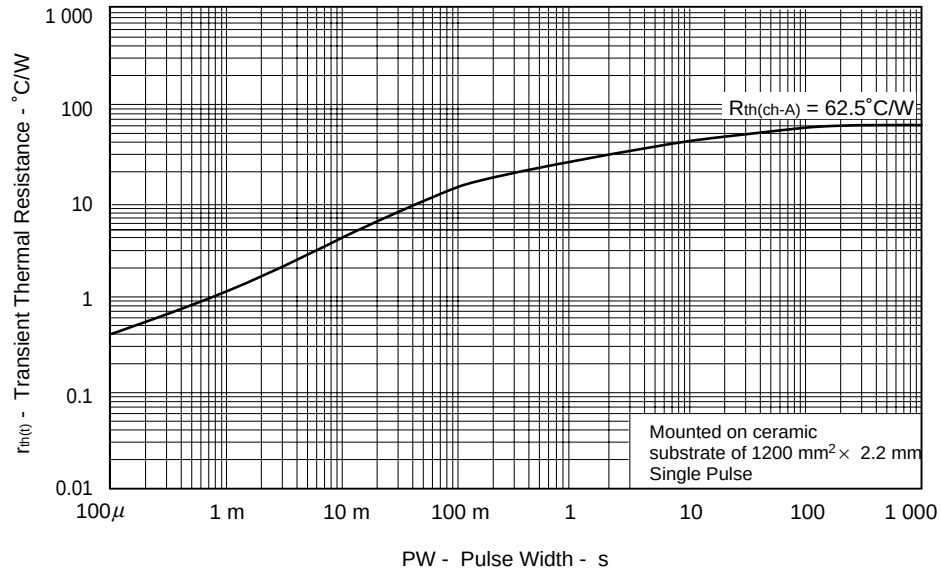
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



★ FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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