YAMAHA LSI

YM7405B

IDNDCH

ISDN basic access interface with D channel packet

■ GENERAL DESCRIPTION

The YM7405B is an upgraded version of the YM7405 chip with the ISDN user-network interface function (digital four-wire time-division full-duplex operation).
In only one chip, the YM7405B is compatible with ITU-T Recommendation I.430, Q.920 and Q.921 [1992 edition], supports Layer 1 (physical layer) and Layer 2 (LAP-D protocol), and is making it suitable for D channel packet mode terminals.
The YM7405B supports ETSI (European Telecommunications Standards Institute) ETS 300 012 [April 1992] and ETS 300 125 [September 1991] also by setting it ETSI operation mode. (Refer to "YM7405B APPLICATION NOTE")
The YM7405B also includes the Layer 3 processor interface function and analog driver and receiver in an 80-pin QFP or 100-pin TQFP package and has great potential for mounting and functional designing of terminal equipments (TE) and PBX (NT2) trunk circuits.

■ FEATURES

1) Layer 1

- Compatible with ITU-T Recommendation I.430 [1992 edition] and TTC Standard JT-I430 [1993 edition]. (default)
- Supports ETSI ETS 300 012 [April 1992] operation mode (Refer to "YM7405B APPLICATION NOTE").
- Four-wire time-division full-duplex 192 Kbps transmission.
- Interface structure: 2B+D (B=64 Kbps, D=16 Kbps).
- Frame assembling and disassembling function.
- Collision control (built-in random number (Ri) reset), priority control (built-in retransmission control), and state transition control.
- Multiframing capability (S channel and Q channel access).
- B channel I/O clock selection function. (Internal clock mode/External clock mode)
- B channel selection function.
- Loop-back test function (for test and maintenance).
- Built-in analog driver and receiver.
- Leased line capability (JT-I430-a).

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YM7405B CATALOG
CATALOG No.:LSI-217405B2
1996.1

2) Layer 2

- Compatible with ITU-T Recommendation Q.920 and Q.921 [1992 edition] and TTC Standard JT-Q920 and JT-Q921 [1993 edition]. (default)
- Supports ETSI ETS 300 125 [September 1991] operation mode (Refer to "YM7405B APPLICATION NOTE").
- HDLC frame control (Flag control, FCS generation/checking, automatic zero insertion/ deletion, abort pattern transmission/detection, etc.).
- LAP-D status control (sequence control, flow control, SAPI control).
- Built-in timer for time-out check.
- Multi-link capability (circuit switching, packet switching).
- Automatic assigned TEI/non-automatic assigned TEI (VC/PVC) capability.
- XID frame support.

3) Layer 3 interface function

- Connectable to 8-bit or 16-bit microprocessor (8086 family, Z80 family, 6800 family and 68000 family)
- Data transfer method: DMA transfer.
- Primitive logical interface.

4) Power-down mode (low-power operation)

5) CMOS technology with single +5 volt supply

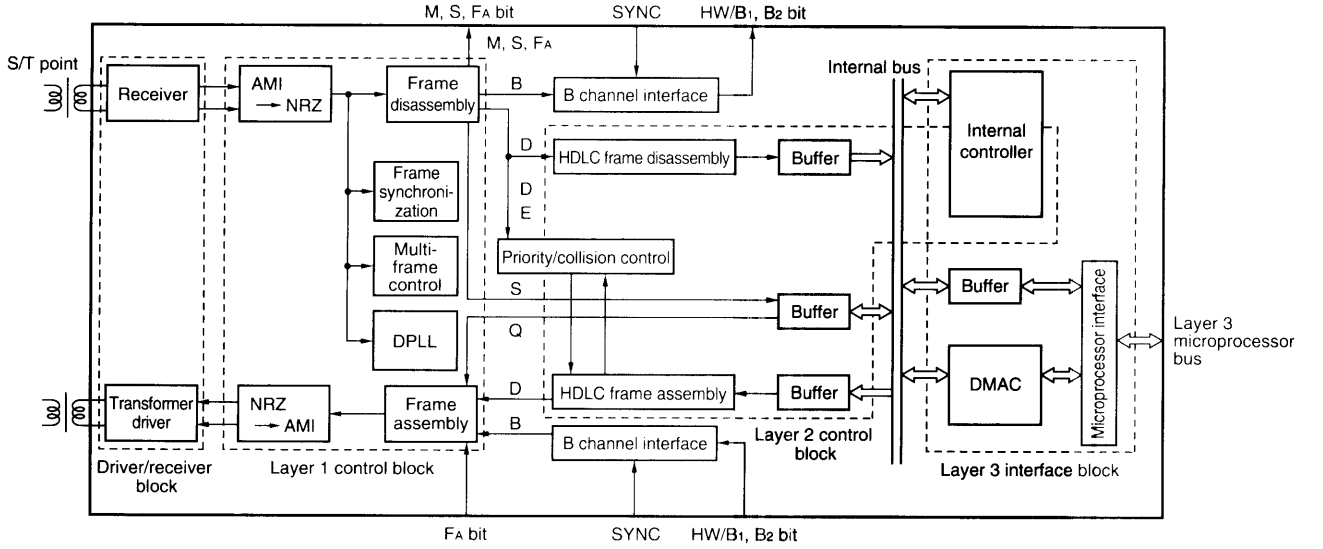
6) 80-pin QFP or 100-pin TQFP

7) YM7405 pin and software compatible

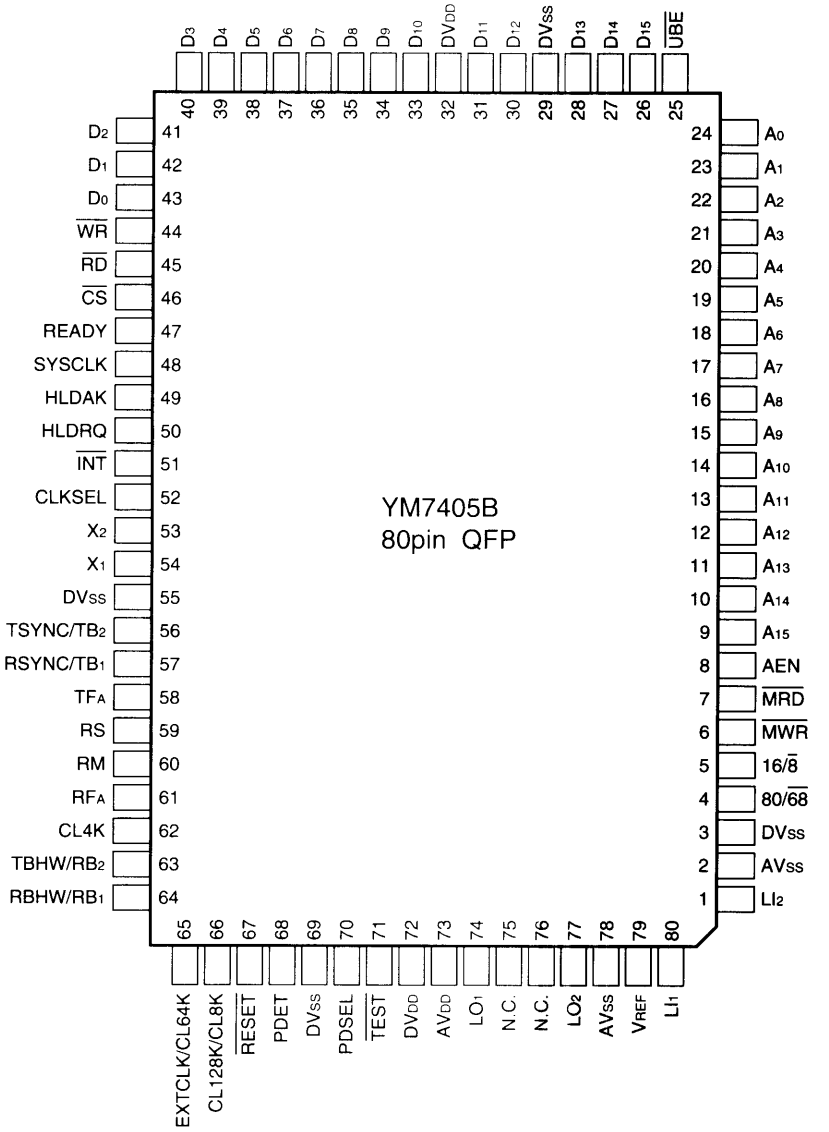
■ SPECIFICATIONS

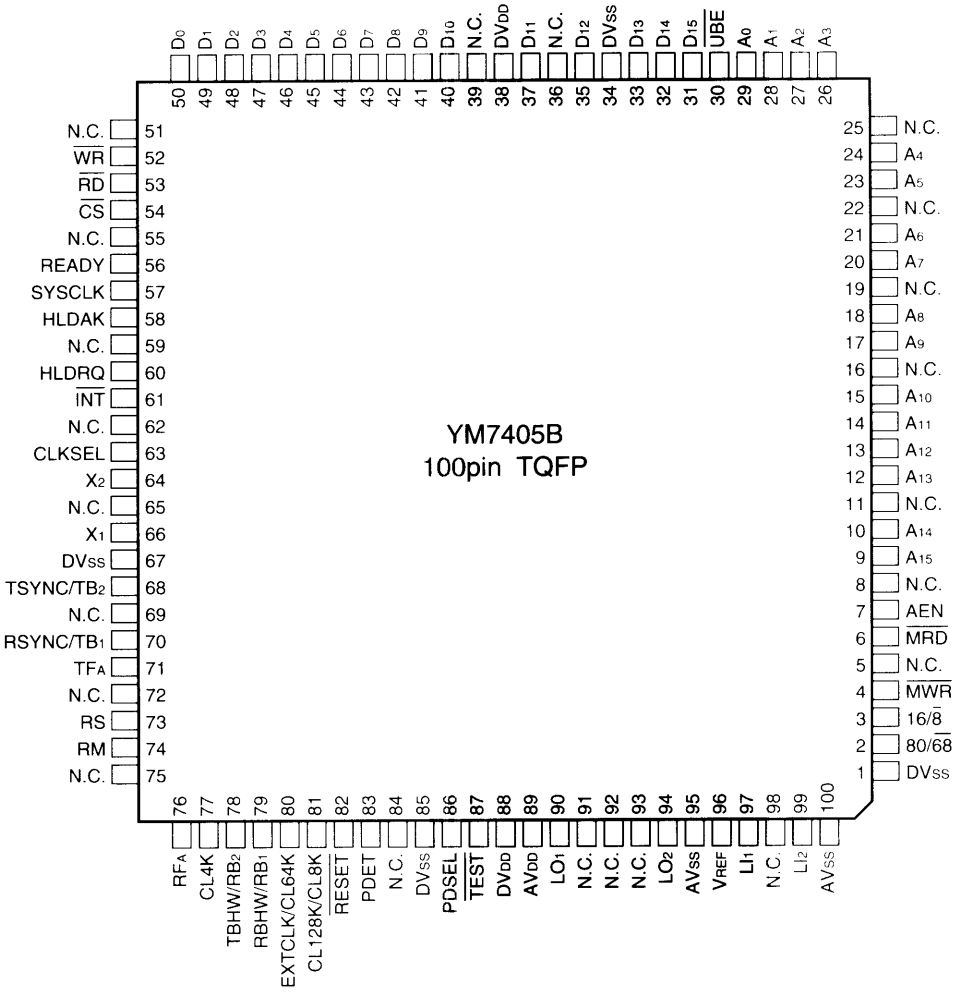
	Item Number	Item	Specifications	Remarks
Layer 1	1	Transmission medium	Conductive balanced cable (4-wire...T wire, R wire)	
	2	Maximum transmission distance	Compatible with ITU-T I.430	
	3	Connection method	Transformer coupling, 4-wire	For transmission and reception
	4	Transmission capacity	B + B + D = 64 + 64 + 16 Kbps	
	5	Encoding algorithm	100% AMI	
	6	Bit rate	192 Kbps	
	7	Frame synchronization	Transmission symbol violation (14-bit algorithm)	
	8	Timing recovery/synchronization	DPLL	
	9	Frame structure	Compatible with ITU-T I.430	
	10	D channel collision	Echo bit check method	
	11	Multiframing control	Q channel, S channel microprocessor interface	
	12	B channel interface	Internal/external clock synchronization can be selected. 128 Kbps to 2 Mbps transmission possible when external clock selected.	2 Mbps highway interface capability
	13	Leased line interface	Compatible with TTC JT-I430-a	
Layer 2	1	Automatic zero insertion/deletion	Automatic zero insertion after all sequences of five contiguous "1" bits. Automatic zero deletion when receiving data.	
	2	Automatic flag generation/detection	Automatic generation/detection of opening flag/closing flag	
	3	FCS generation/checking	Generation and checking of polynomial $X^{16}+X^{12}+X^{5}+1$	
	4	Abort pattern transmission/detection	Transmission or detection of seven or more contiguous "1" bits	
	5	Invalid frame detection and abort	• Frame not bounded by two flags • FCS error frame • Frame which has an address field of 1 octet • Frame which is not an integer multiple	
	6	SAPI, TEI address control	• Supports data link for TEI assignment, broadcast data link, and data link for sending/receiving multiple Layer 3 messages • Multi-link capability (circuit switching, packet switching)	Non-automatic assigned TEI support
	7	Sequence control Flow control	• Send/receive sequence number and busy state control by S frame and I frame • Retransmission procedure on expiry of timer T200 and T203	XID frame support
	8	Frame structure	Compatible with ITU-T Q.921	
Layer 3 interface	1	DMA transfer	Send and receive 2 channels	
	2	Program I/O	Send and receive both have an 8-byte FIFO buffer	

■ BLOCK DIAGRAM



■ PIN ASSIGNMENTS




YM7405B
100pin TQFP
1 DVSS
2 80/68
3 16/8
4 MWR
5 N.C.
6 MRD
7 AEN
8 N.C.
9 A15
10 A14
11 N.C.
12 A13
13 A12
14 A11
15 A10
16 N.C.
17 A9
18 A8
19 N.C.
20 A7
21 A6
22 N.C.
23 A5
24 A4
25 N.C.
26 A3
27 A2
28 A1
29 A0
30 UBE
31 D15
32 D14
33 D13
34 DVSS
35 D12
36 N.C.
37 D11
38 DVDD
39 N.C.
40 D10
41 D9
42 D8
43 D7
44 D6
45 D5
46 D4
47 D3
48 D2
49 D1
50 D0
51 N.C.
52 WR
53 RD
54 CS
55 N.C.
56 READY
57 SYSCLK
58 HLDAK
59 N.C.
60 HLDRQ
61 INT
62 N.C.
63 CLKSEL
64 X2
65 N.C.
66 X1
67 DVSS
68 TSYNC/TB2
69 N.C.
70 RSYNC/TB1
71 TFA
72 N.C.
73 RS
74 RM
75 N.C.
76 RFA
77 CL4K
78 TBHW/RB2
79 RBHW/RB1
80 EXTCLK/CL64K
81 CL128K/CL8K
82 RESET
83 PDET
84 N.C.
85 DVSS
86 PDSEL
87 TEST
88 DVDD
89 AVDD
90 LO1
91 N.C.
92 N.C.
93 N.C.
94 LO2
95 AVSS
96 VREF
97 LI1
98 N.C.
99 LI2
100 AVSS

■ PIN FUNCTIONS

1. Common section

80-pin QFP	100-pin TQFP	Pin name	I/O	Function	Remarks
32, 72	38, 88	DV_{DD}	PWR	+5 V digital power supply (±5%)	
3, 29, 55, 69	1, 34, 67, 85	DV_{SS}	GND	Digital ground	
73	89	AV_{DD}	PWR	+5 V analog power supply (±5%)	
2, 78	95, 100	AV_{SS}	GND	Analog ground	
54	66	X_1	IN	Connected to 12.288 MHz crystal oscillator. External clock can be input.	
53	64	X_2	OUT	Connected to 12.288 MHz crystal oscillator.	
67	82	$\overline{RESET}$	IN	System reset input (reset when LOW). Over 250 µs "L" input sets all internal registers, flags, counters, etc. to default value.	
71	87	$\overline{TEST}$	IN	Test mode input. Usually fixed at HIGH.	Pull-up resistor
70	86	PDSEL	IN	Power supply detection mode selection.	
68	83	PDET	IN	Power supply detection from DSU.	Pull-down resistor

2. Transformer interface section

80-pin QFP	100-pin TQFP	Pin name	I/O	Function	Remarks
80	97	LI_1	IN	S/T bus input pin Inputs S/T bus data via a transformer.	
1	99	LI_2	OUT	S/T bus input pin Inputs S/T bus data via a transformer.	
79	96	V_{REF}	IN	S/T bus reference input pin Sets S/T bus reference voltage.	
74	90	LO_1	OUT	S/T bus driver output pin (+) Connects to S/T bus drive transformer.	
77	94	LO_2	OUT	S/T bus driver output pin (–) Connects to S/T bus drive transformer.	

3. Layers 1 and 2 control section

80-pin QFP	100-pin TQFP	Pin name	I/O	Function	Remarks
52	63	CLKSEL	IN	Selects internal/external clock mode for B channel data send/receive. HIGH or open : Internal clock mode LOW : External clock mode	Pull-up resistor

[Internal clock mode] CLKSEL pin "HIGH" or open.

80-pin QFP	100-pin TQFP	Pin name	I/O	Function	Remarks
†64	†79	RB_1	OUT	Receive B channel data output pin Used in internal clock mode. Internal register REG 1 selects B channel to be connected. Data rate: 64 Kbps	
†63	†78	RB_2	OUT		
59	73	RS	OUT	S bit data output pin	
61	76	RF_A	OUT	F_A bit data output pin	
60	74	RM	OUT	M bit data output pin	
†57	†70	TB_1	IN	Send B channel data input pin Used in internal clock mode. Internal register REG 1 selects B channel to be connected. Data rate: 64 Kbps	Pull-up resistor
†56	†68	TB_2	IN		
58	71	TF_A	IN	F_A bit data input pin Used only when TF_A pin enabled mode. Connects to RF_A pin when TF_A pin enabled and multi-framing not used.	Pull-up resistor
†65	†80	CL64K	OUT	Outputs a 64 kHz clock synchronized with CL8K. Used to generate the bit timing of RB_1, RB_2, TB_1, and TB_2.	
†66	†81	CL8K	OUT	Outputs the 8 kHz clock extracted from the receive data. Used to generate the first bit timing of RB_1, RB_2, TB_1, and TB_2.	
62	77	CL4K	OUT	Outputs the 4 kHz frame synchronization signal extracted from the receive data. Used for multiframing.	

† Changes as shown on next page in external clock mode (when "LOW" selected at CLKSEL pin).

[External clock mode] CLKSEL pin "LOW".

80-pin QFP	100-pin TQFP	Pin name	I/O	Function	Remarks
64	79	RBHW	OUT (O.D.)	In the external clock mode, outputs the receive B channel data synchronized with EXTCLK.	Open drain
63	78	TBHW	IN	In the external clock mode, inputs the send B channel data synchronized with EXTCLK.	
59	73	RS	OUT	S bit data output pin	
61	76	RFA	OUT	FA bit data output pin	
60	74	RM	OUT	M bit data output pin	
57	70	RSYNC	IN	In the external clock mode, inputs the 8 kHz synchronization pulse for the receive B channel data.	Pull-up resistor
56	68	TSYNC	IN	In the external clock mode, inputs the 8 kHz synchronization pulse for the send B channel data.	Pull-up resistor
58	71	TFA	IN	FA bit data input pin Used only when TFA pin enabled mode. Connects to RFA pin when TFA pin enabled and multiframing not used.	Pull-up resistor
65	80	EXTCLK	IN	In the external clock mode, inputs the clock for B channel data send/receive. Operates at 128 kHz to 2 MHz.	
66	81	CL128K	OUT	In the external clock mode, outputs the 128 kHz clock extracted from the receive data. Used to synchronize RSYNC, TSYNC, and EXTCLK.	
62	77	CL4K	OUT	Outputs the 4 kHz frame synchronization signal extracted from the receive data. Used for multiframing.	

4. Layer 3 interface section

80-pin QFP	100-pin TQFP	Pin name	I/O	Function	Remarks
9 – 23	9, 10 12 – 15 17, 18 20, 21 23, 24 26 – 28	A_{15} – A_1	IN/OUT	During program I/O transfer with Layer 3 microprocessor, accept addresses for I/O register and primitive selection. In the DMA mode, these pins output the DMA addresses.	
26 – 28 30, 31 33 – 43	31 – 33 35, 37 40 – 50	D_{15} – D_0	IN/OUT	8-bit bidirectional data bus (D_0 – D_7) during program I/O transfer with Layer 3 microprocessor. In the DMA mode, these pins become a 16-bit bidirectional data bus.	When using an 8-bit MPU, pins D_8 to D_{15} must be pulled high.
25	30	$\overline{UBE}$	IN/OUT	Becomes input at program I/O transfer with Layer 3 micro-processor. Only D_0 to D_7 are valid data. In the DMA mode, the signal output from this pin depends on the value input at the 16/$\overline{8}$ pin. • In the 8-bit data bus mode (16/$\overline{8}$="L"), $\overline{UBE}$ always outputs $\overline{A_0}$. • In the 16-bit data bus mode (16/$\overline{8}$="H"), this pin indicates which pins (D_0 – D_7 or D_8 – D_{15}) contain valid data. $\overline{UBE}$ / A_0 / D_0 – D_7 / D_8 – D_{15} L / H / / ✓ H / L / ✓ /	When using an 8-bit MPU, this pin must be pulled high.
24	29	A_0 ($\overline{LBE}$)	IN/OUT	Indicates address A_0 when the Layer 3 microprocessor I/O accesses to the YM7405B during program I/O transfer (input) with the Layer 3 microprocessor. In the DMA mode (output), this pin indicates memory access address A_0. See $\overline{UBE}$.	
44	52	$\overline{WR}$	IN	Indicates that the Layer 3 microprocessor is in a write cycle. When a 6800/68000 is used, this pin connects to the R/$\overline{W}$ signal.	
45	53	$\overline{RD}$	IN	Indicates that the Layer 3 microprocessor is in a read cycle. When a 68000 is used, this pin connects to the $\overline{AS}$ signal. When a 6800 is used, this pin connects to the $\overline{E}$ signal.	
46	54	$\overline{CS}$	IN	This signal selects the YM7405B when the Layer 3 microprocessor sets the control information for I/O and DMA transfer.	
47	56	READY	IN	This signal is used to widen the $\overline{MRD}$ and $\overline{MWR}$ signals output by the YM7405B during DMA transfer when the YM7405B is used with low-speed memory. While the READY signal is LOW, the $\overline{MRD}$ and $\overline{MWR}$ signals remain active low level.	
51	61	$\overline{INT}$	OUT (O.D.)	Interrupt signal from the YM7405B to the Layer 3 microprocessor.	Open drain
6	4	$\overline{MWR}$	OUT	Indicates that the YM7405B is in a write cycle when data is transferred in the DMA mode. At program I/O transfer with the Layer 3 microprocessor, the output of this pin becomes high impedance.	

<table>
<tr><th>80-pin QFP</th><th>100-pin TQFP</th><th>Pin name</th><th>I/O</th><th>Function</th><th>Remarks</th></tr>
<tr><td>7</td><td>6</td><td>$\overline{MRD}$</td><td>OUT</td><td>Indicates that the YM7405B is in a read cycle when data is transferred in the DMA mode.
At program I/O transfer with the Layer 3 microprocessor, the output of this pin becomes high impedance.</td><td></td></tr>
<tr><td>8</td><td>7</td><td>AEN</td><td>OUT</td><td>When data is transferred in the DMA mode, this pin enables the address and outputs it to the system address bus. It is used to disable other system bus drivers.</td><td></td></tr>
<tr><td>49</td><td>58</td><td>HLDAK</td><td>IN</td><td>Inputs the response signal permitting DMA from the Layer 3 microprocessor.</td><td></td></tr>
<tr><td>50</td><td>60</td><td>HLDRQ</td><td>OUT</td><td>Outputs the signal requesting DMA to the Layer 3 microprocessor.</td><td></td></tr>
<tr><td>4</td><td>2</td><td>80/$\overline{68}$</td><td>IN</td><td rowspan="2">Sets the type of Layer 3 microprocessor.<table><tr><th>80/$\overline{68}$</th><th>16/$\overline{8}$</th><th>MPU type</th></tr><tr><td>H</td><td>H</td><td>8086 family (default)</td></tr><tr><td>L</td><td>H</td><td>68000 family</td></tr><tr><td>H</td><td>L</td><td>Z80 family</td></tr><tr><td>L</td><td>L</td><td>6800 family</td></tr></table></td><td rowspan="2">Pull-up resistor</td></tr>
<tr><td>5</td><td>3</td><td>16/$\overline{8}$</td><td>IN</td></tr>
<tr><td>48</td><td>57</td><td>SYSCLK</td><td>IN</td><td>Inputs the Layer 3 microprocessor system clock. Operated by 2 to 10 MHz clock signal.</td><td>Pull-up resistor</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Units
Supply voltage	V_{DD}	− 0.3	+7.0	V
Input voltage	V_{IN}	− 0.3	V_{DD} +0.3	V
Operating temperature range	T_{OP}	0	+70	°C
Storage temperature range	T_{ST}	− 50	+125	°C

(Based on DVss, AVss=0.0 V)

2. Recommended operating conditions

Supply voltage : 5 V ±5% (based on DVss, AVss=0.0 V)
Operating temperature range : 0 – 70°C

3. DC Characteristics

(V_{DD}=5 V ±5%, T_{OP}=0 – 70 °C)

Parameter		Symbol	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	**(Note 1)**	V_{IH}	0.9V_{DD}			V
Low-Level Input Voltage (CMOS)	**(Note 1)**	V_{IL}			0.1V_{DD}	V
High-Level Input Voltage (TTL)	**(Note 2)**	V_{IH}	2.2			V
Low-Level Input Voltage (TTL)	**(Note 2)**	V_{IL}			0.8	V
High-Level Output Voltage (CMOS)	**(Note 3)**	V_{OH}	V_{DD}–0.4			V
Low-Level Output Voltage (CMOS)	**(Note 3)**	V_{OL}			V_{SS}+0.4	V
High-Level Output Voltage (TTL)	**(Note 4)**	V_{OH}	2.7			V
Low-Level Output Voltage (TTL)	**(Note 4)**	V_{OL}			0.4	V
Low-Level Output Voltage (Open-D)	**(Note 5)**	V_{OL}			0.4	V
Leakage Current		I_L	−10		10	µA
Off-State Leakage Current	**(Note 6)**	I_{LZ}	−10		10	µA
Power Supply Current	**(Note 7)**	I_{DD}		25		mA
Analog Power Supply Current	**(Note 7)**	AI_{DD}		5		mA

Note 1: With respect to X1 pin.

Note 2: With respect to other pins (excepting analog pins).

Note 3: Excepting analog pins.
Test Conditions : $|I_{OH}| < 10\mu A$

Note 4: $\overline{MWR}$, $\overline{MRD}$, A15–A0, $\overline{UBE}$, D15–D0, HLDRQ pins.
Test Conditions : I_{OH} = –0.6mA, I_{OL} = 1.2mA
RS, RM, RFA, RB1–RB2, CL64K, CL8K, CL4K, AEN pins
Test Conditions : I_{OH} = –0.2mA, I_{OL} = 0.4mA

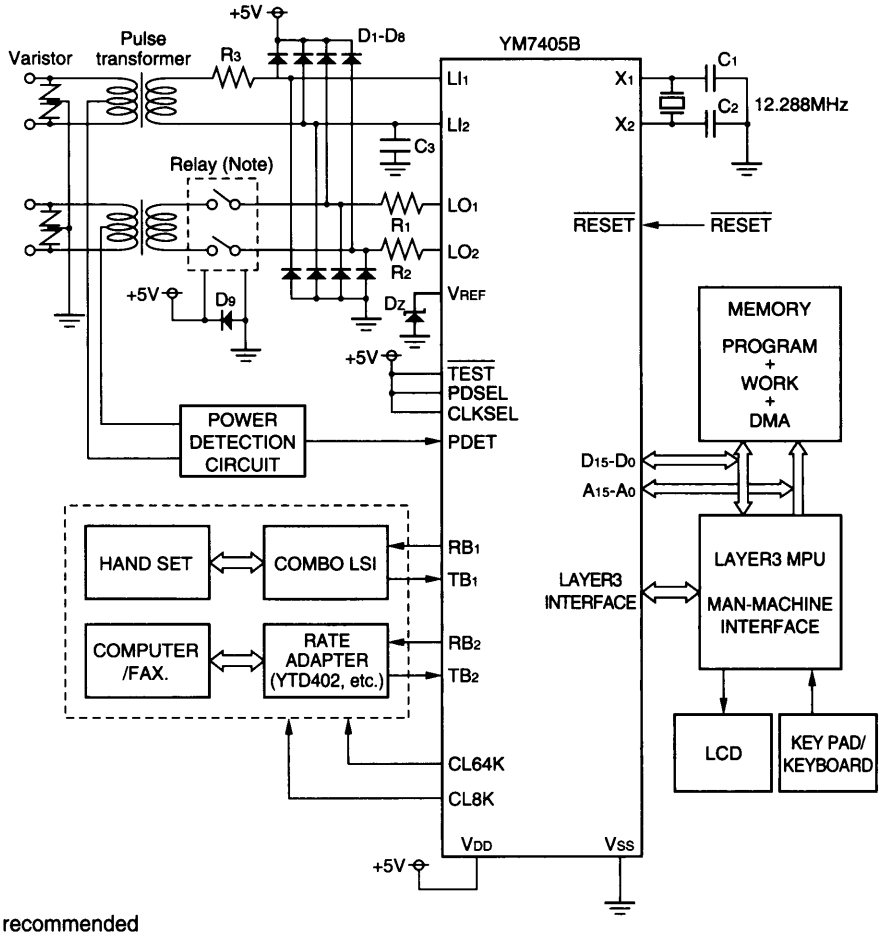
Note 5: $\overline{INT}$ pin Test Conditions : I_{OL} = 1.2mA
RBHW pin Test Conditions : R_L = 500Ω, I_{OL} = 0.8mA

Note 6: With respect to cases where D0-D15, A0-A15 and $\overline{UBE}$ pins are in the input state and where $\overline{MWR}$ and $\overline{MRD}$ pins are in Hi-Z state.

Note 7: Test in active state.

■ EXAMPLE APPLICATION CIRCUITS

The YM7405B can be used for digital telephones, group 4 facsimiles, multimedia communications systems, etc. The YM7405B contains all the Layer 1, Layer 2, and driver/receiver functions for ISDN terminal equipments. A digital telephone can be easily built by simply adding a Layer 3, man-machine interface control section, send/receive pulse transformers. Figure 1 is an example of circuits for the composite terminal equipment. Figure 2 shows an example of interface bus connection to the microprocessor.



Recommended parts

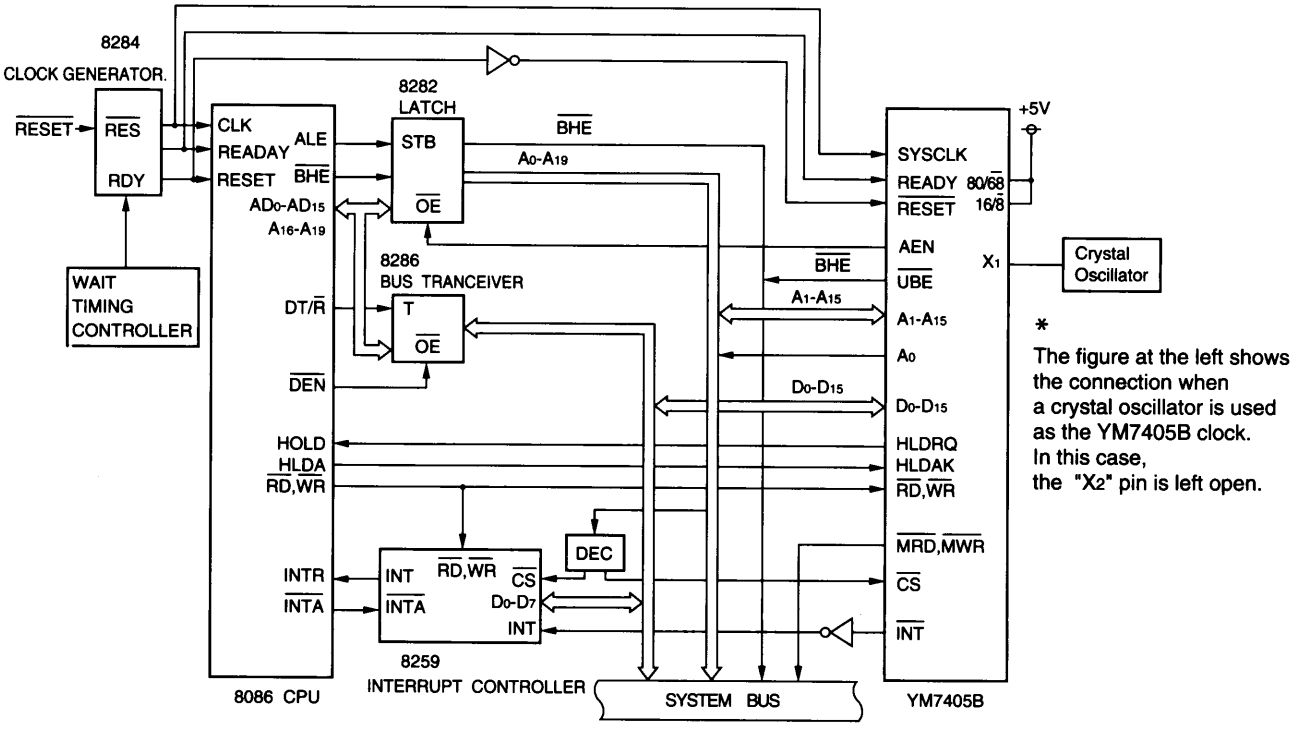
- Pulse transformer
  Tokin
  JPC
  TDK
  Nagano JRC
  Pulse Engineering, etc.
- Zener diode (Dz)
  Hitachi HZ4BLL

Please contact Yamaha for detailed information.

$C_1 = C_2 = 15\text{-}30pF$
$C_3 = 0.1\mu F$
$R_1 = R_2 = 39\Omega$
$R_3 = 8.2k\Omega$

Note: The use of a relay is recommended when the TE transmitter output impedance can not be achieved as described in ITU-T Recommendation I.430. The use of common mode filter choke is recommended when LCL can not be achieved as described in ITU-T Recommendation I.430.

Figure 1 Application to composite terminal equipment



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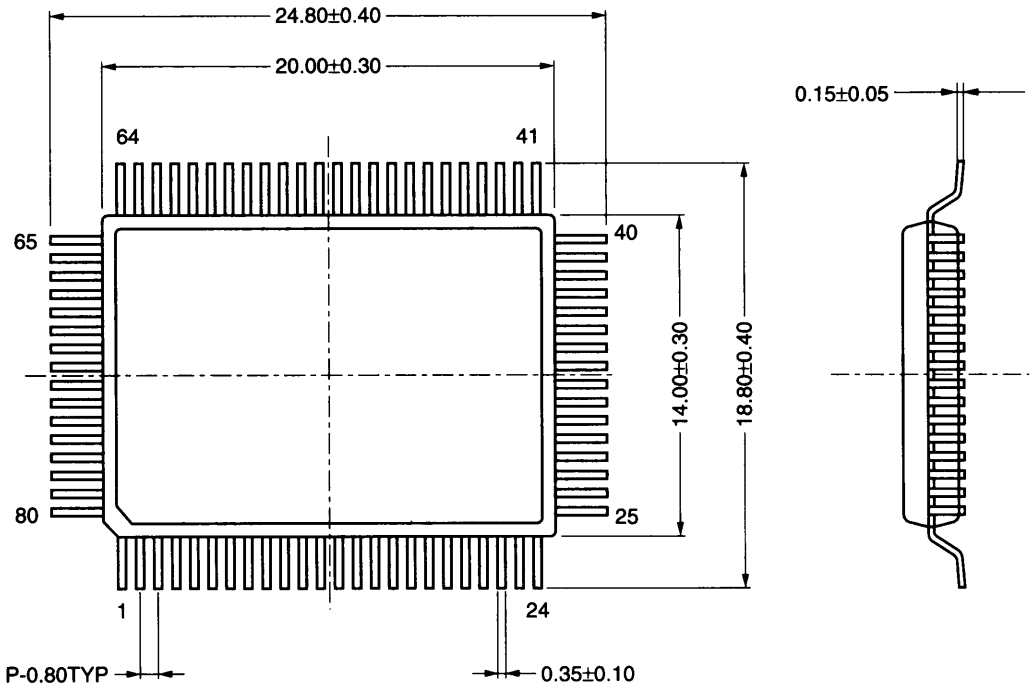
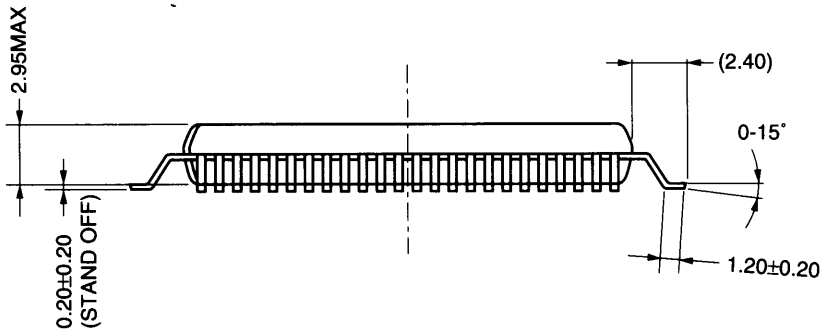
The figure at the left shows the connection when a crystal oscillator is used as the YM7405B clock. In this case, the "X2" pin is left open.

Figure 2 Example of 8086 family Layer 3 connection

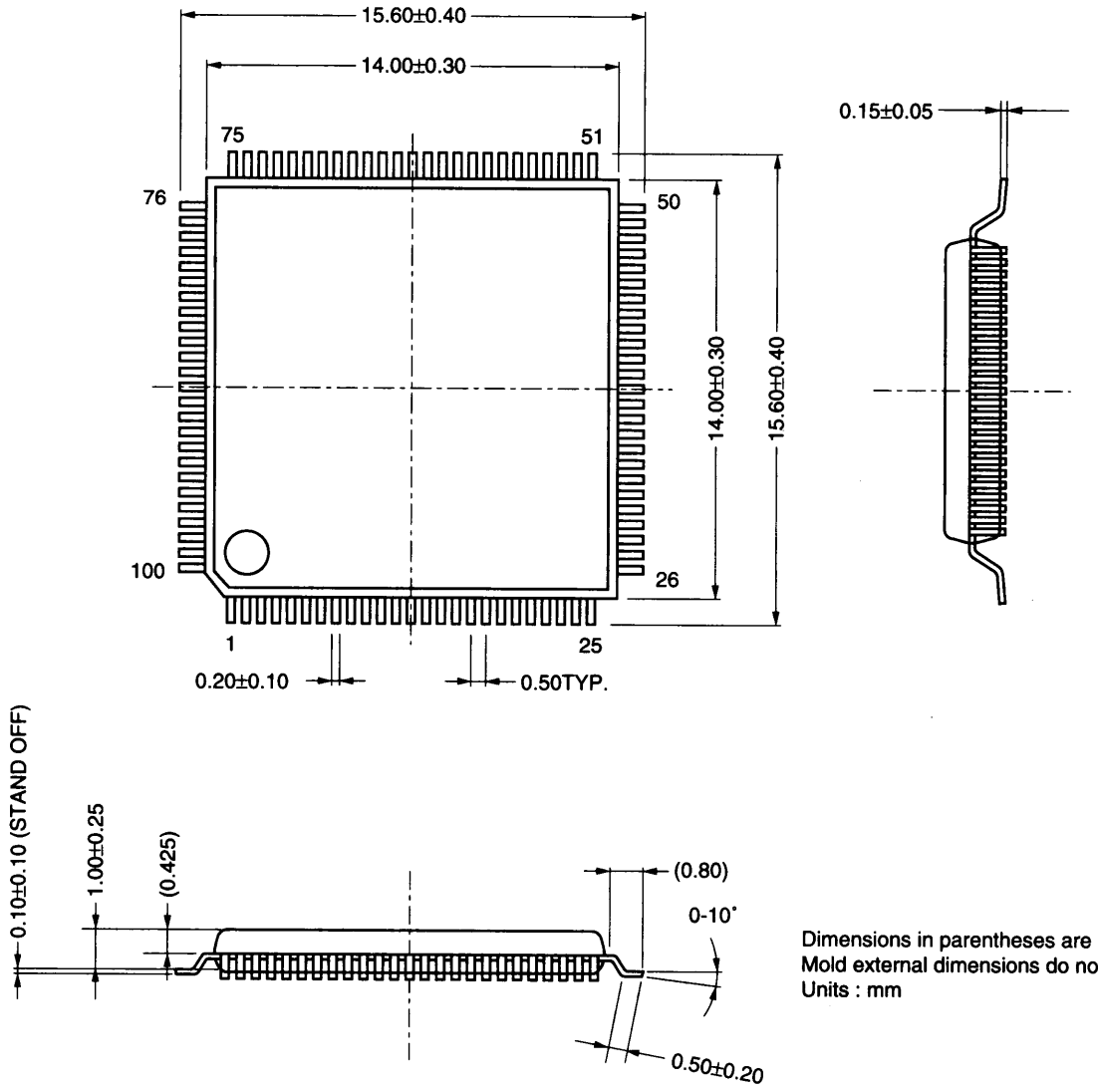
80-pin QFP





Dimensions in parentheses are reference values.
Mold external dimensions do not include burrs.
Units : mm

100-pin TQFP



Dimensions in parentheses are reference values.
Mold external dimensions do not include burrs.
Units : mm

Note: The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of Yamaha.

Figure 3 External dimensions

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