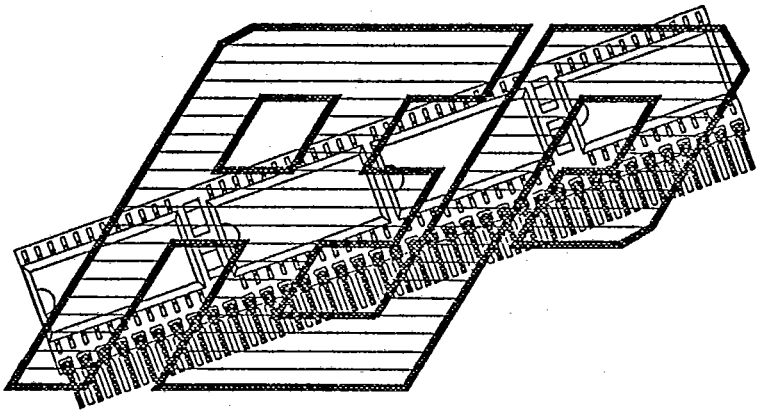
T-46-07-27

- >> *32-bit bus interface latches, non-inverting or inverting.*
- >> *High density .070 center spaced ZIP leads for maximum I/O in minimum area.*
- >> *Space saving vertical mounting orientation.*
- >> *Convenient "in one side, out the other" broadside pin-out.*
- >> *TTL compatible*
- >> *Uses single +5V power supply*



32 LINE LATCH MODULE

DESCRIPTION:

The AEPLZ32 is a high speed,high density 32-line latch module ideal for use with 16 or 32-bit wide address/data paths or buses. It combines the advantages of the 845 (non-inverting) or 846 (inverting) type parallel latch ICs with very large data widths and a board-space saving configuration. The vertical mounting orientation and compact I/O pin footprint make it superb for projects with tight space constraints.

Physically the module consists of an FR4 PC material substrate mounted with four 845 or 846 type latch ICs, four 0.10 microfarad decoupling capacitors, and 75 I/O pins in a staggered ZIP package format. It can be ordered with any 845 or 846 type parallel latches made by any manufacturer producing them in a 24 pin SOP package. The module features two Preset pins and two Output Enable pins controlling two sets of sixteen outputs. Overall Output Enable, Master Reset, and Latch Enable pins are also used.

Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors' data sheets, like those attached, or from their data books.

Mechanical dimensions are 0.505 inch high by 2.66 inches long by 0.22 inch wide. The I/O pins are in two rows which are 0.1 inch apart and offset longitudinally 0.035 inch. In each row the pins are on 0.070 inch center spacing. See included specification drawing.

The AEPLZ32 is one of a family of digital circuit support function modules which includes a 32 line buffer, a 32 line transceiver, and a 32 line register module. These are natural companions for AEP memory modules.

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EXAMPLE PART NUMBERING CHART

LZ32 with non-inverting	
74F845 latches	AEPLZ32-F845
74FCT845A latches	AEPLZ32-FCT845A
74LS845 latches	AEPLZ32-LS845
LZ32 with inverting	
74F846 latches	AEPLZ32-F846
74FCT846A latches	AEPLZ32-FCT846
74LS846 latches	AEPLZ32-LS846

Latches notes:
The standard latch ICs used are the 74FCT845A or 74PCT845A. Please contact AEP if a type is desired that is not listed above. If the pin out configuration is the same as the 74F845 or 74F846 and the desired type is available in a standard 24 pin SOP, there should be no problem using it on the module.

The "A" at the end of the standard IC number is a "High Performance" speed indicator. AEP may use the "A" version of a device even if it is not explicitly specified unless requested not to. An exact specification (type and manufacturer) of the IC device desired is recommended. Please contact AEP for assistance if needed.

Vendor notes:
The IC device specification information included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this might affect module price.

Substrate Label note:
The finished Latch Module may have "AEPRZ32" printed on the back of the PC material substrate. This is a substrate designation label only. Similar modules occasionally share the same substrate. The function, pin-out, and part number of a module is determined by the ICs used.

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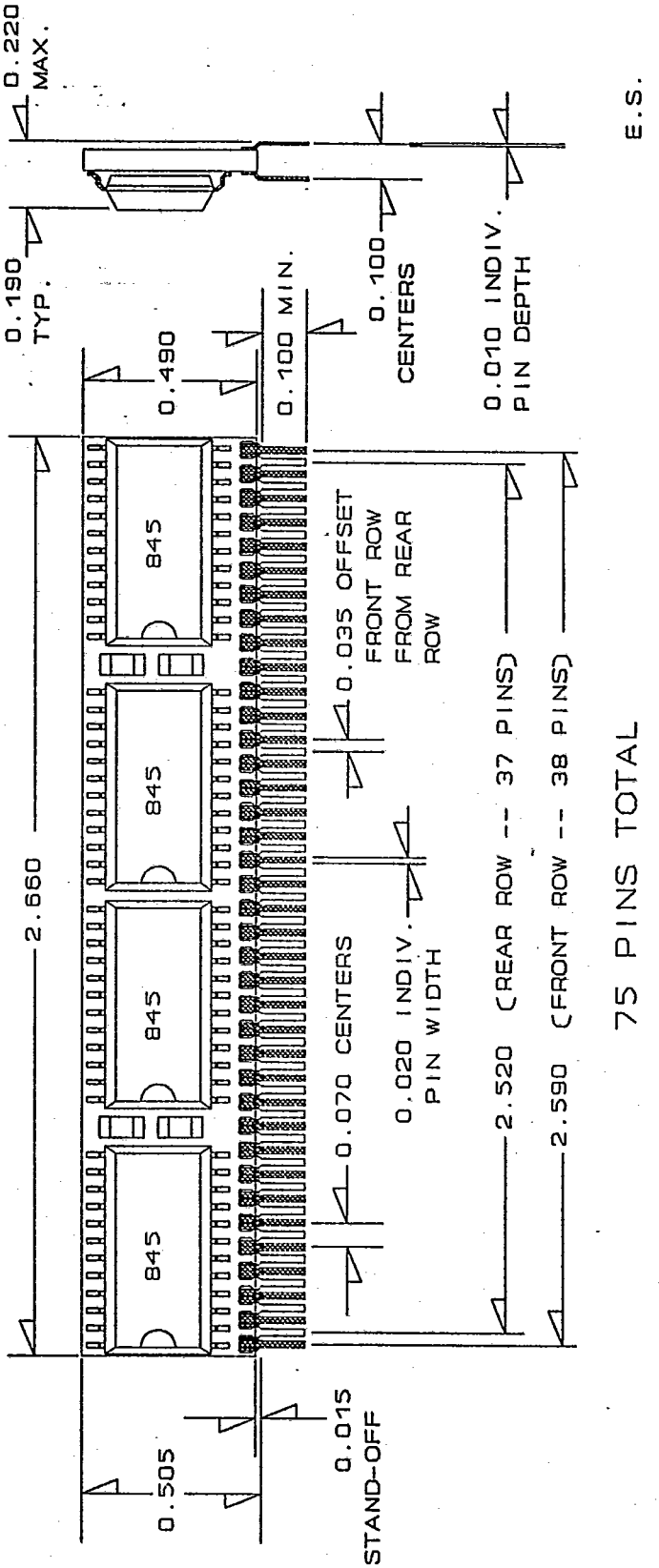
AEPLZ32-845
32 LINE LATCH MODULE

DIMENSIONS IN INCHES, TOLERANCE: +/- 0.010 UNLESS SPECIFIED



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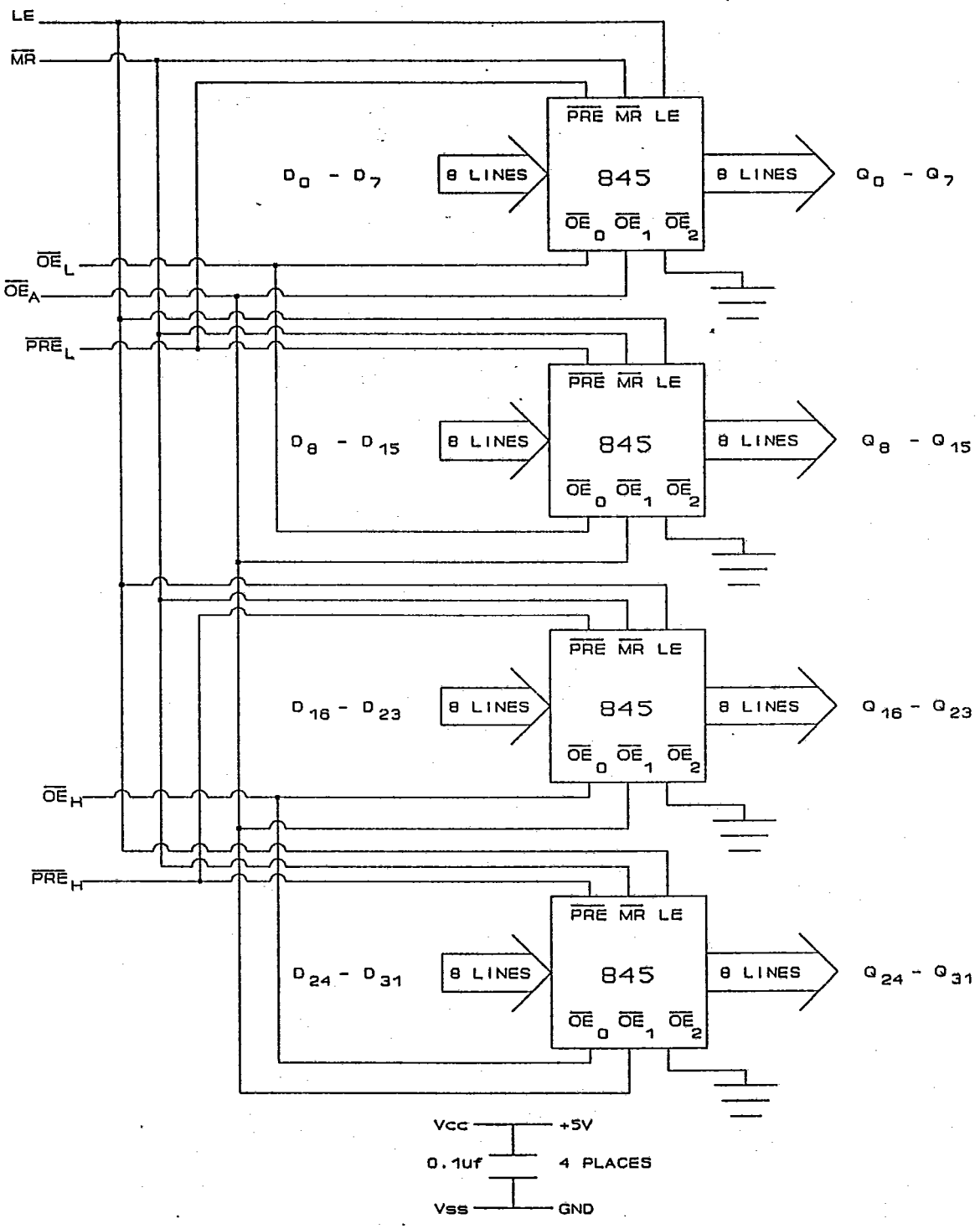
32 LINE LATCH MODULE FUNCTIONAL DIAGRAM



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32 LINE LATCH MODULE
PIN CONFIGURATION (TOP VIEW)

	PIN #s		
(DATA INPUTS)	D_0 – 1	2 – Q_0	(DATA OUTPUTS)
	D_1 – 3	4 – Q_1	
	D_2 – 5	6 – Q_2	
	D_3 – 7	8 – Q_3	
	D_4 – 9	10 – Q_4	
	D_5 – 11	12 – Q_5	
	D_6 – 13	14 – Q_6	
	D_7 – 15	16 – Q_7	
($PRESET_{LOW}$*)	PRE_L – 17	18 – OE_A	($OUTPUT\ ENABLE_{ALL}$*)
($OUTPUT\ ENABLE_{LOW}$*)	OE_L – 19	20 – GND	(GROUND)
	D_8 – 21	22 – Q_8	
	D_9 – 23	24 – Q_9	
	D_{10} – 25	26 – Q_{10}	
	D_{11} – 27	28 – Q_{11}	
	D_{12} – 29	30 – Q_{12}	
	D_{13} – 31	32 – Q_{13}	
	D_{14} – 33	34 – Q_{14}	
	D_{15} – 35	36 – Q_{15}	
(POWER)	Vcc – 37	38 – Vcc	(POWER)
	D_{16} – 39	40 – Q_{16}	
	D_{17} – 41	42 – Q_{17}	
	D_{18} – 43	44 – Q_{18}	
	D_{19} – 45	46 – Q_{19}	
	D_{20} – 47	48 – Q_{20}	
	D_{21} – 49	50 – Q_{21}	
	D_{22} – 51	52 – Q_{22}	
	D_{23} – 53	54 – Q_{23}	
(GROUND)	GND – 55	56 – MR	(MEMORY RESET*)
($OUTPUT\ ENABLE_{HIGH}$*)	OE_H – 57	58 – PRE_H	($PRESET_{HIGH}$*)
	D_{24} – 59	60 – Q_{24}	
	D_{25} – 61	62 – Q_{25}	
	D_{26} – 63	64 – Q_{26}	
	D_{27} – 65	66 – Q_{27}	
	D_{28} – 67	68 – Q_{28}	
	D_{29} – 69	70 – Q_{29}	
	D_{30} – 71	72 – Q_{30}	
	D_{31} – 73	74 – Q_{31}	
(LATCH ENABLE)	LE – 75		

*ACTIVE LOW

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