CMD

Microcircuits

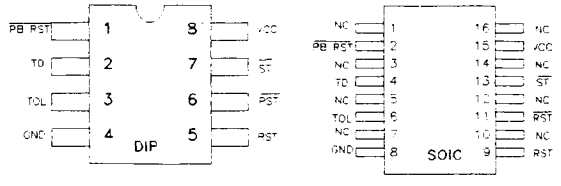
CM1232

CMOS MICROPROCESSOR MONITOR CIRCUIT

Features

- Precision Voltage Monitor -
  - 5% or 10% Power Supply selected by TOL pin
- Power On or Out of Tolerance Reset
- Watchdog Timer - 150ms, 600ms, or 1.2 sec
- Pushbutton monitoring for external override
- Low Power CMOS
- Space saving 8-pin DIP

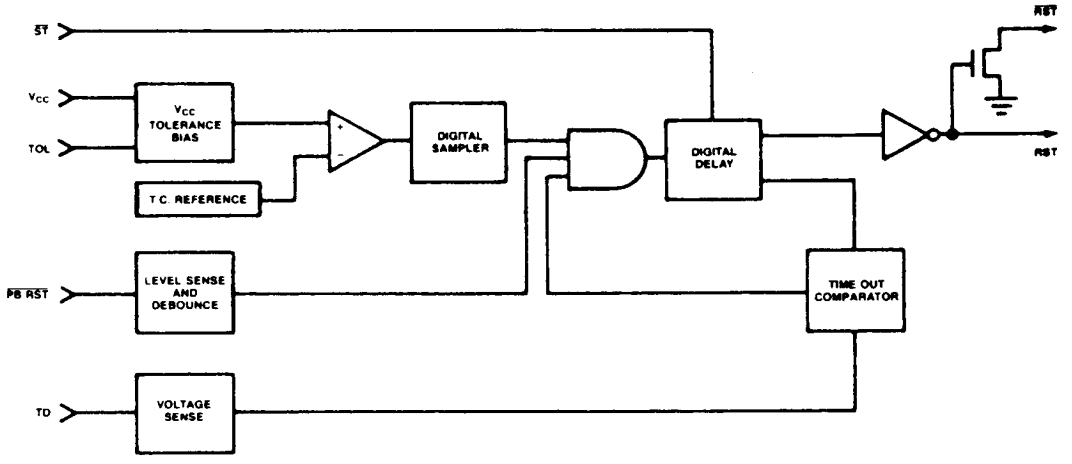
Package Options



General Description

CMD Microcircuits Microprocessor Monitor features precision circuitry for simplified monitoring of microprocessor systems: power supply monitoring, software execution checking, and external override. A temperature compensated reference circuit monitors power (VCC) and forces Reset active whenever an out of tolerance condition occurs. Reset is held active for 250ms after VCC returns to an in tolerance condition. Software execution is monitored by the watchdog timer which will produce an active Reset unless the strobe input is driven low prior to timeout. An external override is accomplished by the Push Button Reset Input which debounces the input and creates an active Reset for a minimum of 250ms. The combination of CMD Microcircuits' Advanced CMOS and reduced system component count produces a more accurate and reliable system than is possible with discreet components.

Micromonitor Block Diagram



PRELIMINARY PRODUCT INFORMATION

Absolute Maximum Ratings:

Ratings	Symbol	Value
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input Voltage (All Inputs)	V_{IN}	-0.3V to V_{CC}+0.3V
DC Current per Pin	I_{IN}	-10mA to +10mA
Operating Temperature	T_A	0°C to 70°C
Storage Temperature	T_S	-65°C to + 150°C
Junction Temperature	T_J	-150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Note: Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Notes
$\overline{ST}$ and $\overline{PB\ RST}$ Input, High Level	V_{IH}	2.0		V_{CC}+.3	V	1
$\overline{ST}$ and $\overline{PB\ RST}$ Input, Low Level	V_{IL}	-0.3		+0.8	V	1
TD Input, High Level	V_{IH}	V_{CC}		V_{CC}+.3	V	1,4
TD Input, Low Level	V_{Il}	-0.3		V_{SS}	V	1,4
Input Leakage	I_{IL}	-1.0		+1.0	μA	3,4
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA	5
Output Current @ .4V	I_{OL}	3.2	6.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1
Input Capacitance (T_A = 25°C)	C_{IN}			5.0	pF	
Output Capacitance (T_A = 25°C)	C_{OUT}			7.0	pF	

PRELIMINARY PRODUCT INFORMATION

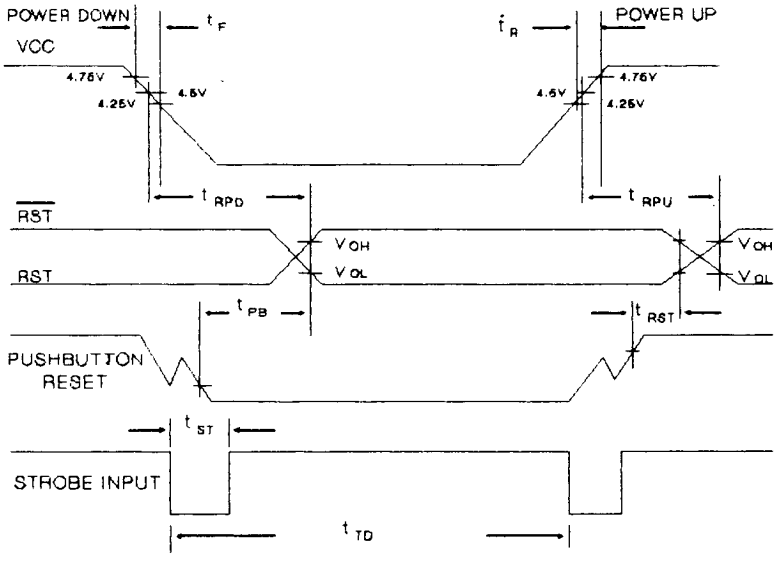
AC Electrical Characteristics: (0°C to 70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units	Notes
$\overline{\text{PB RST}}$ V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{\text{ST}}$ Pulse Width	t_{ST}	20			ns	
V_{CC} Detect to RST and $\overline{\text{RST}}$	t_{RPD}			100	ns	
V_{CC} Slew Rate 4.75V - 4.25V	t_F	300			μs	
V_{CC} Detect to RST and $\overline{\text{RST}}$	t_{RPU}	250	610	1000	ms	6
V_{CC} Slew Rate 4.25V - 4.75V	t_R	0			ns	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open, $\overline{\text{ST}}$ at V_{SS} or V_{CC}, and $\overline{\text{PB RST}}$ and TD floating.
3. $\overline{\text{PB RST}}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. TD is internally pulled to $0.4V_{CC}$ through an internal impedance of 125KΩ, and will switch watchdog timer to mid time out period when input pin is left floating.
5. $\overline{\text{RST}}$ is an open drain output.
6. t_R = 5μs

Timing Diagrams



NOTE:
t_{TD} is the maximum elapsed time between $\overline{\text{ST}}$ pulses which will keep the watchdog timer from forcing RST and $\overline{\text{RST}}$ to the active state for a time of t_{TRST}. t_{TD} times are given as maximum. The minimum time is 25% of the maximum.

t_{TD} = 250ms max. with TD pin at Ground
t_{TD} = 1 second max. with TD pin floating
t_{TD} = 2 seconds max. with TD pin at V_{CC}

FUNCTIONAL DESCRIPTION

Power Monitor

The C1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level (defined by TOL), the internal V_{CC} comparator activates RST (Pin 5) and $\overline{RST}$ (Pin 6). With TOL connected to ground, these reset signals become active as V_{CC} falls below 4.75V. With TOL connected to V_{CC}, the reset signals become active as V_{CC} falls below 4.5V. RST and $\overline{RST}$ make excellent control signals for a microprocessor since processing can be stopped at the last possible moment of valid V_{CC}. On power up the two reset signals are kept active for a minimum of 250ms to allow the power supply and processor to stabilize.

Pushbutton Reset

The C1232 provides an active low input pin for direct connection to a pushbutton (Figure 1). Internally this input is debounced and activates the RST and $\overline{RST}$ signals for a minimum of 250ms. The 250ms delay starts as the Pushbutton Reset pin is released from the low level.

Watchdog Timer

The C1232 provides a watchdog timer function by forcing RST and $\overline{RST}$ signals active whenever the $\overline{ST}$ input does not transition for a predetermined time period. The time period is determined by the TD input: 150ms with TD connected to ground; 600ms with TD left unconnected; and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out as soon as RST and $\overline{RST}$ go inactive. If a high to low transition occurs on the ST input prior to time out, the watchdog timer is reset and begins its timeout period again. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ signals are driven to the active state for a minimum of 250ms. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, or control signals. When the microprocessor is functioning normally, these signals would be generated by the microprocessor from a software routine, keeping the watchdog timer from timing out as long as the microprocessor routine was functioning properly. An example is shown in Figure 2.

Pushbutton Reset

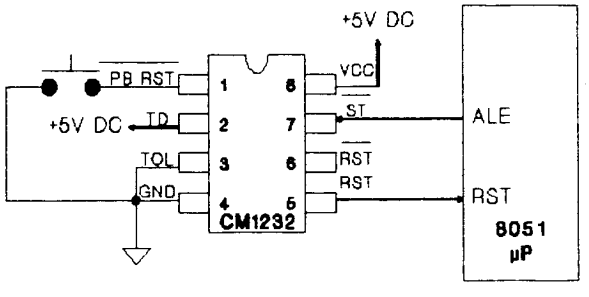


Figure 1

Watchdog Timer

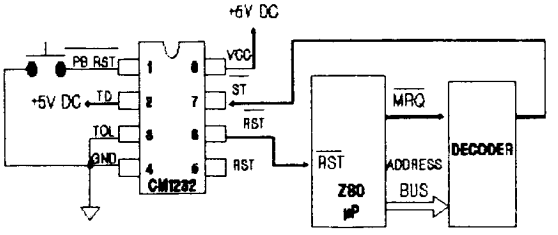


Figure 2

018414 V _ R