CYBUS3384
CYBUS3L384

Dual 5-Bit Bus Switch

Features

- **Zero propagation delay**
- **2Ω switches connect inputs to outputs**
- **Direct bus connection when switches are ON**
- **High (>500 Meg Ω) resistance when switch is OFF**
- **Performs bidirectional translator function between 3.3V and 5.0V power supplies**
- **CMOS for low power dissipation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Inputs and outputs interface with 5.0V CMOS, TTL, or 3.3V CMOS**
- **ESD > 2000V**
- **Power-off disable**

CYBUS3L384

- **Low power version**

Functional Description

The CYBUS3384 and CYBUS3L384 are ten-bit, two-port bidirectional bus switches that allow one bus to be connected directly to, or isolated from, another without introducing additional propagation delay or ground noise. The input and output voltage levels allow direct interface with TTL and CMOS devices. Two bus enable signals, $\overline{BE}_1$ and $\overline{BE}_2$, turn on the upper and lower five bits, respectively.

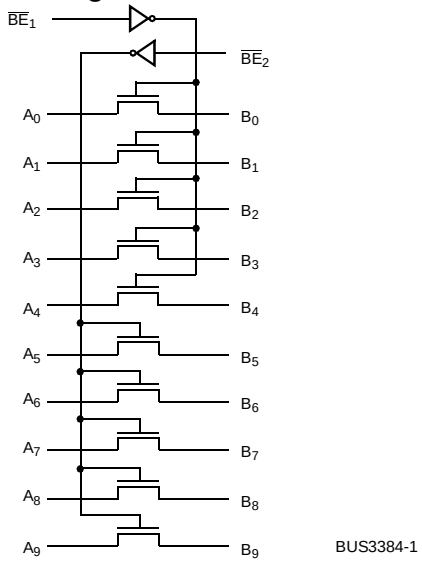
Designed with a low resistance of 2Ω, the CYBUS3384 and CYBUS3L384 are ideal for use in VME or other high DC drive applications.

The power-off disable feature enables modules and cards to be either inserted or withdrawn from operating equipment without shutting down power. Additionally, they facilitate bidirectional interfacing between 3.3V and 5V systems by placing a single diode in series with the 5V V_{CC} line and a resistor from pin 24 to ground.

The CYBUS3384 and CYBUS3L384 are also suitable for small signal analog application where crosstalk and off isolation performance of –66 dB at 50 MHz is required.

The CYBUS3L384 is a low-power version of the CYBUS3384 with a typical I_{CC} of 0.2 μA.

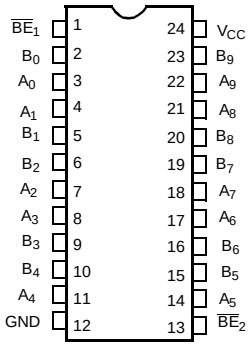
Logic Block Diagram



BUS3384-1

Pin Configurations

DIP/SOIC/QSOP
Top View



BUS3384-2

Pin Description

Name	Description
A	Bus A, Inputs or Outputs
B	Bus B, Inputs or Outputs
$\overline{BE}_1$, $\overline{BE}_2$	Bus Switch Enable

Function Table[1]

Inputs				
$\overline{BE}_1$	$\overline{BE}_2$	$B_{0–4}$	$B_{5–9}$	Function
H	H	High-Z	High-Z	Non-connect
L	H	$A_{0–4}$	High-Z	Connect
H	L	High-Z	$A_{5–9}$	Connect
L	L	$A_{0–4}$	$A_{5–9}$	Connect

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +165°C

Ambient Temperature with Power Applied..... –65°C to +135°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin)..... 120 mA

Power Dissipation..... 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

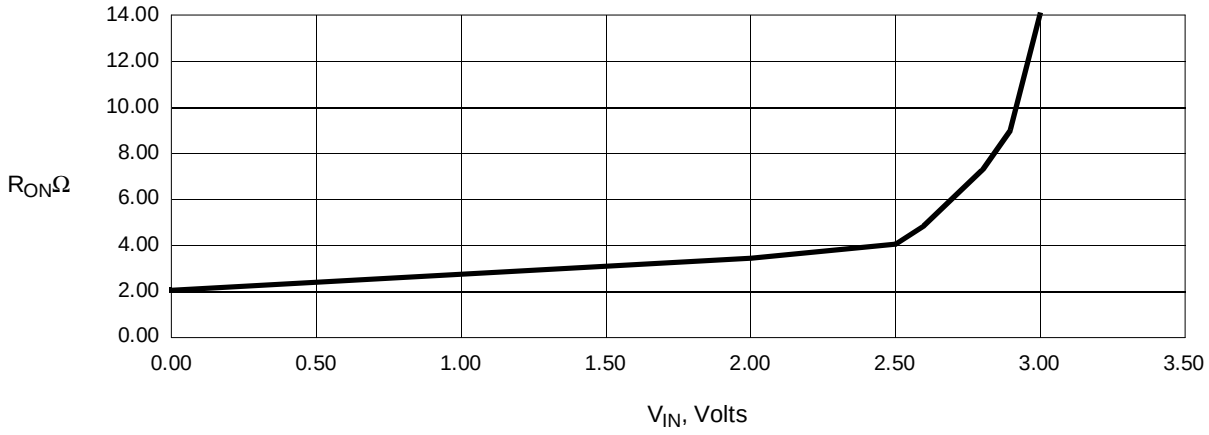
Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	–40°C to +85°C	4.0V to 5.5V
Military	–55°C to +125°C	4.0V to 5.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage	Control Inputs Only	2.0			V
V_{IL}	Input LOW Voltage	Control Inputs Only			0.8	V
V_H	Hysteresis[5]	Control Inputs Only		0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
R_{ON}	Switch On Resistance[6]	V_{CC}=4.75V, V_{IN}=0.0V, I_{ON}=30 mA		2	4	W
		V_{CC}=4.75V, V_{IN}=2.4V, I_{ON}=15 mA		4	8	W
I_{IN}	Input Leakage Current	V_{CC}=Max., V_{IN}=V_{CC}			±1	µA
I_{OZ}	Off State Current (High-Z)	V_{CC}=Max., V_{OUT}=0.5V		0.001	±1	µA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V, V_{IN}=V_{CC}			±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		100		mA

On Resistance vs. V_{IN} @ 4.75 V_{CC}



Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is guaranteed but not tested.
6. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on pin A or pin B.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	3	4	pF
C_{OUT}	Output Capacitance	7	8	pF

Power Supply Characteristics

Parameter	Description	Test Conditions[8]		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., V_{IN}≤GND or V_{CC}, f=0	3384	0.2	3.0	µA
			3L384	0.2	3.0	µA
ΔI_{CC}	Quiescent Power Supply Current (Input HIGH)[9]	V_{CC}=Max., V_{IN}=3.4V, f=0, Per Control Input			2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., Control Input Toggling, @ 50% Duty Cycle, A & B Pins Open			0.12	mA/ MHz
I_C	Total Power Supply Current[11, 12]	V_{CC}=Max., Two Control Inputs Toggling, @ 50% Duty Cycle, f_1=10 MHz, V_{IN}=3.4V	3384		4.4	mA
			3L384		4.4	mA

Switching Characteristics Over the Operating Range[13]

Parameter	Description	Military		Commercial		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B[14, 15]		0.25		.25	ns
t_{PZH} t_{PZL}	Switch Turn On Delay, $\overline{BE}_1$, $\overline{BE}_2$ to A, B[13]	1.5	7.5	1.5	6.5	ns
t_{PHZ} t_{PHZ}	Switch Turn Off Delay, $\overline{BE}_1$, $\overline{BE}_2$ to A, B[13, 14]	1.5	6.5	1.5	5.5	ns
$\|Q_{ci}\|$	Charge Injection, Typical[16, 17]		1.5		1.5	pC

Notes:

8. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
9. Per TTL driven input (V_{IN}=3.4V); A and B pins do not contribute to I_{CC}. All other inputs at V_{CC} or GND.
10. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
12. Note that activity on A or B inputs do not contribute to I_C. The switches merely connect and pass through activity on these pins.
13. See Test Circuit and Waveform. Minimum limits are guaranteed but not tested.
14. This parameter is guaranteed by design but not tested.
15. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
16. Measured at switch turn off, A to C, load=50 pF in parallel with 10 meg scope probe, V_{IN} at A=0.0V.
17. Tested initially and after any design change which may affect this parameter.

Ordering Information CYBUS3384

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
0.25	CYBUS3384PC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CYBUS3384QC	Q13	24-Lead (150-Mil) QSOP	
	CYBUS3384SOC	S13	24-Lead (300-Mil) Molded SOIC	
0.25	CYBUS3384DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CYBUS3384LMB	L64	28-Square Leadless Chip Carrier	

Ordering Information CYBUS3L384

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
0.25	CYBUS3L384PC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CYBUS3L384QC	Q13	24-Lead (150-Mil) QSOP	
	CYBUS3L384SOC	S13	24-Lead (300-Mil) Molded SOIC	

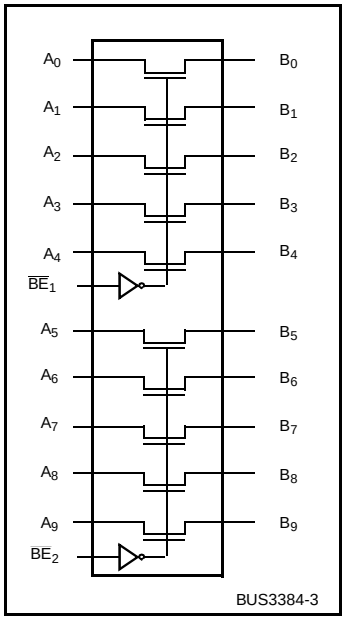


Figure 1. CYBUS3384

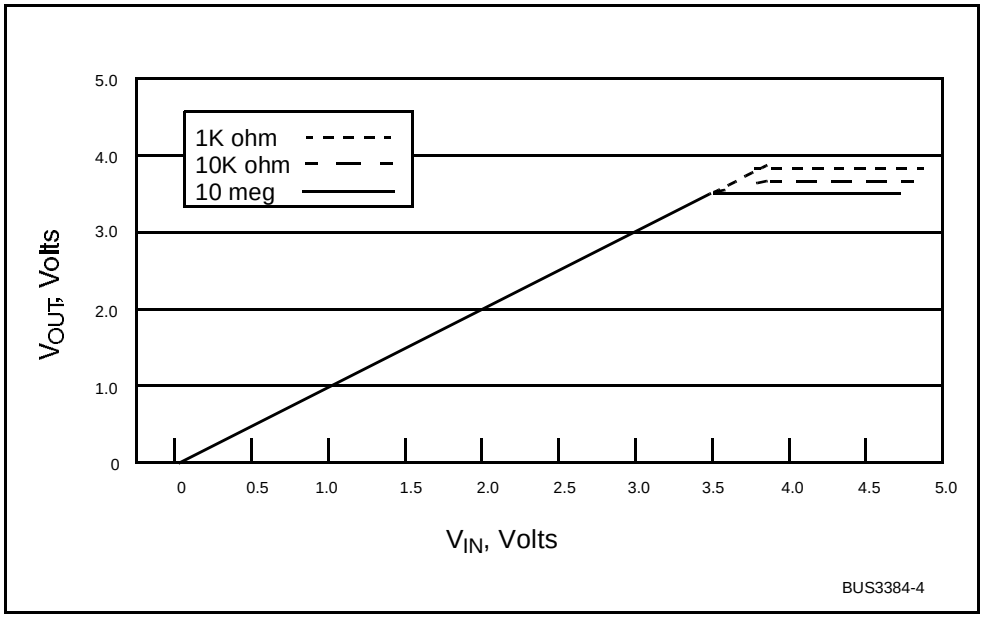


Figure 2. V_{OUT} vs. Volts

Application Information

The CYBUS3384 is a ten-channel bidirectional solid state bus switch with a “near zero” propagation delay.

The CYBUS3384 is organized into two groups of five N-Channel MOSFETs. Each group has an independent control input for output enable (see *Figure 1*). Because the N-channel MOSFET is physically symmetric, the device pin can act as an input or an output.

The two enable input ($\overline{BE}_1$ and $\overline{BE}_2$) sense TTL level signals and drive the gates of the N-channel MOSFETs to VCC. With the gate at V_{CC}, the output voltage will follow the input voltage up to V_{CC} minus the threshold voltage. At this point the N-channel MOSFET begins to turn off, rapidly increasing the effective resistance (R_{ON}) such that further increases to input voltage no longer increase the output voltage (see *Figure 2*).

When either the input or output of the CYBUS3384 is near zero volts and the gate is at V_{CC}, the device is fully on, (low resistance) and available to pass large currents in either direction. In this condition, the CYBUS3384 inputs are directly connected to the outputs.

The CYBUS3384 provides no signal drive itself. As a result the rise and fall times of the CYBUS3384 outputs are determined by the device driving the CYBUS3384 inputs rather than the CYBUS3384 itself.

The propagation delay contributed by the CYBUS3384 is essentially zero when the N-channel gate is at V_{CC}.

When the device is unpowered, the CYBUS3384 draws no current from the I/O or control inputs, and there is no current

path from the I/O or control to the power pins. There are no back power or current drain problems when the device is unpowered.

The CYBUS3384 provides an ideal interface between 5V and 3.3V components, since the CYBUS3384 provides no signal drive, the I_{CC} demands are small, limited to AC switching of the N-channel gates, control circuitry, and a minute amount of I/O leakage. Due to the low current demands of the CYBUS3384, it is possible to lower the CYBUS3384 VCC from a standard 5.0V supply with a small, inexpensive diode and a resistor to provide a low-current full-bidirectional signal compatibility between 5V logic family signals and 3.3V logic family signals.

By adding a small, inexpensive diode and a resistor, the CYBUS3384 V_{CC} supply voltage can be shifted to 4.3V as shown in *Figure 3*. 5V signals will then be limited to 3.3V as they pass through the CYBUS3384. 3.3V signals will pass back through the CYBUS3384 unaltered and provide compatibility with 5V TTL input requirements. Note that the conversion is bidirectional and is limited to 3.3V independent of which side is driven to 5V. The CYBUS3384 could convert 5V signals for use on a 3.3V bus of convert a 5V bus to signals compatible with 3.3V components.

3.3V/5V Supply Operation

In certain system applications, the CYBUS3384 must operate from either a 5V or 3.3V power supply, depending on the state of the system. If this occurs, the circuit shown in *Figure 4* can be added to step the 3.3V supply up to a nominal 5V level. The low-cost, high-efficiency Step Up regulator shown in the figure is available for Linear Technology, Maxim, and other suppliers. The diode arrangement will automatically select the active supply. Standard silicon diodes can be used because the CYBUS3384 V_{CC} is specified at 4.0V.

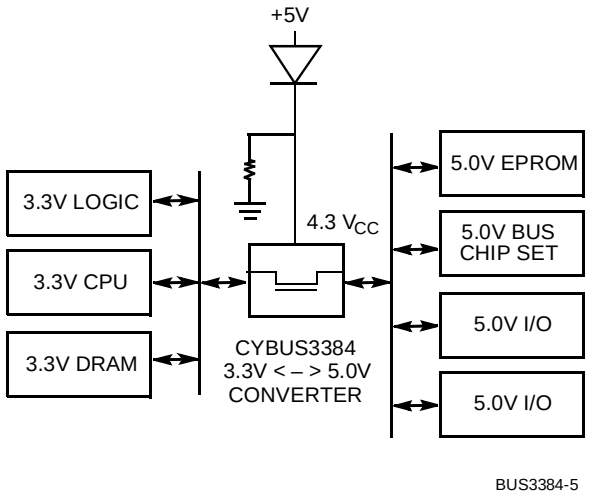


Figure 3. System with CYBUS3384 as 5V TTL to 3V Converter

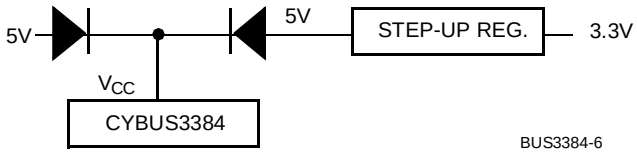


Figure 4. 3.3V/5V Supply Switch

Low Power Bus Isolation

Modern battery-operated systems rely on internal power management schemes to disconnect power from subsystems not in use. Usually the subsystem bus input ESD protection circuits consist of a pair of clamp diodes to limit input voltage excursions to a maximum of V_{CC}+Vt and –Vt (see *Figure 5*). Removing power from these causes the VCC ESD clamp diode to connect the dead circuit inputs to GND, often significantly increasing bus loading and power dissipation (see *Figure 6*). The CYBUS3384 placed on the input of the load to be disconnected effectively prevents bus loading and its associated problems.

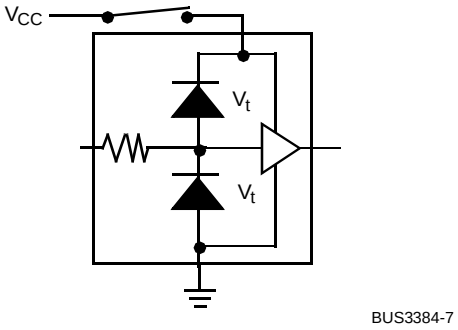


Figure 5. Gate Input (Power ON)

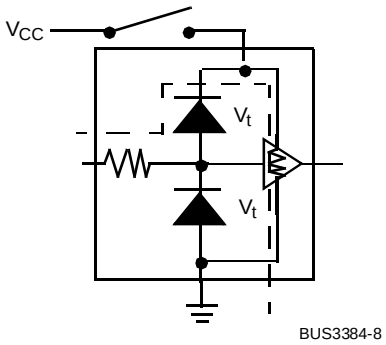


Figure 6. Gate Input (Power OFF)

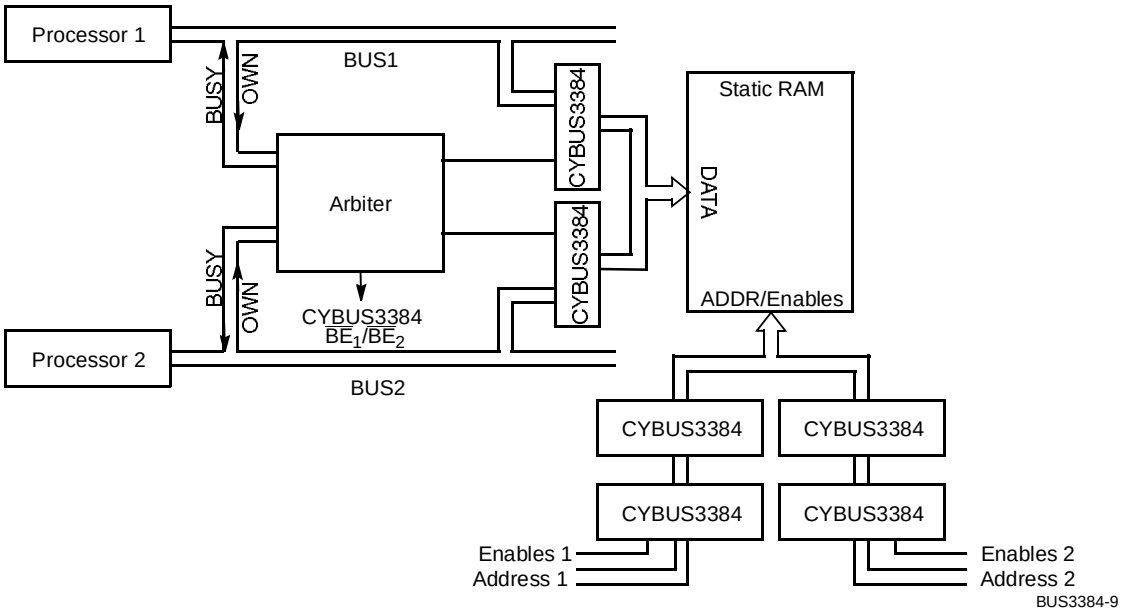


Figure 7. High Speed Dual Port RAM

High Speed Dual Port RAM

As shown in *Figure 7*, a high-speed, dual-port memory is implemented using a combination of commodity SRAM, a simple arbitration circuit, and the CYBUS3384. Processor 1 is the system host processor while Processor 2 is dedicated peripheral processor (such as a DSP for acquisitioning and manipulating data). Either processor can own the SRAM by first reading the BUSY bit to determine if the SRAM is available. If so, the requesting processor takes control by writing the OWN bit (which redirects the bus through the CYBUS3384s and sets the BUSY bit notifying the other bus the SRAM is not available). Processor 1 owns the bus and may now access the SRAM as needed. When finished, Processor 1 resets the OWN bit releasing the SRAM. The SRAM access sequence is identical for Processor 2. In this application, the CYBUS3384 saves 10 ns compared to using an F244 address buffer and an F245 data bus transceiver. This, in turn, allows the use of a slower, more available SRAM, resulting in lower system cost and power savings.

Selectable Termination Loads

In some applications, it is desirable to vary the characteristic termination impedance as the system configuration changes. This is a common problem in automatic test equipment applications. Because of their low ON resistance, miniature relays are often used to switch termination loads. A single CYBUS3384 can replace as many as 10 such relays resulting in faster switching operation, lower power, and significant cost savings.

Fast Latch

Figures 8 and *9* show variations of a latch having a sub 1-ns propagational delay time using the CYBUS3384 in combination with other components. This circuit has the advantage of being four to ten times faster than an equivalent implementation using a 373 latch—and with no added noise. *Figure 8* relies on the stray capacitance of the bus to maintain data when the CYBUS3384 opens. Assuming 50-pF stray capacitance at room temperature and a 1 microampere input leakage current, a 1 volt “droop” from the initial voltage level would take 50 microseconds. *Figure 9* shows the addition of a physical capacitor if there is insufficient stray capacitance. *Figure 10* shows an active bus termination capable of sustaining the programmed logic for an indefinite period of time in the presence of V_{CC}.

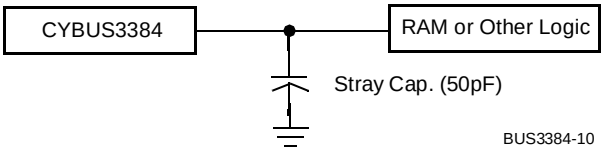


Figure 8. Latch Variation with Spray Capacitance

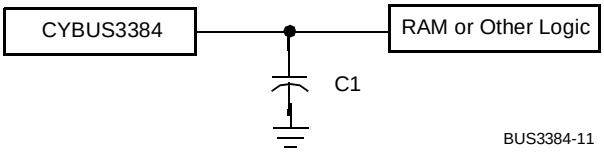


Figure 9. Latch Variation with Physical Capacitor

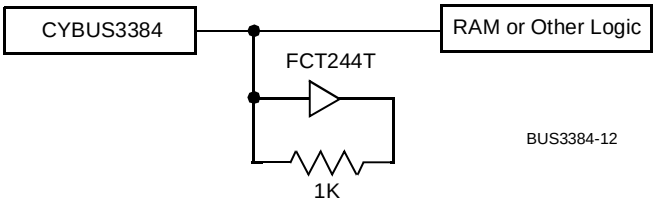


Figure 10. Active Bus Termination

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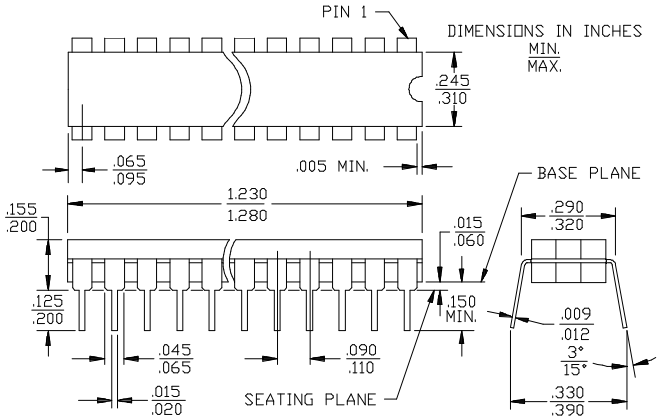
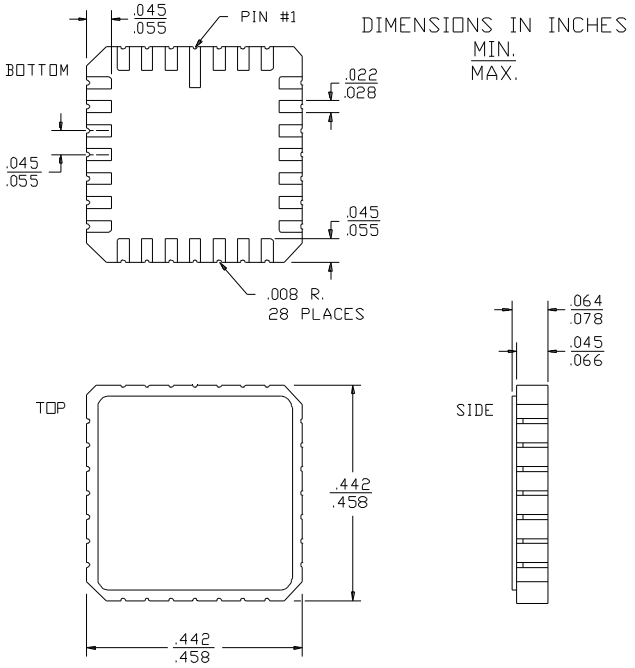
Package Diagrams

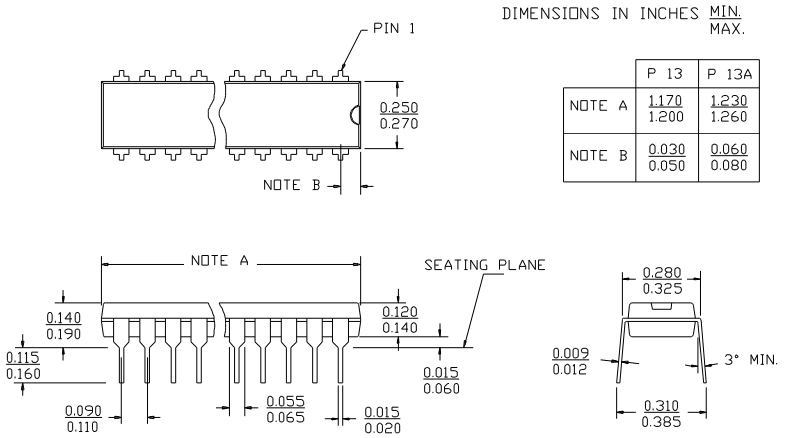
24-Lead (300-Mil) CerDIP D14
MIL–STD–1835 D–9 Config.A



28-Square Leadless Chip Carrier L64
MIL–STD–1835 C–4



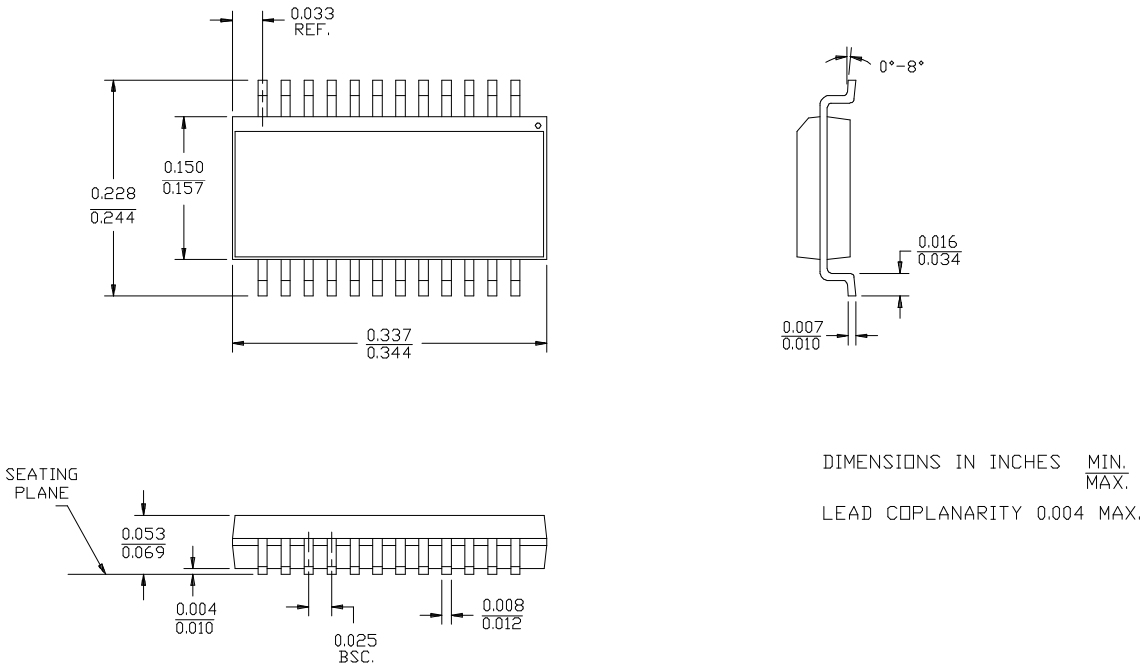
24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 / 1.200	1.230 / 1.260
NOTE B	0.030 / 0.050	0.060 / 0.080

Package Diagrams (Continued)

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13