373

T-46-07-11

National Semiconductor

DM54ALS373/DM74ALS373 Octal D-Type TRI-STATE® Transparent Latch

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

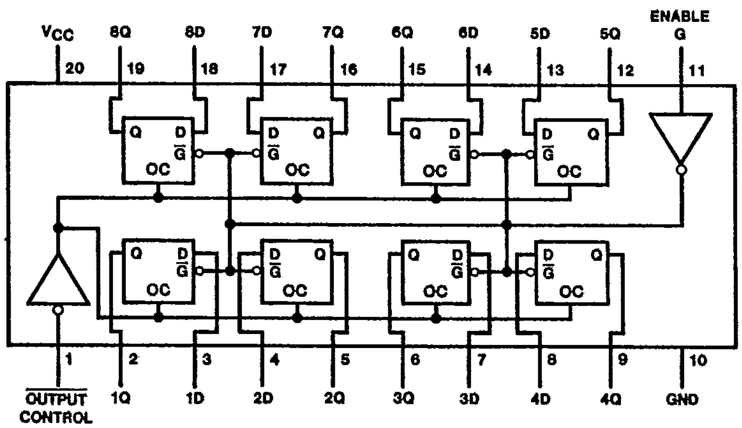
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS373 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6220-1

Order Number DM54ALS373J, DM74ALS373WM, DM74ALS373N or DM74ALS373SJ
See NS Package Number J20A, M20B, M20D or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	57.0°C/W
M Package	76.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS373			DM74ALS373			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
t_W	Width of Enable Pulse, High or Low	10			10			ns
t_{SU}	Data Setup Time	10↓			10↓			ns
t_H	Data Hold Time	7↓			7↓			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V	54ALS I_{OH} = −1 mA	2.4	3.2		V
			74ALS I_{OH} = −2.6 mA	2.4	3.3		V
		V_{CC} = 4.5V to 5.5V I_{OH} = −400 µA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V				20	µA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V				−20	µA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		9	16	mA
			Outputs Low		16	25	mA
			Outputs Disabled		17	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS373		DM74ALS373		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	2	14	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	1	17	4	16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	6	26	6	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	1	23	7	23	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	3	18.5	6	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	20.5	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	13.5	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	18	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

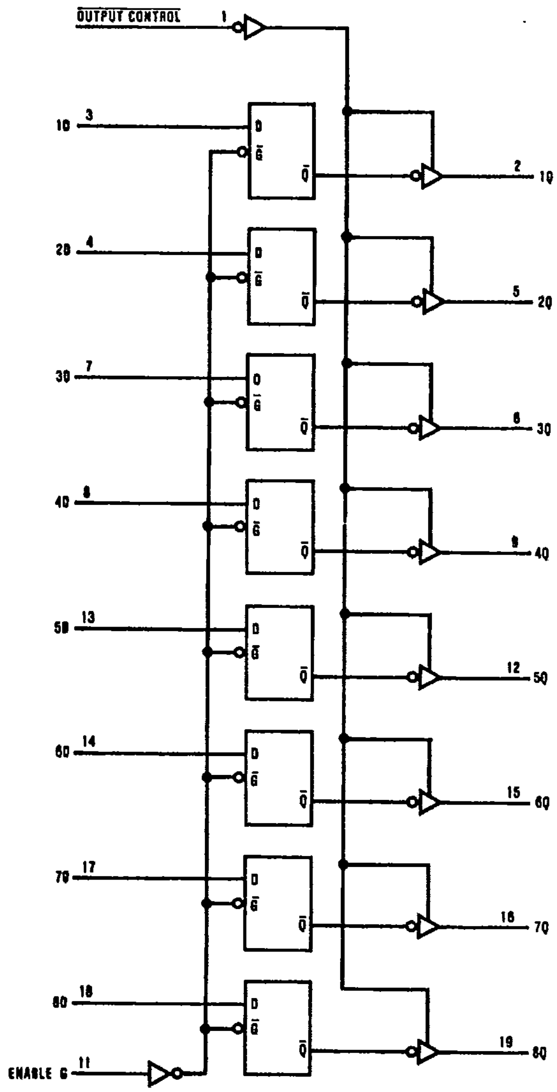
Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram

T-46-07-11



TL/F/6220-2