LXT334 & LXT304A — Low Cost & High Performance Quad E1 Interface Solution

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN070*.

Application Note

Contents

Figures

Tables

1.0 Introduction

This application note shows how to design a CTR12/13 compliant quad port solution using the LXT334 quad E1 transceiver. In order to obtain the jitter attenuation performance required by this specification, the LXT304A is used as a stand-alone jitter attenuator to obtain the transmit timing source.

1.1 ETSI CTR12/13 Requirements

The European Telecommunications Standards Institute (ETSI) drafted two types of standards that define harmonized requirements. The first, for which compliance is voluntary, is the European Telecommunications Standard (ETS). The ETS completely describes all details of the specified interface or equipment. The Technical Basis for Regulation (TBR) requirements are combined with regulatory provisions to form a Common Technical Regulation, or CTR.

In Europe there are two categories of 2.048 Mbps leased line service: unstructured and structured. Unstructured service provides a usable bit rate of 2048 kbps with no network-provided timing or framing support. CTR-12 defines the necessary technical requirements for unstructured service.

Structured service provides a usable bit rate of 1984 kbps with network framing support. CTR-13 defines the technical requirements for structured leased line service.

CTR-12 and CTR-13 include a common Output Jitter section (5.2.1.4). For terminal equipment, this section defines a maximum output jitter of 0.11 UIpp for frequencies from 20 Hz to 100 kHz when measured with a bandpass filter (40 Hz -100 kHz). The input jitter is limited to 1.5 UIpp. The output jitter limit applies to equipment in configurations where output timing is derived locally as well as configurations where output timing is derived from one or more leased lines. These requirements also apply with a data rate offset of up to ±50 ppm from 2.048 MHz.

Not all the equipment designed for the E1 market has to meet CTR12/13. The designer must check with the product specification to determine if such performance is needed.

1.2 Design Considerations

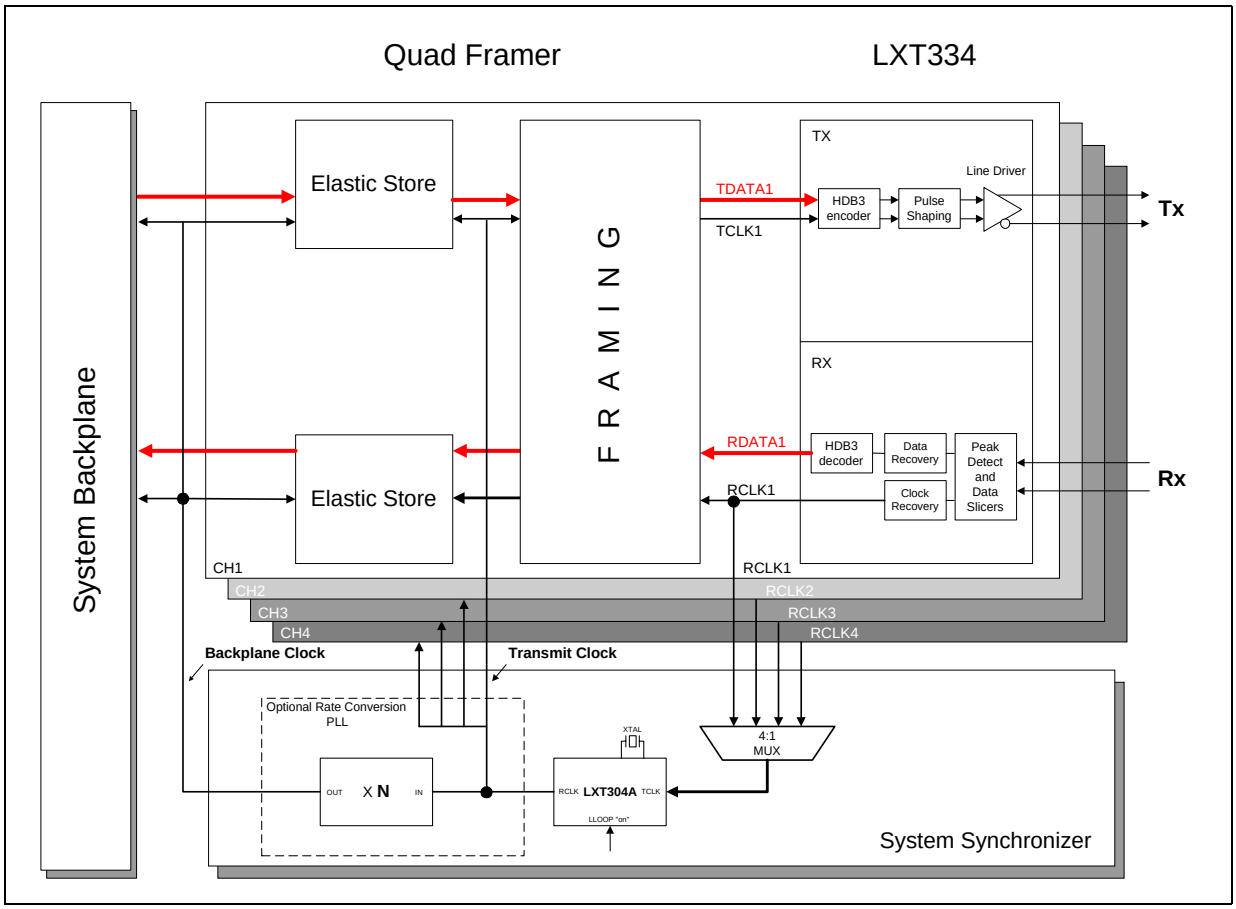
Figure 1 shows a block diagram of a quad port solution using the LXT334 LIU. The LXT334 provides the data and clock recovery functions with optional HDB3 encoding/decoding. On the transmit side, the pulse shaping feature on the LXT334 provides a stable pulse meeting G.703 E1 templates. A high performance transmit driver provides excellent transmit return loss exceeding ETSI 300166 requirements.

The LXT334 will typically interface with a quad E1 framer. Most industry standard framers provide elastic stores for adaptation between backplane timing and receive timing. These are two frame wide fifos capable of performing controlled slips (frame discarding or repetition). They also accommodate some of the low frequency jitter (wander).

An important block in these designs is the *system synchronizer*. Typically, the system synchronizer must be able to extract backplane and transmit timing from an internal source or from one of the tributary inputs. The synchronizer's jitter attenuation performance will determine the amount of jitter in the transmit clock and consequently, the output jitter conveyed to the network. Many designs rely on external VCXO-based PLL circuits added to the transceiver to make the jitter

attenuation performance CTR12/13 compliant. This application note shows how to design a CTR12/13 compliant solution using the LXT334 as the line interface and the LXT304A as a jitter attenuator.

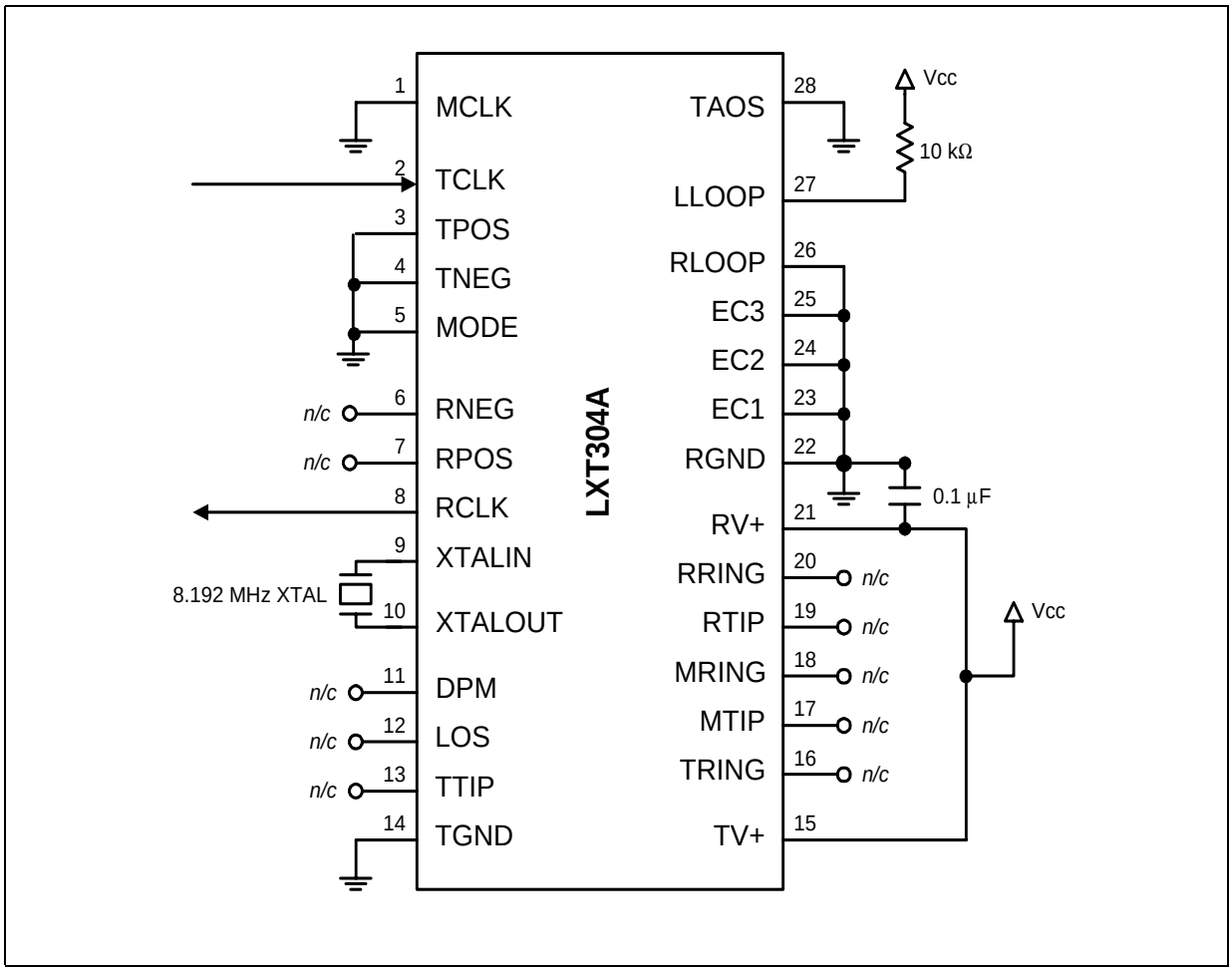
Figure 1. CTR12/13 Compliant Quad Port Solution



A four to one multiplexer allows the synchronizer to choose any one of the tributary recovered clocks as the source for backplane/transmit timing. This clock is then delivered to the LXT304A jitter attenuator. The combined jitter attenuation performance of the LXT334 clock recovery circuit and the LXT304A jitter attenuator provides a good margin for CTR12/13 compliance. In the following section we present experimental results supporting this statement. The 2.048 MHz clock obtained from the LXT304A is used for transmission. An additional frequency multiplier PLL might be necessary in the cases where the backplane clock runs at a different frequency.

When used as a single chip jitter attenuator, the LXT304A provides more than 50% cost savings, as well as board space savings, compared to VCXO based solutions. The LXT304A incorporates an on-chip crystal oscillator, using an external pullable quartz crystal. A specification for the crystal is provided in Table 1. Figure 2 shows the appropriate pin configuration for the LXT304A when used as a stand-alone jitter attenuator for CTR12/13 compliant designs.

Figure 2. LXT304A Configuration as a Stand-alone E1 Jitter Attenuator



1.3 Test Results

Figure 3 represents a test setup used to evaluate the performance of the LXT334 and LXT304A in this kind of application. The pattern generator was set to a 2^{15} - 1 pseudo random pattern. A function generator was used to get a 2.048MHz clock output adjustable within ± 50 ppm. The HP3785A jitter generator adds jitter to this clock. The jittered clock is then applied to the pattern generator's external clock input of. CTR12/13 defines the amount of jitter added to this clock. The jittered line signal is then applied to the LXT334 receiver. The jitter present in the recovered clock and data is attenuated by the LXT304A. The signals are then looped back to the network through the LXT334 transmitter. The HP3785A was used to measure the output jitter in the 40Hz to 100KHz frequency band. Please refer to AN-44 *Jitter Performance Requirements for E1 Leased Lines* for a description of how to setup the HP3785A jitter measurement filters.

Figure 4 shows typical results obtained using this configuration. The results were taken over a ± 50 ppm frequency offset range. Figure 4 demonstrates that the combined jitter attenuation performance of the LXT334 and the LXT304A provides very good margins within CTR12/13 requirements.

Figure 3. CTR12/13 Jitter Performance Evaluation

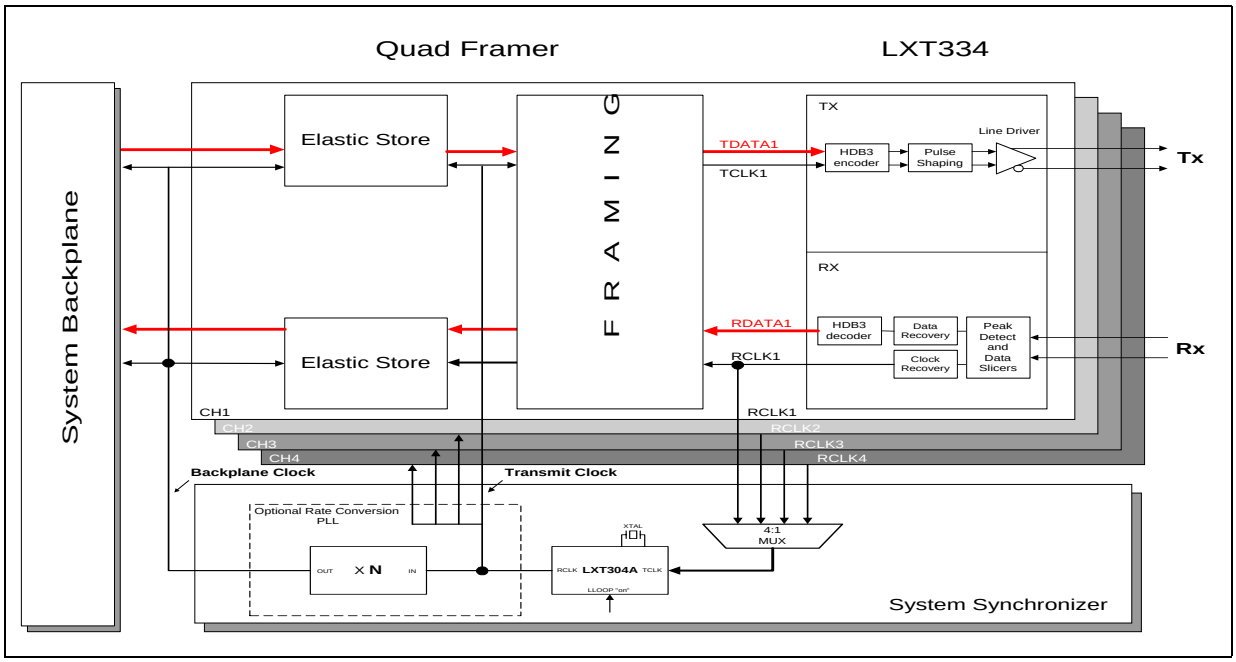


Table 1. LXT304A Crystal Specifications

Parameter	Specification
Frequency	8.192 MHz
Frequency Stability	±20 ppm @ 25 °C ±25 ppm @ -40 to +85 °C (ref 25 °C reading)
Pullability (Pull range may be slightly asymmetrical)	C_L = 19 pF to 37 pF, crystal should pull -95 ppm to -115 ppm from nominal frequency. C_L = 19 pF to 11.6 pF, crystal should pull +95 ppm to +130 ppm from nominal frequency.
Effective series resistance	30 Ω maximum
Crystal cut	AT
Resonance	Parallel
Drive level	2.0 mW maximum
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical
Recommendation: CXT8192 crystal manufactured by CTS Corporation, Tel: (815)786-8411	

Figure 4. Combined Jitter Attenuation Performance (LXT304A and LXT334)