ADVANCE INFORMATION

PI74ALPTX16244

16-Bit Buffer/Driver with 3-State Outputs

Product Features:

- PI74ALPTX family is designed for low voltage operation,
- Supports Live Insertion
- V_{DD} = 1.8V to 3.6V
- 3.6V Tolerant Inputs and Outputs
- Bus Hold
- High Drive, -32/64mA
- Typical V_{OLP} (Output Ground Bounce) < 0.4V at V_{DD} = 2.5V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) < 0.4V at V_{DD}= 2.5V, T_A = 25°C
- Industrial operation at –40°C to +85°C
- Packages available:
  - 48-pin 240 mil wide plastic TSSOP (A48)
  - 48-pin 173 mil wide plastic TVSOP (K48)

Product Description:

Pericom Semiconductor's PI74ALPTX series of logic circuits are produced in the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The buffer/driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

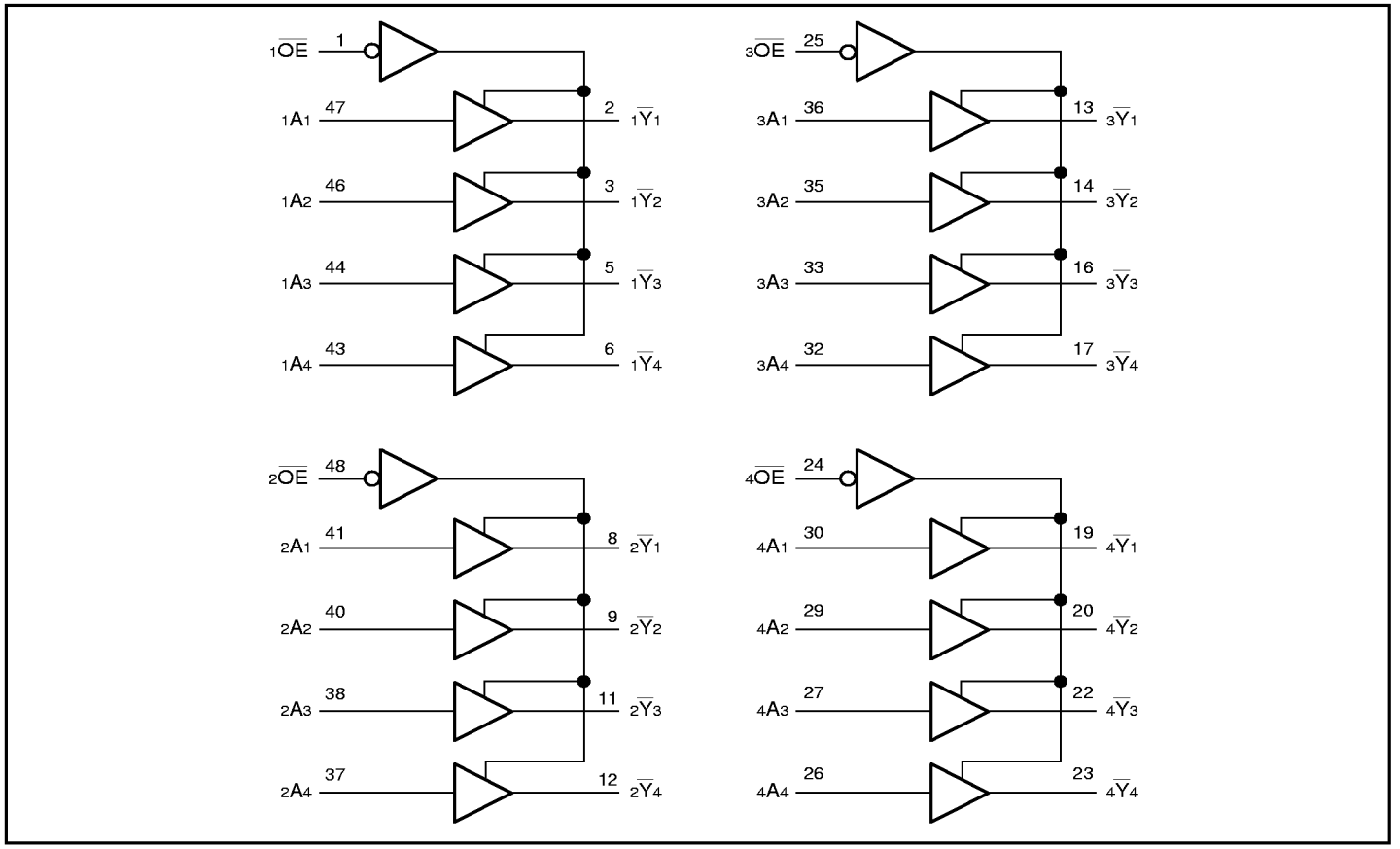
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74ALPTX16244 can be used as a translator, allowing it to operate in mixed 3V/5V systems.

The PI74ALPTX16244 has "Bus Hold," which retains the data input's last state whenever the data input goes to high-impedance, preventing "floating" inputs and eliminating the need for pullup/down resistors.

Logic Block Diagram



Product Pin Description

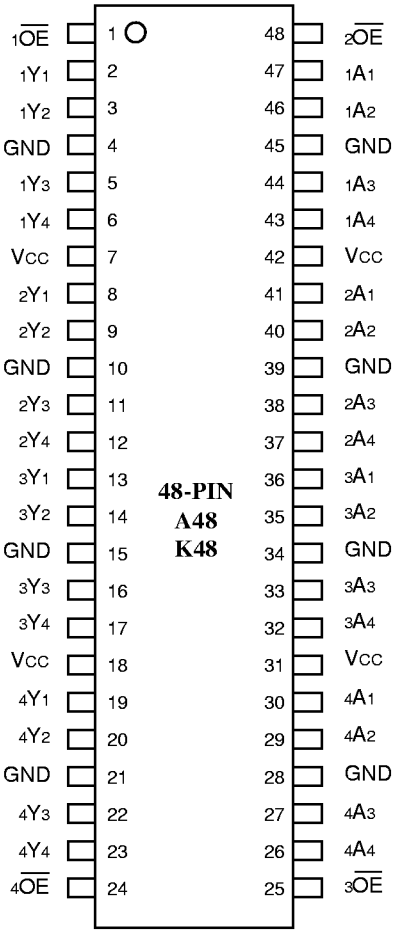
Pin Name	Description
n$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
nAx	Inputs
nYx	3-State Outputs
GND	Ground
VCC	Power

Truth Table[1]

Inputs		Outputs
n$\overline{OE}$	nAx	nYx
L	H	H
L	L	L
H	X	Z

Note:
1. H = High Signal Level
   L = Low Signal Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{DD} ..... –0.5V to 4.6V
Input Voltage Range, V_I ..... -0.5V to 4.6V
Output Voltage Range, V_O (3-Stated) ..... -0.5V to 4.6V
Output Voltage Range, V_O[1] (Active) ..... –0.5V to V_{DD} +0.5V
DC Input Diode Current (I_{IK}) V_I<0V ..... -50mA
DC Output Diode Current (I_{OK})
V_O<0V ..... -50mA
V_O>V_{DD} ..... ±50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... -64/128mA
DC V_{DD} or GND Current per Supply Pin (I_{CC} or GND) ..... ±100mA
Storage Temperature Range, T_{stg} ..... –65°C to150°C

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions[2]

			Min.	Max.	Unit
V_{DD}	Supply voltage	Operating	1.8	3.6	V
		Data Retention Only	1.2	3.6	
V_{IH}	High-level input voltage	V_{DD} = 2.7V to 3.6V	2.0		
V_{IL}	Low-level input voltage	V_{DD} = 2.7V to 3.6V		0.8	
V_I	Input voltage		-0.3	3.6	
V_O	Output voltage	Active State	0	V_{DD}	
		Off State	0	3.6	
	Output current in I_{OH}/I_{OL}	V_{DD} = 3.0V to 3.6V V_{DD} = 3.0V to 3.6V V_{DD} = 2.3V to 2.7V V_{DD} = 1.8V		-32/64 ±24 ±18 ±6	mA
Δt/Δv	Input transistion rise or fall rate[3]		0	10	ns/V
T_A	Operating free-air temperture		-40	85	C

Notes

1. Absolute maximum of I_O must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
3 As measured between 0.8V and 2.0V, V_{DD} = 3.0V.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted)

DC Characteristics 74ALPTX16244 ($2.7V<V_{DD} \leq 3.6V$)

	Parameter	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0			V
V_{IL}	LOW Level Input Voltage					0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 µA		V_{DD} - 0.2			
		I_{OH} = –12 mA	2.7	2.2			
		I_{OH} = –18 mA	3.0	2.4			
		I_{OH} = –24 mA		2.2			
		I_{OH} = –32 mA		2.3			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7 - 3.6			0.2	
		I_{OL} = 12 mA	2.7			0.4	
		I_{OL} = 18 mA	3.0			0.4	
		I_{OL} = 24 mA				0.5	
		I_{OL} = 32 mA				0.5	
		I_{OL} = 64 mA				0.55	
I_I	Input Leakage Current	V_I = 0.0V, V_I = 3.6V	3.6			±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.7 - 3.6			±10	
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0			10	
I_{HOLD}	Bus Hold Current A or B Outputs	V_I = 0.8V	3.0	75			
		V_I = 2.0V		-75			
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ to GND	2.7 - 3.6			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				±20	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD}$ -0.6V, Other inputs at V_{DD} or Gnd				750	

DC Characteristics ALPTX16244 (2.3V ≤ V_{DD} ≤ 2.7V)

	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.6			V
V_{IL}	LOW Level Input Voltage					0.7	
V_{OH}	HIGH Level Output Voltage	I_{OH} = -100 µA		V_{DD} - 0.2			
		I_{OH} = -6 mA	2.3	2.0			
		I_{OH} = -12 mA		1.8			
		I_{OH} = -16 mA		1.7			
		I_{OH} = -24 mA		1.7			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 - 2.7			0.2	
		I_{OL} = 12 mA	2.3			0.4	
		I_{OL} = 18 mA				0.4	
		I_{OL} = 24 mA				0.5	
I_I	Input Leakage Current	V_I = 0.0V, V_I = 2.7V	2.7			±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	2.3 - 2.7			±10	
I_{OFF}	Power-OFF Leakage Current	0 ≤ (V_I,V_O) ≤ 3.6V	0			10	
I_{HOLD} (1)	Bus Hold Current A or B Outputs	V_I = 0.7V	2.5		90		
		V_I = 1.7V			-90		
I_{DD}	Quiescent Supply Current	V_I = V_{DD} or GND	2.3 - 2.7			20	
		V_{DD} ≤ (V_I,V_O) ≤ 3.6V				±20	
ΔI_{DD}	Increase in I_{DD} per input	V_{IH} = V_{DD} -0.6V, Inputs at V_{DD} or Gnd				TBD	

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted) (continued from previous page)

DC Characteristics ALPTX16244 (1.8V ≤ V_{DD} ≤ 2.3V)

	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IH}	HIGH Level Input Voltage		1.8 - 2.3	0.7 x V_{DD}			V
V_{IL}	LOW Level Input Voltage					0.2 x V_{DD}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = -100 µA	1.8	V_{DD} -0.2			
		I_{OH} = -6 mA		1.4			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA				0.2	
		I_{OL} = 6 mA				0.3	
I_I	Input Leakage Current	V_I = 0.0V, V_I = 1.8V				±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}				±10	
I_{OFF}	Power-OFF Leakage Current	0 ≤ (V_I,V_O) ≤ 3.6V	0			10	
I_{HOLD} (1)	Bus Hold Current A or B Outputs	V_I = 0.4	1.8		50		
		V_I = 1.3			-50		
I_{DD}	Quiescent Supply Current	V_I = V_{DD} or GND				20	
		V_{DD} ≤ (V_I,V_O) ≤ 3.6V				±20	
ΔI_{DD}	Increase in I_{DD} per input	V_I = V_{DD} -06V, Other inputs at V_{DD} or Gnd				TBD	

Note: 1. Not guaranteed

AC Electrical Characteristics 74ALPTX16244

Symbol	Parameter	TA = -40°C to +85°C, C_L = 50pF, R_L = 500Ω						Units
		V_{DD} = 3.3V ±0.3V		V_{DD} = 2.5V ±0.2V		V_{DD} = 1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Prop Delay	1.0	2.4	1.0	3.5	1.5	5.7	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	3.8	2.0	5.9	1.5	7.0	
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	4.0	2.0	5.2	1.5	5.0	
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)		0.5		0.5		0.5	

Note

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH or LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics (Target Spec, Eng. Ref Only)

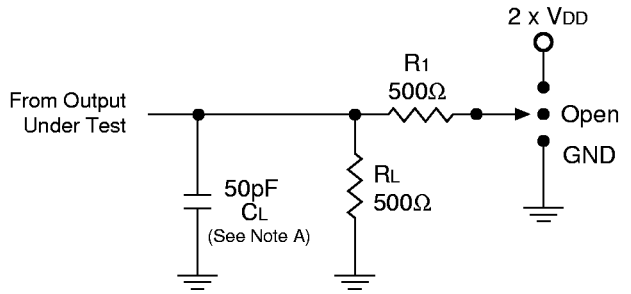
Symbol	Parameter	Conditions	V_{DD}	T_A = +25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50pF, V_{IH} = V_{DD}, V_{IL} = 0V	1.8 2.5 3.3	0.25 0.6 0.8	V
V_{OLP}	Quiet Output Dynamic Valley V_{OL}	C_L = 50pF, V_{IH} = V_{DD}, V_{IL} = 0V	1.8 2.5 3.3	-0.25 -0.6 -0.8	
V_{OLP}	Quiet Output Dynamic Valley V_{OH}	C_L = 50pF, V_{IH} = V_{DD}, V_{IL} = 0V	1.8 2.5 3.3	1.5 1.9 2.2	

Capacitance

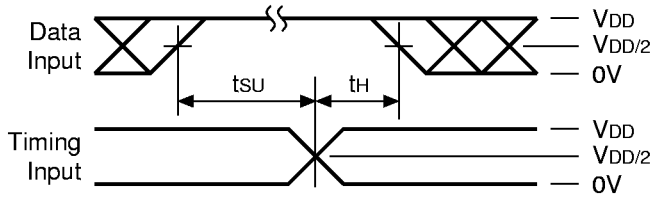
Symbol	Parameter	Conditions	T_A = +25°C Typical	Units
C_{IN}	Input Capacitance	V_{DD} = 1.8, 2.5V or 3.3V, V_I = 0V or V_{DD}	TBD	pF
C_{OUT}	Output Capacitance	V_I = 0V or V_{DD}, V_{DD} = 1.8V, 2.5V or 3.3V	TBD	
C_{PD}	Power Dissipation Capacitance	V_I = 0V or V_{DD}, F = 10 MHz V_{DD} = 1.8V, 2.5V or 3.3V	TBD	

Test Circuits and Switching Waveforms

Parameter Measurement Information (V_{DD} = 1.8V - 3.6V)



Setup, Hold, and Release Timing



Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

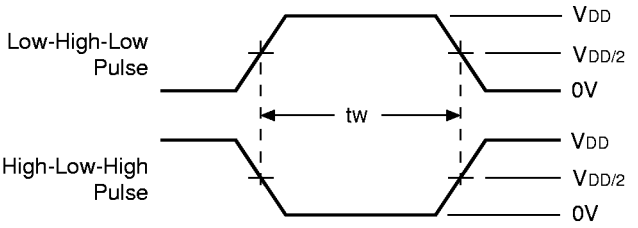
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns, ***measured from 10% to 90%, unless otherwise specified.***

D. The outputs are measured one at a time with one transition per measurement.

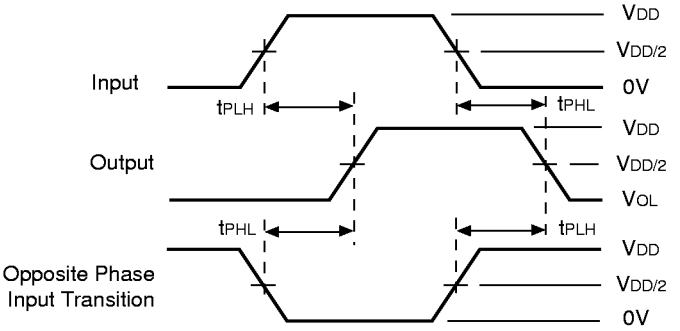
Switch Position

Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x VDD
t_{PHZ}/t_{PZH}	GND

Pulse Width



Propagaton Delay



Enable Disable Timing