

Programmable logic array

(18 × 42 × 10)

PLUS153–10

DESCRIPTION

The PLUS153–10 PLD is a high speed, combinatorial Programmable Logic Array. The Philips Semiconductors state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce maximum propagation delays of 10ns or less.

The 20-pin PLUS153 device has a programmable AND array and a programmable OR array. Unlike PAL® devices, 100% product term sharing is supported. Any of the 32 logic product terms can be connected to any or all of the 10 output OR gates. Most PAL ICs are limited to 7 AND terms per OR function; the PLUS153–10 can support up to 32 input wide OR functions.

The polarity of each output is user-programmable as either Active-High or Active-Low, thus allowing AND-OR or AND-NOR logic implementation. This feature adds an element of design flexibility, particularly when implementing complex decoding functions.

The PLUS153–10 device is user-programmable using one of several commercially available, industry standard PLD programmers.

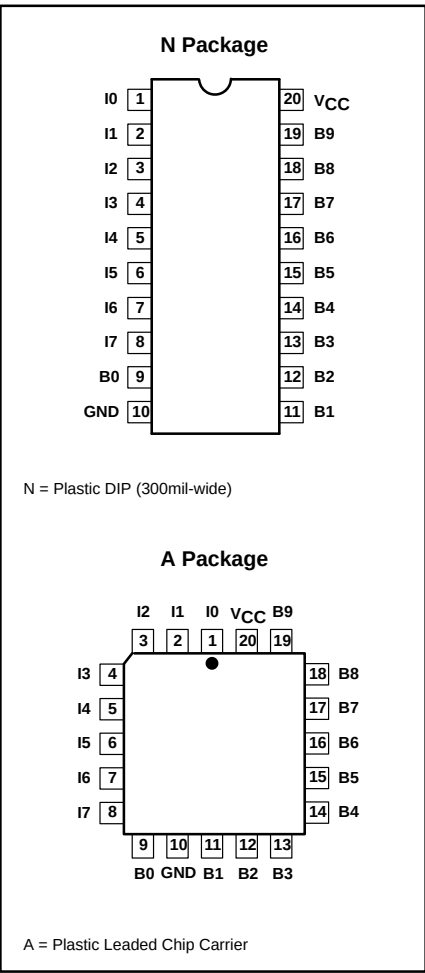
FEATURES

- I/O propagation delays (worst case)
 - PLUS153–10 – 10ns max.
- Functional superset of 16L8 and most other 20-pin combinatorial PAL devices
- Two programmable arrays
 - Supports 32 input wide OR functions
- 8 inputs
- 10 bi-directional I/O
- 42 AND gates
 - 32 logic product terms
 - 10 direction control terms
- Programmable output polarity
 - Active-High or Active-Low
- Security fuse
- 3-State outputs
- Power dissipation: 825mW (typ.)
- TTL Compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

PIN CONFIGURATIONS



ORDERING INFORMATION

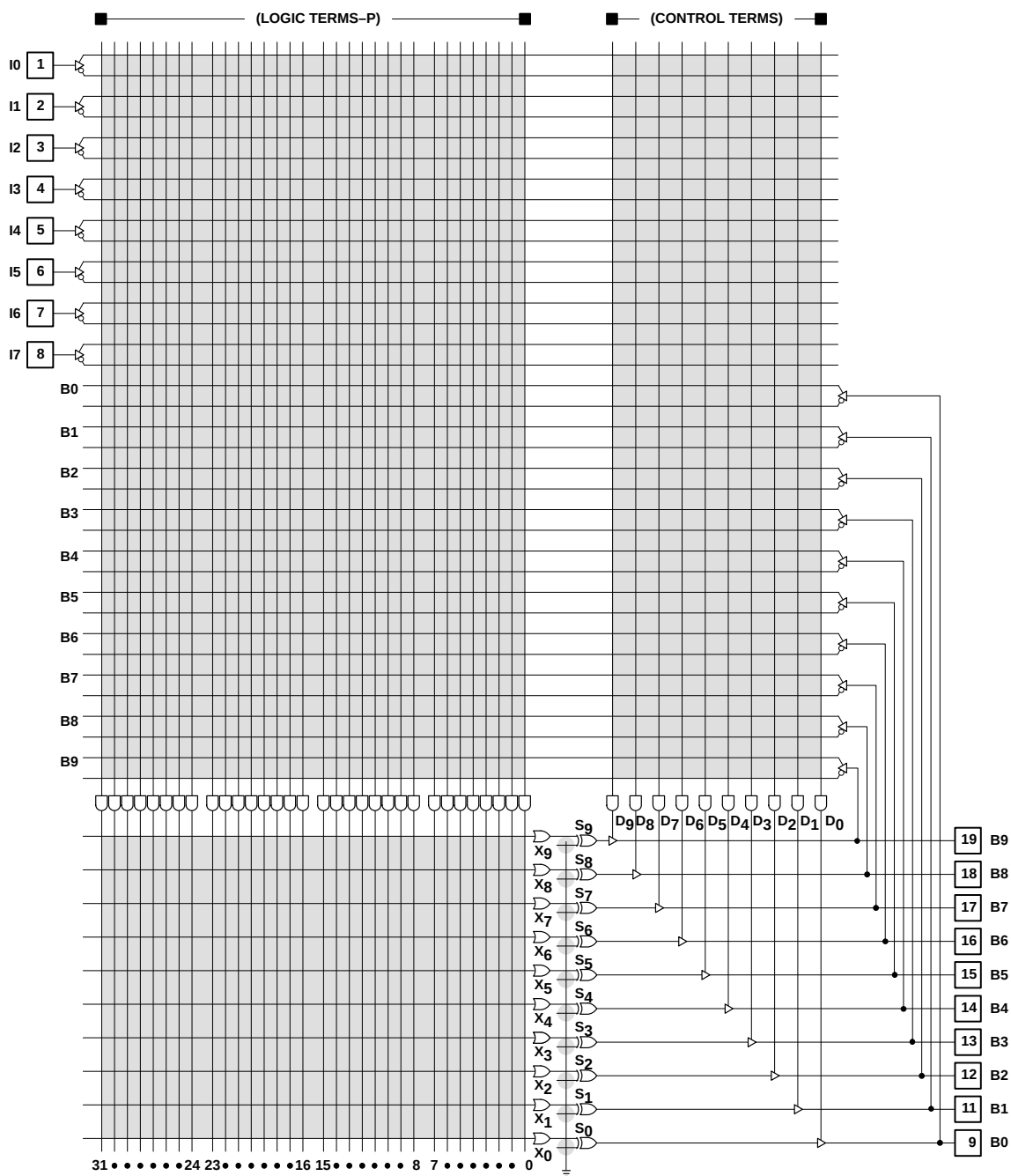
DESCRIPTION	t _{PD} (MAX)	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Dual-In-Line 300mil-wide	10ns	PLUS153–10N	0408D
20-Pin Plastic Leaded Chip Carrier	10ns	PLUS153–10A	0400E

®PAL is a registered trademark of Advanced Micro Devices Corporation.

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LOGIC DIAGRAM



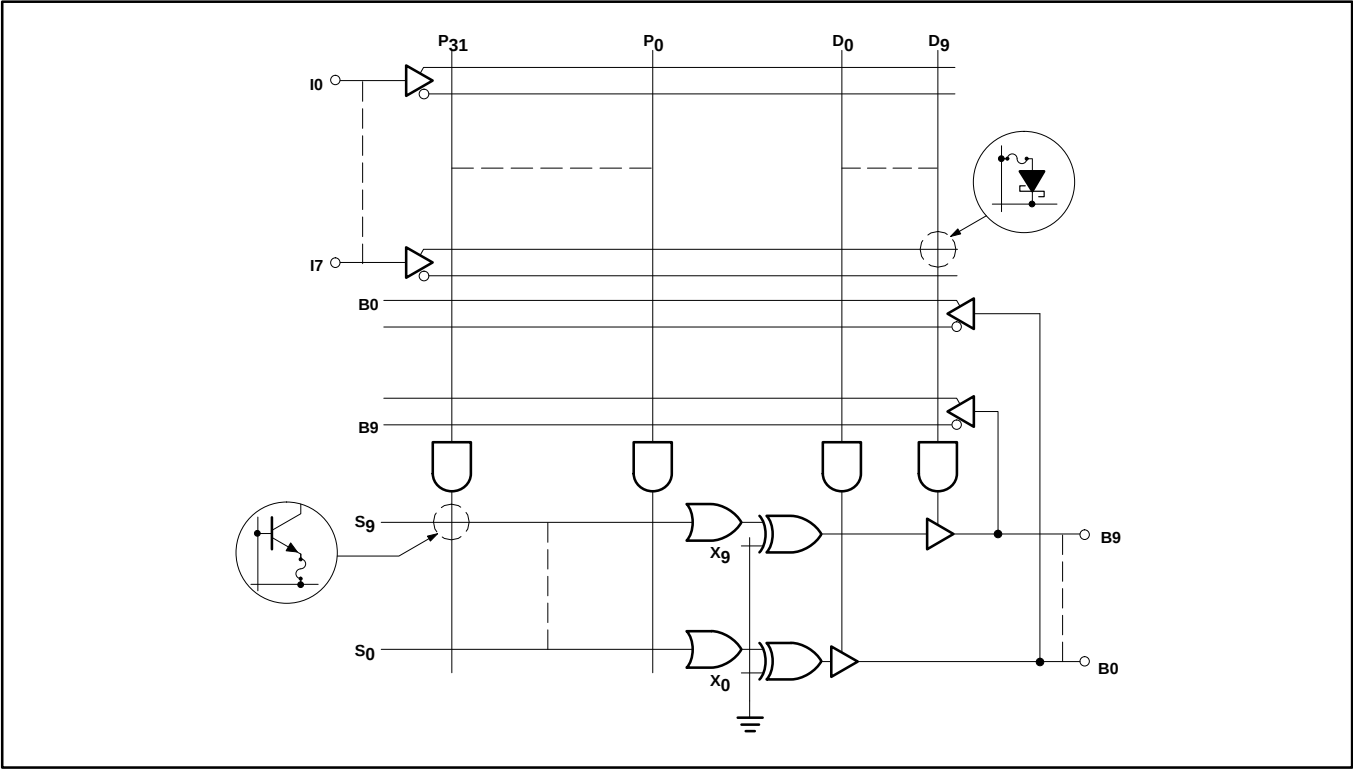
NOTES:

1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ● Programmable connection.

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FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING		UNIT
		MIN	MAX	
V _{CC}	Supply voltage		+7	V _{DC}
V _{IN}	Input voltage		+5.5	V _{DC}
V _{OUT}	Output voltage		+5.5	V _{DC}
I _{IN}	Input currents	−30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{amb}	Operating free-air temperature range	0	+75	°C
T _{stg}	Storage temperature range	−65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

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DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_{amb} ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage ²						
V _{IL}	Low	V _{CC} = MIN	2.0		0.8	V
V _{IH}	High	V _{CC} = MAX			V	
V _{IC}	Clamp	V _{CC} = MIN, I _{IN} = −12mA			V	
Output voltage ²						
V _{OL}	Low ⁴	V _{CC} = MIN I _{OL} = 15mA	2.4	0.4 2.9	0.5	V
V _{OH}	High ⁵	I _{OH} = −2mA			V	
Input current ⁹						
I _{IL}	Low	V _{CC} = MAX V _{IN} = 0.45V		−20 1	−100 40	μA
I _{IH}	High	V _{IN} = V _{CC}			μA	
Output current						
I _{O(OFF)}	Hi-Z state ⁸	V _{CC} = MAX V _{OUT} = 2.7V V _{OUT} = 0.45V	−15	0 −15 −30	80 −140 −70	μA
I _{OS}	Short circuit ^{3, 5, 6}	V _{OUT} = 0V			mA	
I _{CC}	V _{CC} supply current ⁷	V _{CC} = MAX		165	200	mA
Capacitance						
C _{IN}	Input	V _{CC} = 5V V _{IN} = 2.0V		8 15		pF
C _B	I/O	V _B = 2.0V				pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I₀ – I₂ = 0V, inputs I₃ – I₅ = 4.5V, inputs I₇ = 4.5V and I₆ = 10V. For outputs B₀ – B₄ and for outputs B₅ – B₉ apply the same conditions except I₇ = 0V.
5. Same conditions as Note 4 except I₇ = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with inputs I₀ – I₇ and B₀ – B₉ = 0V.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only (I₀ – I₇).

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AC ELECTRICAL CHARACTERISTICS

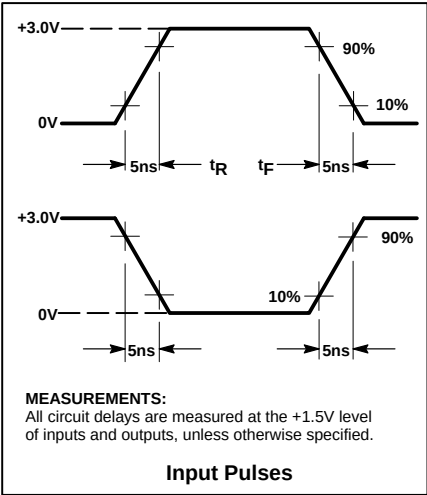
0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V, R₁ = 300Ω, R₂ = 390Ω

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS			UNIT
					MIN	TYP	MAX	
t _{PD}	Propagation Delay ²	Input +/–	Output +/–	C _L = 30pF		8	10	ns
t _{OE}	Output Enable ¹	Input +/–	Output –	C _L = 30pF		8	10	ns
t _{OD}	Output Disable ¹	Input +/–	Output +	C _L = 5pF		8	10	ns

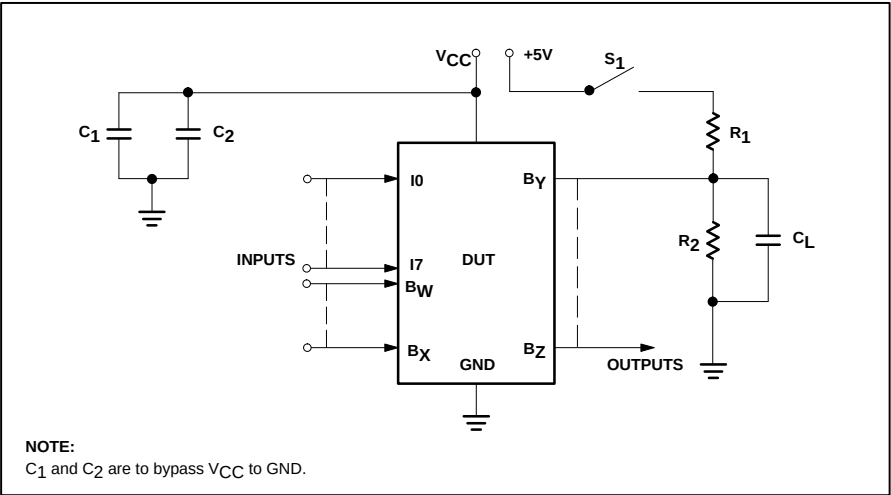
NOTES:

1. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S₁ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} – 0.5V) with S₁ open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S₁ closed.
2. All propagation delays are measured and specified under worst case conditions.

VOLTAGE WAVEFORMS



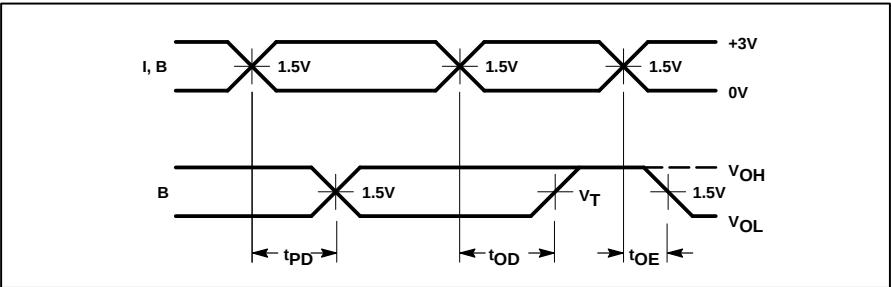
TEST LOAD CIRCUIT



TIMING DEFINITIONS

SYMBOL	PARAMETER
t _{PD}	Propagation delay between input and output.
t _{OD}	Delay between input change and when output is off (Hi-Z or High).
t _{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



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LOGIC PROGRAMMING

The PLUS153–10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ and CUPL™ design software packages also support the PLUS153–10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

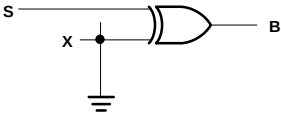
PLUS153–10 logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SNAP only.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

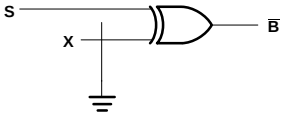
PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Third-Party Programmer/Software Support*) of this data handbook for additional information.

OUTPUT POLARITY – (B)

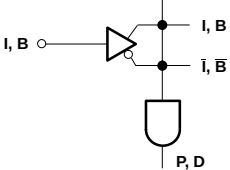


ACTIVE LEVEL	CODE
HIGH ¹ (NON-INVERTING)	H

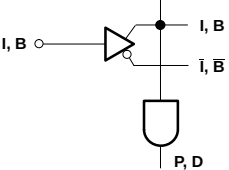


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

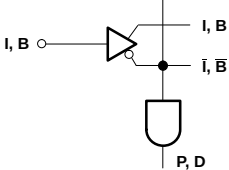
AND ARRAY – (I, B)



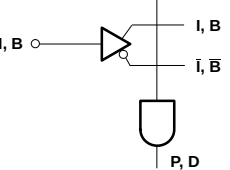
STATE	CODE
INACTIVE ^{1, 2}	O



STATE	CODE
I, B	H

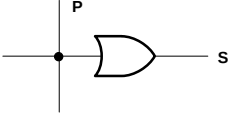


STATE	CODE
I, B	L

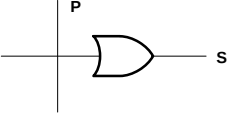


STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P _n STATUS	CODE
ACTIVE ¹	A



P _n STATUS	CODE
INACTIVE	•

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

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PROGRAM TABLE

CUSTOMER NAME _____										PURCHASE ORDER # _____										PHILIPS DEVICE # _____										CE(XXXX)										CUSTOMER SYMBOLIZED PART # _____										TOTAL NUMBER OF PARTS _____										PROGRAM TABLE # _____										REV _____										DATE _____																																							
NOTES In the unprogrammed state: • All AND gates are pulled to a logic "0" (Low). • Output polarity is non-inverting. • Unused I and B bits in the AND array should be programmed as Don't Care (-). • Unused product terms in the OR array should be programmed as INACTIVE (o).										OR <table border="1"> <tr> <td>ACTIVE</td> <td>A</td> <td>B(0)</td> </tr> <tr> <td>INACTIVE</td> <td>•</td> <td></td> </tr> </table> CONTROL <table border="1"> <tr> <td>HIGH</td> <td>H</td> <td>(POL)</td> </tr> <tr> <td>LOW</td> <td>L</td> <td></td> </tr> </table>										ACTIVE	A	B(0)	INACTIVE	•		HIGH	H	(POL)	LOW	L		AND <table border="1"> <tr> <td>INACTIVE</td> <td>0</td> </tr> <tr> <td>I, B</td> <td>H</td> </tr> <tr> <td>$\overline{I}, \overline{B}$</td> <td>L</td> </tr> <tr> <td>DON'T CARE</td> <td>-</td> </tr> </table>										INACTIVE	0	I, B	H	$\overline{I}, \overline{B}$	L	DON'T CARE	-	POLARITY <table border="1"> <tr> <td colspan="20"></td> </tr> <tr> <td colspan="20"></td> </tr> <tr> <td colspan="20"></td> </tr> </table>																																																																					
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Programmable logic array

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SNAP RESOURCE SUMMARY DESIGNATIONS

