

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Added CAGE 75596 as a source of supply. - glg	99-05-04	Raymond Monnin

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						
PMIC N/A	PREPARED BY Charles Reusing				DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles Reusing																			
	APPROVED BY Michael A. Frye																			
	DRAWING APPROVAL DATE 91-05-08																			
	REVISION LEVEL A																			
MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 16K X 4 BITS SRAM, (STD POWER), MONOLITHIC SILICON		SIZE A	CAGE CODE 67268	5962-89712																
SHEET		1	OF	13																

DSCC FORM 2233
APR 97

5962-E229-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

<u>5962-89712</u>	<u>01</u>	<u>X</u>	<u>X</u>
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>	<u>Access time</u>
01		16K X 4 SRAM with separate I/O	45 ns
02		16K X 4 SRAM with separate I/O	35 ns
03		16K X 4 SRAM with separate I/O	25 ns
04		16K X 4 SRAM with separate I/O	20 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	GDIP4-T28 or CDIP3-T28	28	Dual-in-line package
Y	GDFP2-F28	28	Flat package
Z	CQCC4-N28	28	Rectangular chip carrier package
U	CQCC3-N28	28	Rectangular chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage to ground potential (V_{CC})	-----	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-----	-0.5 V dc to +7.0 V dc
DC input voltage (V_{IN}) 1/	-----	-0.5 V dc to +7.0 V dc
DC output current	-----	20 mA
Maximum power dissipation	-----	1.0 W
Lead temperature (soldering, 10 seconds)	-----	+260 C
Thermal resistance, junction-to-case (θ_{JC}):	-----	See MIL-STD-1835
Junction temperature (T_J) 2/	-----	+150 C
Storage temperature range	-----	-65 C to +150 C
Temperature under bias	-----	-55 C to +125 C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	-----	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	-----	0 V dc
Input high voltage (V_{IH})	-----	2.2 V dc minimum
Input low voltage (V_{IL})	-----	0.8 V dc maximum
Operating case temperature range (T_C)	-----	-55 C to +125 C

1/ V_{IL} minimum = -3.0 V for pulse width less than 20 ns.

2/ Maximum junction temperature may be increased to 175 C during burn-in and steady state life.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

- MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicon coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-PRF-38535, appendix A) shall be subjected to and pass the internal moisture content test, (see test method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) TA = +125 C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. Subgroups 7 and 8 shall include verification of the truth table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/ 2/} -55 C ≤ T _C ≤ +125 C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -4.0 mA, V _{IN} = V _{IH} or V _{IL}	1,2,3	All	2.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 8.0 mA, V _{IN} = V _{IH} or V _{IL}	1,2,3	All		0.4	V
Input high voltage	V _{IH} ^{3/}		1,2,3	All	2.2		V
Input low voltage	V _{IL} ^{3/}		1,2,3	All		0.8	V
Input leakage current	I _{IX}	V _{IN} = 5.5 V to GND	1,2,3	All	-10	10	μA
Output leakage current	I _{OZ}	V _{CC} = 5.5 V V _{OUT} = 5.5 V to GND	1,2,3	All	-10	10	μA
Operating supply current	I _{CC1}	V _{CC} = 5.5 V, I _{OUT} = 0 mA CE = V _{IL} , f = f _{MAX} ^{4/}	1,2,3	01.02		140	mA
				03		155	
				04		175	
Standby power supply current, TTL	I _{CC2}	V _{CC} = 5.5 V, I _{OUT} = 0 mA CE = V _{IH} , f = 0 ^{4/} all other inputs V _{IL} or V _{IH}	1,2,3	01.02		50	mA
				03		60	
				04		70	
Standby power supply current, CMOS	I _{CC3}	CE (V _{CC} - 0.2 V), V _{CC} = 5.5 V, f = 0 ^{4/} all other inputs 0.2 V or (V _{CC} - 0.2 V)	1,2,3	01-03		20	mA
				04		25	
Input capacitance	C _{IN} ^{5/}	V _{IN} = 0.0 V, V _{CC} = 5.0 V T _A = +25 C, f = 1 Mhz, (see 4.3.1c)	4	All		8	pF
Output capacitance	C _{OUT} ^{5/}	V _O = 0 V, V _{CC} = 5.0 V T _A = +25 C, f = 1 Mhz, (see 4.3.1c)	4	All		8	pF
Functional tests		See 4.3.1d	7,8A,8B	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ -55 C ≤ T _C ≤ +125 C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t _{AVAV}	See figures 3 and 4	9, 10, 11	01	45	ns	
				02	35		
				03	25		
				04	20		
Address access time	t _{AVQV}		9, 10, 11	01	45	ns	
				02	35		
				03	25		
				04	20		
Output hold from address change	t _{AVQX}		9, 10, 11	All	5	ns	
Chip enable access time	t _{ELQV}		9, 10, 11	01	45	ns	
				02	35		
				03	25		
				04	20		
Chip enable to output active	t _{ELQX}		9, 10, 11	All	5	ns	
Chip select to output inactive	t _{EHQZ}		9, 10, 11	01,02	15	ns	
				03	10		
				04	8		
				01	25		
Output enable to output valid	t _{OLQV}		9, 10, 11	02	20	ns	
				03	12		
				04	10		
				01	25		
Output enable to output active	t _{OLQX}		9, 10, 11	All	3	ns	
Output enable to output inactive	t _{OHQZ}		9, 10, 11	01,02	15	ns	
				03	10		
				04	8		
				01	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ -55 C ≤ T _C ≤ +125 C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to power up 5/	t _{ELPU}	See figures 3 and 4	9, 10, 11	All	0		ns
				01	45		
Chip enable to 5/ power down	t _{EHPD}		9, 10, 11	02	35		ns
				03	25		
				04	20		
				01	40		
Write cycle time	t _{AVAV}		9, 10, 11	02	30		ns
				03	20		
				04	20		
				01	35		
Chip enable to write end	t _{ELWH} t _{ELEH}		9, 10, 11	02	25		ns
				03	20		
				04	17		
				01	35		
Address setup to end of write	t _{AVWH} t _{AVEH}		9, 10, 11	02	25		ns
				03	20		
				04	17		
				01	35		
Address hold from write end	t _{WHAX} t _{EHAX}		9, 10, 11	All	0		ns
Address setup to write start	t _{AVWL} t _{AVEL}		9, 10, 11	All	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} ^{2/} -55 C ≤ T _C ≤ +125 C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write enable pulse width	t _{WLWH} t _{WLEH}	See figures 3 and 4	9, 10, 11	01	35	ns	
				02	25		
				03	20		
				04	17		
Data setup to write end	t _{DVWH} t _{DVEH}		9, 10, 11	01	20	ns	
				02	15		
				03	13		
				04	10		
Data hold from write end	t _{WHDX} t _{EHDX}		9, 10, 11	All	0	ns	
Write enable high to ^{5/} ^{6/} output active	t _{WHQX}		9, 10, 11	All	5	ns	
Write enable low ^{5/} ^{6/} to output inactive	t _{WLQZ}		9, 10, 11	01	15	ns	
				02	10		
				03,04	7		

- ^{1/} AC tests are performed with input rise and fall times of 5 ns or less, timing references levels of 1.5 V, input pulse levels of 0 to 3.0 v, and the output load in figure 3, circuit A.
- ^{2/} CE₁ and CE₂ are represented by CE in table I.
- ^{3/} These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- ^{4/} At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of 1/t_{AVAV}.
- ^{5/} Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
- ^{6/} Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from 1.5 V level on the input with the load in figure 3, circuit B.

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Device types	All
Case outlines	X, Y, Z, U
Terminal number	Terminal Symbol
1	A
2	A
3	A
4	A
5	A
6	A
7	A
8	A
9	A
10	I _O
11	I ₁
12	CE ₁
13	OE
14	GND
15	CE ₂
16	WE
17	O ₀
18	O ₁
19	O ₂
20	O ₃
21	I ₂
22	I ₃
23	A
24	A
25	A
26	A
27	A
28	V _{CC}

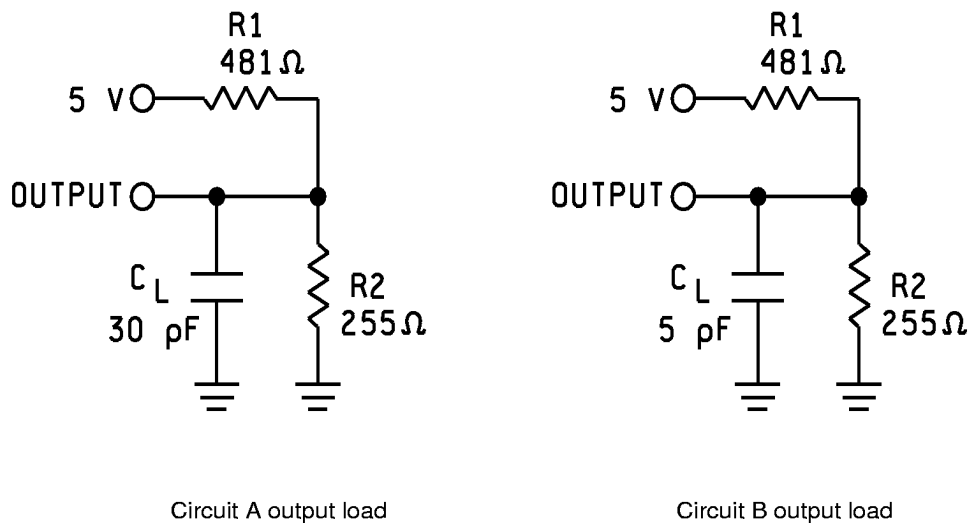
FIGURE 1. Terminal connections.

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CE ₁	CE ₂	WE	OE	Mode	D _{OUT}	Power
H	X	X	X	Not selected	High Z	Standby
X	H	X	X	Not selected	High Z	Standby
L	L	L	X	Write	High Z	Active
L	L	H	L	Read	D _{OUT}	Active
L	L	H	H	Output disable	High Z	Active

FIGURE 2. Truth table.



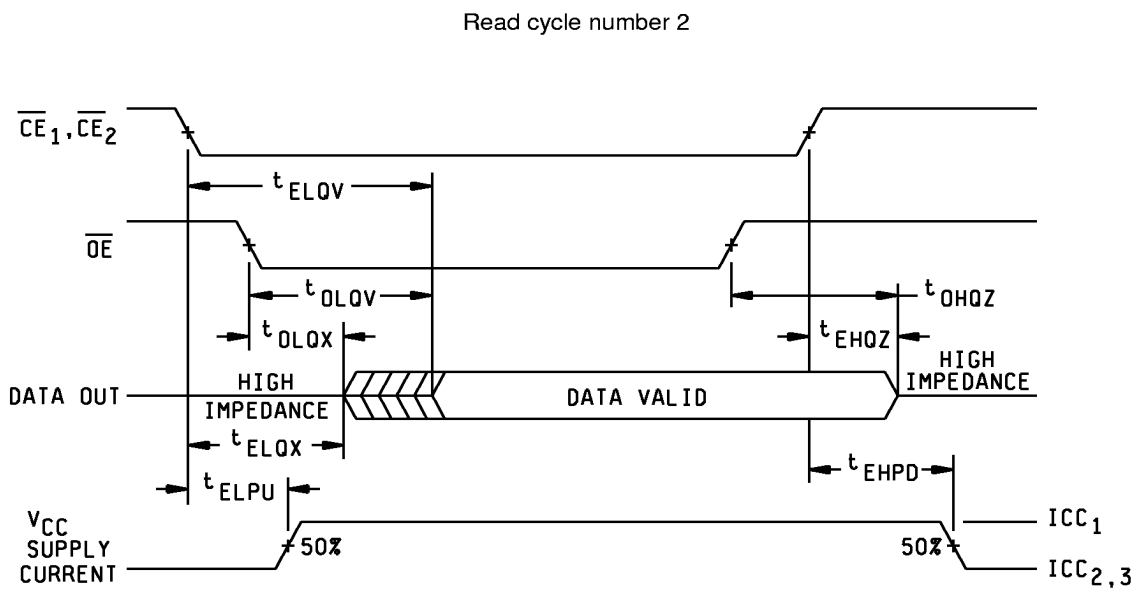
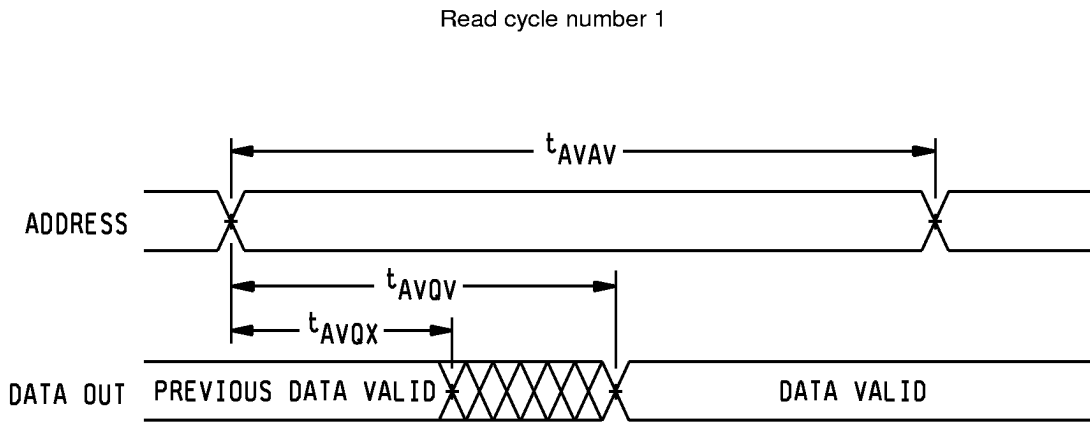
NOTE: Capacitance values include scope and jig capacitance.

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

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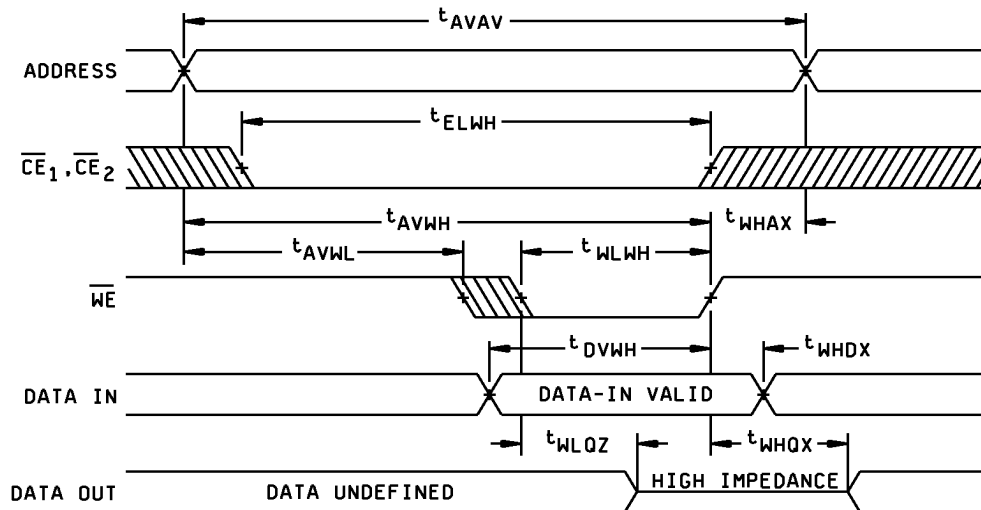
Notes on read operation:

1. WE is high for read cycles.
2. For read cycle number 1, device is continuously selected, CE, OE = V_{IL} .
3. For read cycle number 2, addresses are valid prior to or coincident with CE transition low.

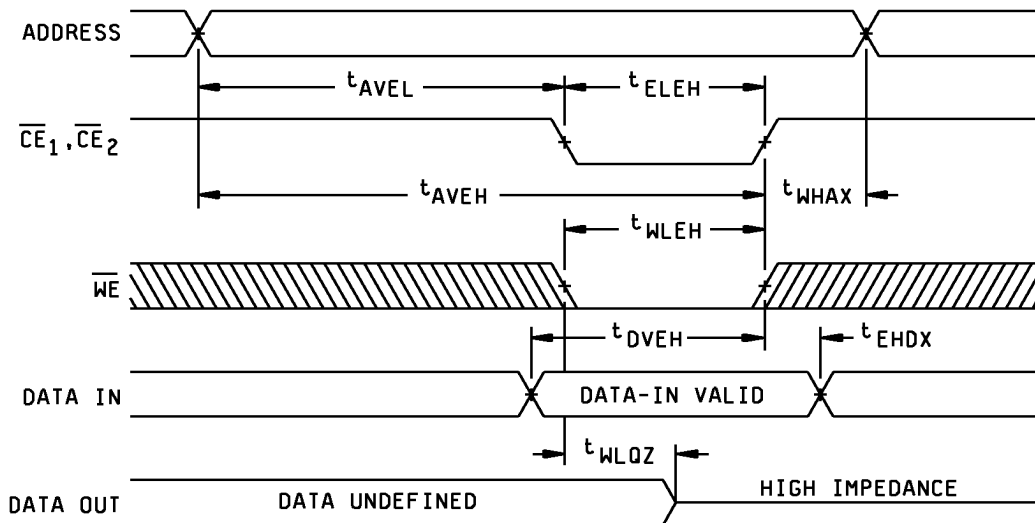
FIGURE 4. Timing waveforms.

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Write cycle number 1 (WE controlled)



Write cycle number 2 (CE controlled)



Notes on write operation:

1. CE or WE must be high during address transitions.
2. If CE switches low coincident with or after WE switches low, the outputs will stay in a high impedance state.
3. If CE switches high coincident with or before WE switches high, the outputs will stay in a high impedance state.
4. A write occurs during the overlap of CE low and WE low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

FIGURE 4. Timing waveforms - continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, (8A, 8B)***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

- * PDA applies to subgroup 1 and 7.
- ** For subgroup see 4.3.1c.
- *** For subgroups 7, 8A and 8B, see 4.3.1d.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) TA = +125 C, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-05-04

Approved sources of supply for SMD 5962-89712 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing part number <u>1/</u>	Vendor CAGE number	Vendor similar part number <u>3/</u>
5962-8971201XA	<u>2/</u> <u>2/</u> 75596	CY7C162A-45DMB IDT71982S45DB P4C1982-45CMB
5962-8971201YA	<u>2/</u> 75596	CY7C162A-45KMB P4C1982-45FMB
5962-8971201UA	<u>2/</u> <u>2/</u> 75596	CY7C162A-45LMB IDT71982S45LB P4C1982-45LMB
5962-8971201ZA	<u>2/</u> 75596	CY7C162A-45LMB P4C1982-45LMB
5962-8971202XA	<u>2/</u> <u>2/</u> 75596	CY7C162A-35DMB IDT71982S35DB P4C1982-35CMB
5962-8971202YA	<u>2/</u> 75596	CY7C162A-35KMB P4C1982-35FMB
5962-8971202UA	<u>2/</u> <u>2/</u> 75596	CY7C162A-35LMB IDT71982S35LB P4C1982-35LMB
5962-8971202ZA	<u>2/</u> 75596	CY7C162A-35LMB P4C1982-35LMB
5962-8971203XA	<u>2/</u> <u>2/</u> 75596	CY7C162A-25DMB IDT71982S25DB P4C1982-25CMB
5962-8971203YA	<u>2/</u> 75596	CY7C162A-25KMB P4C1982-25FMB
5962-8971203UA	<u>2/</u> <u>2/</u> 75596	CY7C162A-25LMB IDT71982S25LB P4C1982-25LMB
5962-8971203ZA	<u>2/</u> 75596	CY7C162A-25LMB P4C1982-25LMB
5962-8971204XA	<u>2/</u> <u>2/</u> 75596	CY7C162A-20DMB IDT71982S20DB P4C1982-20CMB
5962-8971204YA	<u>2/</u> 75596	CY7C162A-20KMB P4C1982-20FMB
5962-8971204UA	<u>2/</u> <u>2/</u> 75596	CY7C162A-20LMB IDT71982S20LB P4C1982-20LMB
5962-8971204ZA	<u>2/</u> 75596	CY7C162A-20LMB P4C1982-20LMB

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN - continued.

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.
- 2/ Not available from an approved source of supply.
- 3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

75596

Vendor name
and address

Performance Semiconductor Corporation
630 East Weddell Drive
Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.