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T-49-19-61

PRELIMINARY

MATRA M H S

September 1989

DATA SHEET

83C154/83C154D

CMOS SINGLE-CHIP 8 BIT MICROCONTROLLER

- 83C154 - CMOS SINGLE CHIP 8 BIT MICRO-CONTROLLER with factory mask programmable ROM
- 83C154D - 83C154 with DOUBLE ROM (under development)
- 80C154 : ROMLESS version of 83C154
- 80C154/83C154 : 0 to 12 MHz
- 80C154-1/83C154-1 : 0 to 16 MHz
- 80C154-L/83C154-L : V_{CC} = 2.7 V to 5.5 V (0 to 6 MHz)
- 83C154F : SECRET ROM VERSION

FEATURES

- 16 K x 8 BIT INTERNAL ROM (32 K x 8 for 83C154D)
- 256 x BIT RAM
- 32 PROGRAMMABLE I/O LINES (PROGRAMMABLE IMPEDANCE)
- THREE 16-BIT TIMER/COUNTERS (INCLUDING WATCH DOG AND 32 BIT TIMER)
- 64 K PROGRAM MEMORY SPACE
- FULLY STATIC DESIGN
- POWER CONTROL MODES
- INTERRUPT PRIORITY CONTROL
- 0 TO 16 MHz
- BOOLEAN PROCESSOR
- 6 INTERRUPT SOURCES
- PROGRAMMABLE SERIAL PORT
- 64 K DATA MEMORY SPACE
- TEMPERATURE RANGE : Commercial, Industrial, Automotive and Military

DESCRIPTION

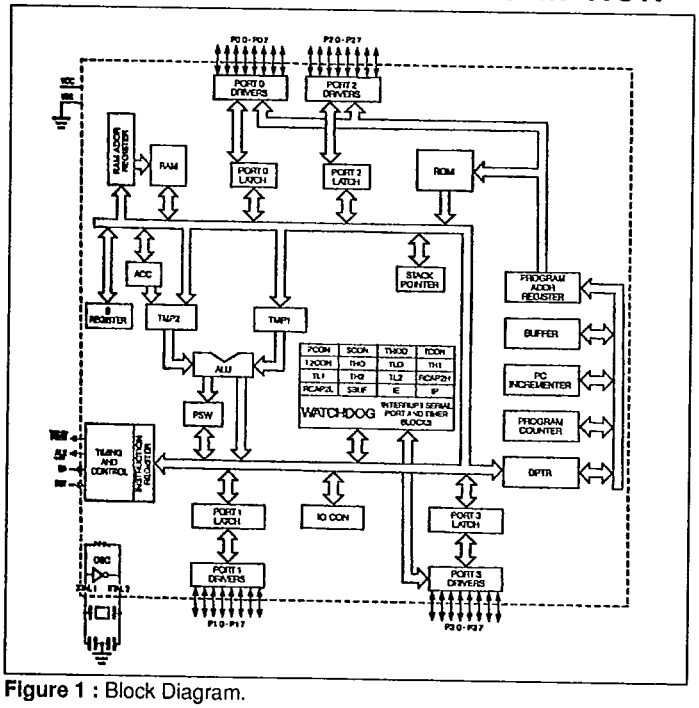

Figure 1 : Block Diagram.

The 83C154/83C154D retains all the features of the MHS 80C52 with extended ROM capacity (16 K bytes or 32 K bytes), 256 bytes of RAM, 32 I/O lines, a 6-source 2-level interrupts, a full duplex serial port, an on-chip oscillator and clock circuits, three 16 bit timers with extra features : 32 bit timer and watch dog functions. Timer 0 and 1 can be configured by program to implement a 32 bit timer. The watch dog function can be activated either with timer 0, or timer 1 or both together (32 bit timer). In addition, the 83C154/83C154D has two software selectable modes of reduced activity for further reduction of power consumption. In the Idle Mode, the CPU is frozen while the RAM is saved, and the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode, the RAM is saved and the timers, serial port and interrupts continue to function when driven by external clocks. In addition as for the MHS 80C51/C52, the stop clock mode is also available.

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MHS provides a new member in the 83C154/154D Family named "83C154F/C154DF" which permits full protection of the internal ROM contents.

With a non protected 83C154/C154D, it is very easy to read out the contents of the internal 16 K/32 K bytes of ROM.

Three methods exist, two of them are special test modes and the last one is by means of MOVC instructions.

- **Test mode "VER" :** Using this special test mode, the internal ROM contents are output on port P0 ; the address being applied on ports P2 (AD15...AD8) and P1 (AD7...AD0).
- **Test mode "TMB" :** With this second test mode, the contents of the 83C154/C154D internal bus is presented on port P1 during the PH2 clock phases.
- **Using MOVC instructions :** If EA = 0, and following a reset, the 83C154/C154D fetches its instructions from external program memory. It is then possible to write a small program whose purpose is to dump the internal ROM contents by means of MOVC A, @A + DPTR and MOVC A, @A + PC instructions.

83C154F/C154DF WITH PROGRAM PROTECTION FEATURES

This new version adds ROM protection features in some strategic points of the 83C154F/C154DF in order to eliminate the possibility of reading the ROM contents (once the protection has been programmed) by one if the three forementioned methods (VER and TMB test modes, or MOVC instructions).

Nevertheless the customer must note the following :

- Once the protection has been programmed, the 83C154F/C154DF program always starts at address 0 in the internal ROM.
- The application program must be self contained in the internal 16 K/32 K of ROM, otherwise it would be possible to trap the program counter address in the external PROM/EPROM and then to dump the internal ROM contents by means of a patch using MOVC instructions.

Thus, if an extra EPROM is necessary, it is advised to ensure that it will contain only constants or tables.

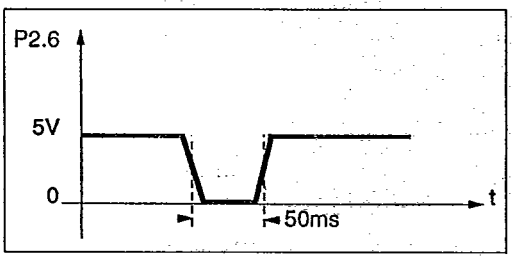
TEST OF THE ONE CHIP PROGRAM MEMORY

- **Before protection is activated :** The 83C154F/C154DF can be tested as any normal 83C154/C154D (using test equipment or any other methods).
- **After protection is activated :** It is then no longer possible to dump the internal ROM contents.

HOW TO PROGRAM THE PROTECTION MECHANISM

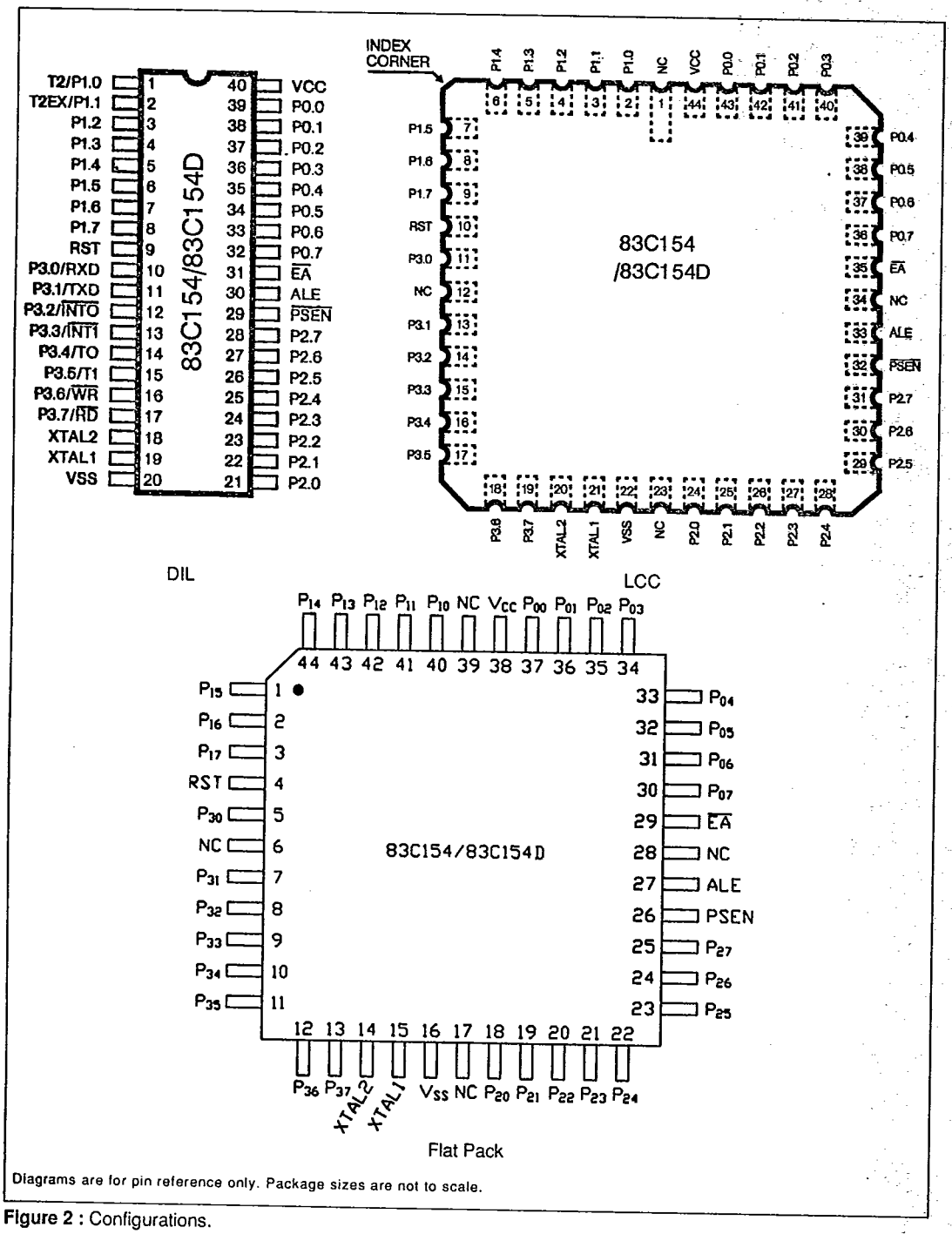
- To burn correctly the fuse a specific configuration of inputs must be settled as below :
  - RST = ALE = 1
  - P2.7 = 1

Furthermore PSEN signal must be tied at + 9 V ± 5 % level voltage and a pulse must be applied on P2.6 input Port. The timing on P2.6 is shown below :



Time Rise and Fall Rise ≤ 100 µs.

- The electrical schematic shows a typical application to deliver P2.6 signal.



Diagrams are for pin reference only. Package sizes are not to scale.

Figure 2 : Configurations.

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IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. The interrupt, serial port, and timer blocks continue to function only with external clock (INT0, INT1, T0, T1).

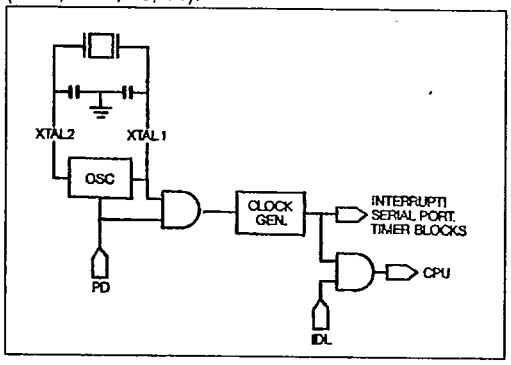


Figure 3 : Idle and Power Down Hardware.

Idle Mode operation allows the interrupt, serial port, and timer blocks to continue to function with internal or external clocks, while the clock to CPU is gated off. The special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON : Power Control Register

(MSB)							(LSB)
SMOD	HPD	RPD	-	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
HPD	PCON.	Hard power Down bit. Setting this bit allows CPU to enter in Power Down state on an external event (1 to 0 transition) on bit T1 (p. 3-5) the CPU quit the Hard Power Down mode when bit T1 (p. 3-5) go high or when reset is activated
RPD	PCON.5	Recover from Idle or Power Down bit. When 0 RPD has no effect. When 1, RPD permits to exit from idle or Power Down with any non enabled interrupt source (except timex 2). In this case the program start at the next address. When interrupt is enabled, the appropriate interrupt routine is serviced.
-	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

IDLE MODE

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. In the idle mode, the internal clock signal is gated off to the CPU, but interrupt, timer and serial port functions are maintained. Table 1 describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

The third way to terminate the Idle mode is the activation of any disabled interrupt when recover is programmed (RPD = 1). This will cause PCON.0 to be cleared. No interrupt is serviced. The next instruction is executed. If interrupt are disabled and RPD = 0, only a

POWER DOWN MODE

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The three ways to terminate the Power Down mode are the same than the Idle mode. But since the onchip oscillator is stopped, the external interrupts, timers and serial port must be sourced by external clocks only, via INT0, INT1, T0, T1.

In the Power Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken

to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

When using voltage reduction : interrupt, timers and serial port functions are guaranteed in the V_{CC} specification limits.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the port switches from 0 to 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in figure 4.

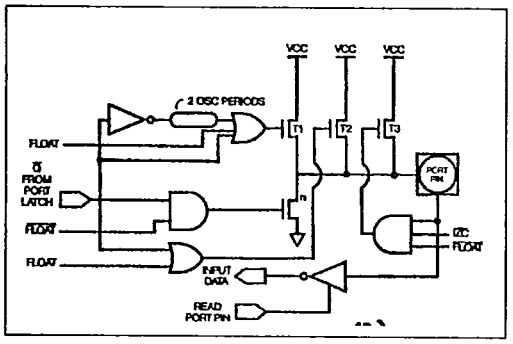


Figure 4 : I/O Buffers in the 83C154/83C154D (Ports 1, 2, 3).

STOP CLOCK MODE

Due to static design, the MHS 83C154/83C154D clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

83C154/83C154D I/O PORTS

The I/O drives for P1, P2, P3 of the 83C154/83C154D are impedance programmable. The I/O buffers for Ports 1, 2 and 3 are implemented as shown in *figure 4.*

When the port latch contains 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the I_{OH} source current. This inverter and T3 form a latch which holds the 1 and is supported by T2. When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

The input impedance of Port 1, 2, 3 are programmable through the register IOCON. The ALF bit (IOCON0) set all of the Port 1, 2, 3 floating when a Power Down mode occurs. The P1HZ, P2HZ, P3HZ bits (IOCON1, IOCON2, IOCON3) set respectively the Ports P1, P2, P3 in floating state. The IZC (IOCON4) allows to choose input impedance of all ports (P1, P2, P3). When IZC = 0, T2 and T3 pullup of I/O ports are active ; the internal input impedance is approximately 10 K. When IZC = 1 only T2 pull-up is active. The T3 pull-up is turned off by IZC. The internal impedance is approximately 100 K.

PIN DESCRIPTIONS

V_{SS}

Circuit ground potential.

V_{CC}

Supply voltage during normal, Idle, and Power Down operation.

PORT 0

Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Table 1 : Status of the external pins during Idle and Power Down Modes.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 83C154/-83C154D. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

PORT 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, an in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.
Port 1 also receives the low-order address byte during program verification. In the 83C154, Port 1 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

PORT 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
It also receives the high-order address bits and control signals during program verification in the 83C154. Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

PORT 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the MHS-51 Family, as listed below.

Port Pin	Alternate Function
P3.0	$\overline{RXD}$ (serial input port)
P3.1	$\overline{TXD}$ (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	$\overline{RD}$ (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits Power-On reset using only a capacitor connected to V_{CC}.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{PSEN}$

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{EA}$

When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 3 FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in *figure 5*. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 6*. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-

by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

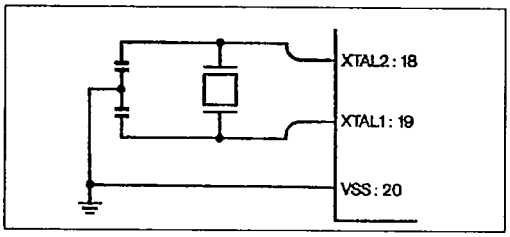


Figure 5 : Crystal Oscillator.

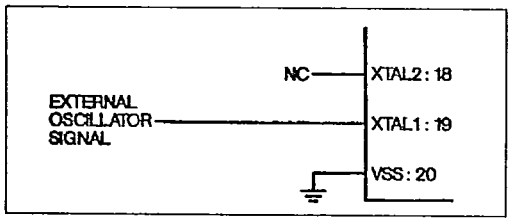


Figure 6 : External Drive Configuration.

PORT 1 SECONDARY FUNCTIONS

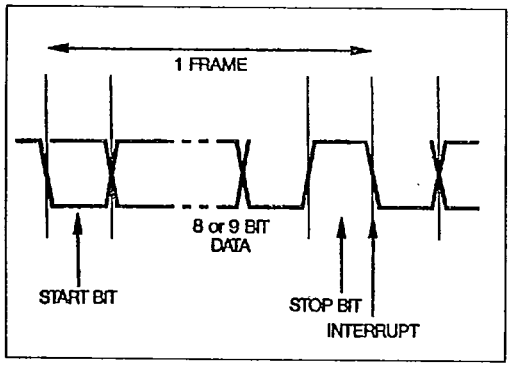
This is a quasi-bidirectional I/O port, internally pulled up when used as input ports. Two of the ports have been allocated a second function which are :
P1.0 [T2] : External clock input for timer/counter 2.
P1.1 [T2EX] : A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

INTERRUPT MODES

The MHS 80C154/83C154/83C154D is capable of handling two external interrupts, three interrupts from the timers, and one interrupt from the serial port, through its incorporated six source, two-level interrupt structure.

SERIAL PORT TIMING

The interrupt is executed after the Stop Bit.



TIMER FUNCTIONS

In fact, timer 0 & 1 can be connected by a software instruction to implement a 32-bit timer function. Timer 0 (mode 3) or timer 1 (mode 0, 1, 2) or a 32-bit timer consisting of timer 0 + timer 1 can be employed in the watchdog mode, in which case a CPU reset is generated upon a TF1 flag.
The internal pull-up resistances at ports 1 – 3 can be set to a ten times increased value simply by software.

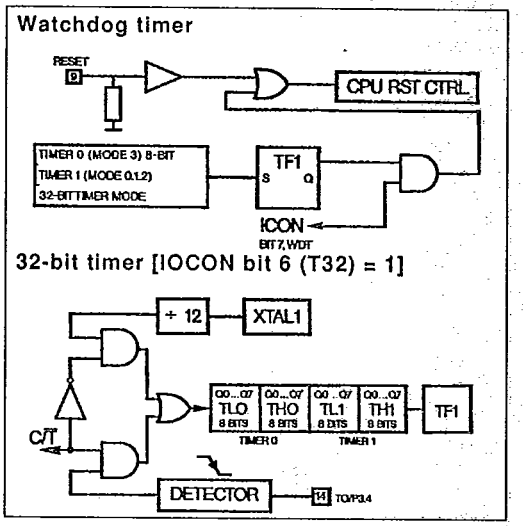


Figure 7.

TIMER/EVENT COUNTER 2

Timer 2 is a 16-bit timer/counter like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/T2 in the Special Function Register T2CON *(Figure 7)*. It has three operating modes : "capture", "autoload", and "baud rate generator", which are selected by bits in T2CON as shown in

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16 bit auto-reload
0	1	1	16-bit capture
1	X	1	baud rate generator
X	X	0	(off)

Table 2 : Timer 2 Operating Modes.

Table 2.

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 ans TH2, to be

captured into registers RCAP2L and RCAP2H, respectively. (RCAP2L and RCAP2H are new Special Function Registers in the 80C52). In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.
The capture mode is illustrated in *Figure 8*.
In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.
The auto-reload mode is illustrated in *Figure 9*.

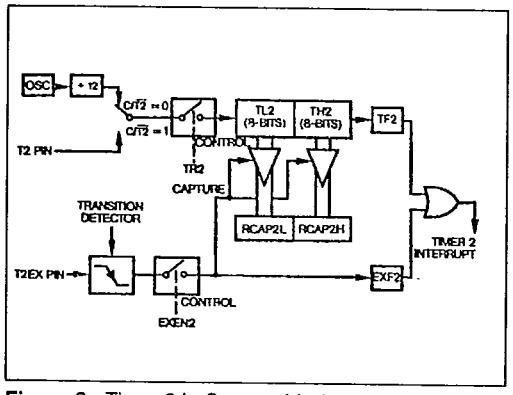


Figure 8 : Timer 2 in Capture Mode.

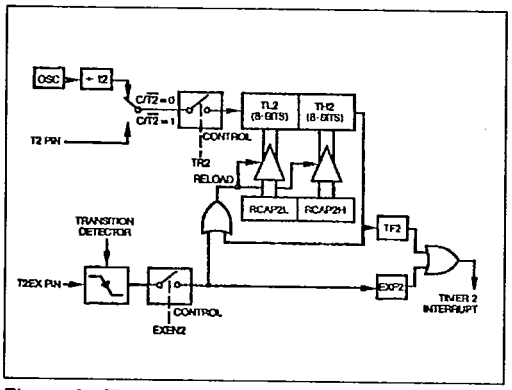


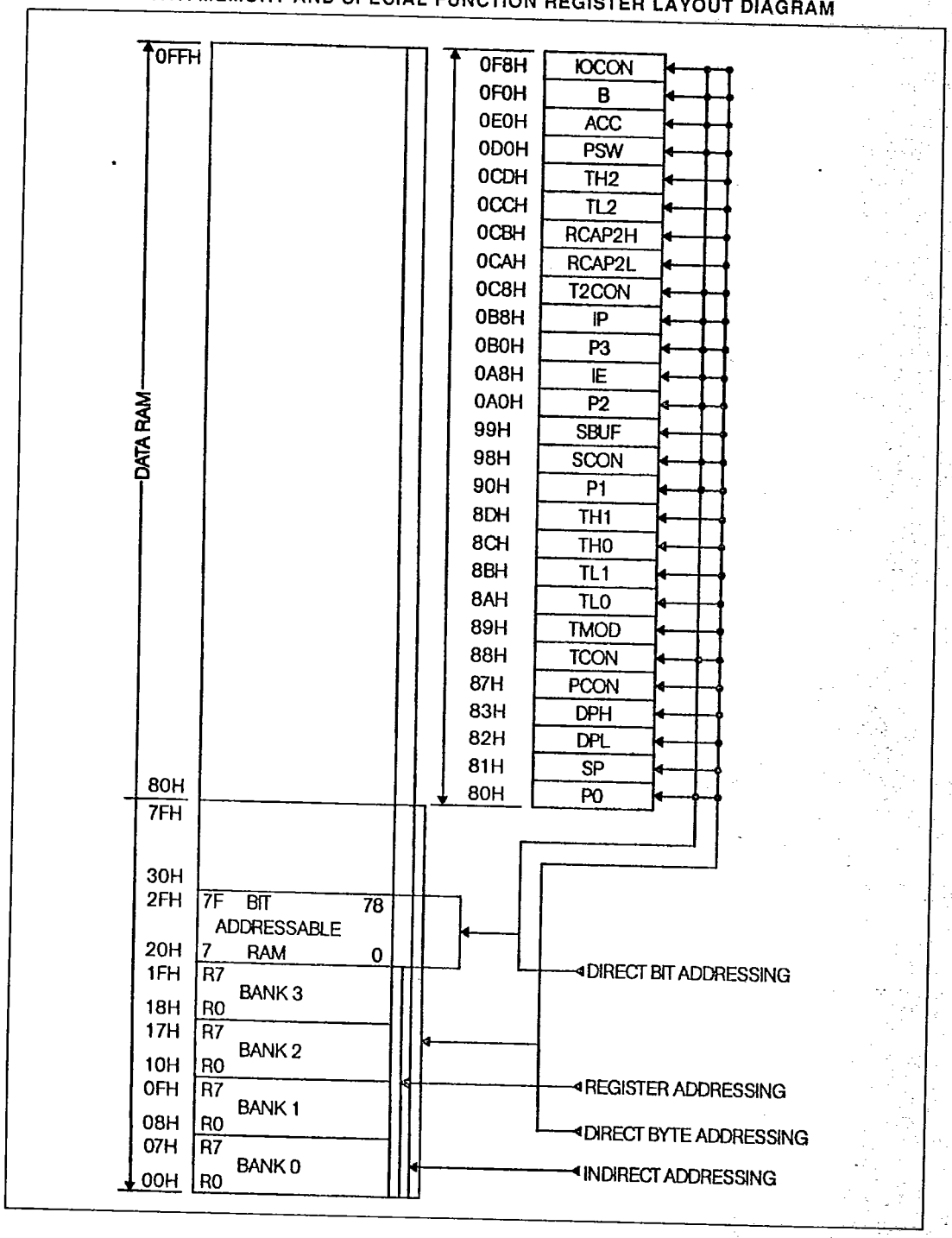
Figure 9 : Timer 2 in Auto-Reload Mode.

(MSB)							(LSB)
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events as T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN 2 = 1. When cleared, auto reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Figure 7 : T2CON :
Timer/Counter 2 Control Register.

DATA MEMORY AND SPECIAL FUNCTION REGISTER LAYOUT DIAGRAM



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DETAILED DIAGRAM OF DATA MEMORY (RAM)

0FFH									255	INDIRECT ADDRESSING
7FH									127	DIRECT BYTE ADDRESSING
2FH	7F	7E	7D	7C	7B	7A	79	78	47	DIRECT BIT ADDRESSING
2EH	77	76	75	74	73	72	71	70	46	
2DH	6F	6E	6D	6C	6B	6A	69	68	45	
2CH	67	66	65	64	63	62	61	60	44	
2BH	5F	5E	5D	5C	5B	5A	59	58	43	
2AH	57	56	55	54	53	52	51	50	42	
29H	4F	4E	4D	4C	4B	4A	49	48	41	
28H	47	46	45	44	43	42	41	40	40	
27H	3F	3E	3D	3C	3B	3A	39	38	39	
26H	37	36	35	34	33	32	31	30	38	
25H	2F	2E	2D	2C	2B	2A	29	28	37	
24H	27	26	25	24	23	22	21	20	36	
23H	1F	1E	1D	1C	1B	1A	19	18	35	
22H	17	16	15	14	13	12	11	10	34	
21H	0F	0E	0D	0C	0B	0A	09	08	33	
20H	07	06	05	04	03	02	01	00	32	
1FH	Bank 3								31	REGISTER ADDRESSING
18H									24	
17H	Bank 2								23	
10H									16	
0FH	Bank 1								15	
08H									8	
07H	Bank 0								7	
00H									0	

DETAILED DIAGRAM OF SPECIAL FUNCTION REGISTERS

Direct Byte Address	Bit Address (MSB)							(LSB)	Special Function Register Symbol
	WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF	
0F8H	FF	FE	FD	FC	FB	FA	F9		IOCON
0F0H	F7	F6	F5	F4	F3	F2	F1	F0	B
0E0H	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	CY	AC	F0	RS1	RS0	0V	F1	P	
0D0H	D7	D6	D5	D4	D3	D2	D1	D0	PSW
0CDH	Not Bit Addressable								TH2
0CCH	Not Bit Addressable								TL2
0CBH	Not Bit Addressable								RCAP2H
0CAH	Not Bit Addressable								RCAP2L
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	
0C8H	CF	CE	CD	CC	CB	CA	C9	C8	T2CON
	PCT		PT2	PS	PT1	PX1	PT0	PX0	
0B8H	BF	-	BD	BC	BB	BA	B9	B8	IP
0B0H	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA		ET2	ES	ET1	EX1	ET0	EX0	
0A8H	AF	-	AD	AC	AB	AA	A9	A8	IE
0A0H	A7	A6	A5	A4	A3	A2	A1	A0	P2
99H	Not Bit Addressable								SBUF
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
98H	9F	9E	9D	9C	9B	9A	99	98	SCON
90H	97	96	95	94	93	92	91	90	P1
8DH	Not Bit Addressable								TH1
8CH	Not Bit Addressable								TH0
8BH	Not Bit Addressable								TL1
8AH	Not Bit Addressable								TL0
89H	Not Bit Addressable								TMOD
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
88H	8F	8E	8D	8C	8B	8A	89	88	TCON
87H	Not Bit Addressable								PCON
83H	Not Bit Addressable								DPH
82H	Not Bit Addressable								DPL
81H	Not Bit Addressable								SP
80H	87	86	85	84	83	82	81	80	P0

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TIME MODE REGISTER (TMOD)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TMOD	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

BIT LOCATION	FLAG	FUNCTION		
TMOD.0	M0	M1	M0	Timer/counter 0 mode setting.
		0	0	8-bit timer/counter with 5-bit prescalar.
		0	1	16-bit timer/counter.
		1	0	8-bit timer/counter with 8-bit auto reloading.
TMOD.1	M1	1	1	Timer/counter 0 separated into TL0 (8-bit) timer/counter and TH0 (8-bit) timer/counter. TF0 is set by TL0 carry, and TF1 is set by TH0 carry.
TMOD.2	C/$\overline{T}$	Timer/counter 0 count clock designation control bit. XTAL1.2 divided by 12 clocks is the input applied to timer/counter 0 when C/$\overline{T}$ = "0". The external clock applied to the T0 pin is the input applied to timer/counter 0 when C/$\overline{T}$ = "1".		
TMOD.3	GATE	When this bit is "0", the TR0 bit of TCON (timer control register) is used to control the start and stop of timer/counter 0 counting. If this bit is "1", timer/counter 0 starts counting when both the TR0 bit of TCON and $\overline{INT0}$ pin input signal are "1", and stops counting when either is changed to "0".		
TMOD.4	M0	M1	M0	Timer/counter 1 mode setting.
		0	0	8-bit timer/counter with 5-bit prescalar.
		0	1	16-bit timer/counter.
TMOD.5	M1	1	0	8-bit timer/counter with 8-bit auto reloading.
		1	1	Timer/counter 1 operation stopped.
TMOD.6	C/$\overline{T}$	Timer/counter 1 count clock designation control bit. XTAL.2 divided by 12 clocks is the input applied to timer/counter 1 when C/$\overline{T}$ = "0". The external clock applied to the T1 pin is the input applied to timer/counter 1 when C/$\overline{T}$ = "1".		
TMOD.7	GATE	When this bit is "0", the TR1 bit of TCON is used to control the start and stop of timer/counter 1 countig. If this bit is "1", timer/counter 1 starts counting when both the TR1 bit of TCON and $\overline{INT1}$ pin input signal are "1", and stops counting when either is changed to "0".		

POWER CONTROL REGISTER (PCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PCON	87H	SMOD	HPD	RPD	–	GF1	GF0	PD	IDL

BIT LOCATION	FLAG	FUNCTION
PCON.0	IDL	IDLE mode set when this bit is set to "1". CPU operations are stopped when IDLE mode is set, but XTAL1-2, timer/counters 0, 1 and 2, the interrupt circuits, and serial port remain active. IDLE mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.1	PD	PD mode set when this bit is set to "1". CPU operations and XTAL1-2 are stopped when PD mode is set. PD mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.2	GF0	General purpose bit. Testing this flag when IDLE mode is cancelled by an interrupt shows whether the interrupt is a normal interrupt or an IDLE mode release interrupt.
PCON.3	GF1	General purpose bit. Testing this flag when PD mode is cancelled by an interrupt shows whether the interrupt is a normal interrupt or a PD mode release interrupt.
PCON.4	–	Reserved bit. The output data is "1" if the bit is read.
PCON.5	RPD	Bit used to specify cancellation of CPU power down mode (IDLE or PD) by interrupt signal. Power down mode cannot be cancelled by interrupt signal if interrupt is not enabled by IE (interrupt enable register) when this bit is "0". If the interrupt flag is set to "1" by an interrupt request signal when this bit is "1" (even if interrupt is disabled), the program is executed from the next address of the power down mode setting instruction. The flag is reset to "0" by software.
PCON.6	HPD	The hard power down setting mode is enabled when this bit is set to "1". If the level of the power failure detect signal applied to the HPD1 pin (pin 3.5) is changed from "1" to "0" when this bit is "1", XTAL1-2 oscillation is stopped and the system is put into hard power down mode. HPD mode is cancelled when the CPU is reset, or HPD1 pin go high.
PCON.7	SMOD	When the timer/counter 1 carry signal is used as a clock in mode 1, 2 or 3 of the serial port, this bit has the following functions. The serial port operation clock is reduced by 1/2 when the bit is "0" for delayed processing. And when the bit is "1", the serial port operation clock is normal for faster processing.

ENABLE	RECOVER	
0	0	PWD not cancelled
1	0	Execute interrupt routine
0	1	Execute next address
1	1	Execute interrupt routine

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TIMER CONTROL REGISTER (TCON) T-49-19-61

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TCON	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT LOCATION	FLAG	FUNCTION
TCON.0	IT0	External interrupt 0 signal used in level detect mode when this bit is "0", and in trigger detect mode when "1".
TCON.1	IE0	Interrupt request flag for external interrupt 0. Bit is reset automatically when interrupt is serviced. Bit can be set an reset by software when IT0 = "1".
TCON.2	IT1	External interrupt 1 signal used in level detect mode when this bit is "0", and in trigger detect mode when "1".
TCON.3	IE1	Interrupt request flag for external interrupt 1. Bit is reset automatically when interrupt is serviced. Bit can be set and reset by software when IT1 = "1".
TCON.4	TR0	Counting start and stop control bit for timer/counter 0. Timer/counter 0 starts counting when this bit is "1", and stops counting when "0".
TCON.5	TF0	Interrupt request flag for timer interrupt 0. Bit is reset automatically when interrupt is serviced. Bit is set to "1" when carry signal is generated from timer/counter 0.
TCON.6	TR1	Counting start and stop control bit for timer/counter 1. Timer/counter 1 starts counting when this bit is "1", and stops counting when "0".
TCON.7	TF1	Interrupt request flag for timer interrupt 1. Bit is reset automatically when interrupt is serviced. Bit is set to "1" when carry signal is generated from timer/counter 1.

SERIAL PORT CONTROL REGISTER (SCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
SCON	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

BIT LOCATION	FLAG	FUNCTION
SCON.0	RI	"End of serial port reception" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been received when in mode 0, or by the STOP bit when in any other mode. In mode 2 or 3, however RI is not set if the RB8 data is "0" with SM2 = "1". RI is set in mode 1 if STOP is received when SM2 = "1".
SCON.1	TI	"End of serial port transmission" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been sent when in mode 0, or after the last bit of data has been when in any other mode.
SCON.2	RB8	The ninth bit of data received in mode 2 or 3 is passed to RB8. The STOP bit is applied to RB8 if SM2 = "0" when in mode 1. RB8 can not be used in mode 0.
SCON.3	TB8	The TB8 data is sent as the ninth data bit when in mode 2 or 3. Any desired data can be set in TB8 by software.
SCON.4	REN	Reception enable control bit. No reception when REN = "0". Reception enabled when REN = "1".
SCON.5	SM2	If the ninth bit of received data is "0" with SM2 = "1" in mode 2 or 3, the "end of reception" signal is not set in the RI flag. Nor is the "end of reception" signal set in the RI flag if the STOP bit is not "1" when SM2 = "1" in mode 1.
SCON.6	SM1	SM0 = 0, SM1 = 0, MODE = 0: 8-bit shift register I/O.
		SM0 = 0, SM1 = 1, MODE = 1: 8-bit UART variable baud rate.
SCON.7	SM0	SM0 = 1, SM1 = 0, MODE = 2: 9-bit UART 1/32 XTAL1, 1/64 XTAL1 baud rate.
		SM0 = 1, SM1 = 1, MODE = 3: 9-bit UART variable baud rate.

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INTERRUPT ENABLE REGISTER (IE)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IE	0A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0

BIT LOCATION	FLAG	FUNCTION
IE.0	EXQ	Interrupt control bit for external interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.1	ET0	Interrupt control bit for timer interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.2	EX1	Interrupt control bit for external interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.3	ET1	Interrupt control bit for timer interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.4	ES	Interrupt control for serial port. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.5	ET2	Interrupt control bit for timer interrupt 2. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.6	–	Reserved bit. The output data is "1" if the bit is read.
IE.7	EA	Overall interrupt control bit. All interrupts are disabled when bit is "0". All interrupts are controlled by IE.0 through IE.5 when bit is "1".

INTERRUPT PRIORITY REGISTER (IP)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IP	0B8H	PCT	–	PT2	PS	PT1	PX1	PT0	PX0

BIT LOCATION	FLAG	FUNCTION
IP.0	PX0	Interrupt priority bit for external interrupt 0. Priority is assigned when bit is "1".
IP.1	PT0	Interrupt priority bit for timer interrupt 0. Priority is assigned when bit is "1".
IP.2	PX1	Interrupt priority bit for external interrupt 1. Priority is assigned when bit is "1".
IP.3	PT1	Interrupt priority bit for timer interrupt 1. Priority is assigned when bit is "1".
IP.4	PS	Interrupt priority bit for serial port. Priority is assigned when bit is "1".
IP.5	PT2	Interrupt priority bit for timer interrupt 2. Priority is assigned when bit is "1".
IP.6	–	Reserved bit. The output data is "1" if the bit is read.
IP.7	PCT	Priority interrupt circuit control bit. The priority register contents are valid and priority assigned interrupts can be processed when this bit is "0". When the bit is "1", the priority interrupt circuit is stopped, and interrupts can only be controlled by the interrupt enable register (IE).

PROGRAM STATUS WORD REGISTER (PSW)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PSW	0D0H	CY	AC	F0	RS1	RS0	OV	F1	P

BIT LOCATION	FLAG	FUNCTION
PSW.0	P	Accumulator (ACC) parity indicator. "1" when the "1" bit number in the accumulator is an odd number, and "0" when an even number.
PSW.1	F1	User flag which may be set to "0" or "1" as desired by the user.
PSW.2	OV	Overflow flag which is set if the carry C_6 from bit 6 of the ALU or CY is "1" as a result of an arithmetic operation. The flag is also set to "1" if the resultant product of executing a multiplication instruction (MULAB) is greater than 0FFH, but is reset to "0" if the product is less than or equal to 0FFH.
PSW.3	RS0	RAM register bank switch.
PSW.4	RS1	RS1 / RS0 / BANK / RAM ADDRESS 0 / 0 / 0 / 00H - 07H 0 / 1 / 1 / 08H - 0FH 1 / 0 / 2 / 10H - 17H 1 / 1 / 3 / 18H - 1FH
PSW.5	F0	User flag which may be set to "0" or "1" as desired by the user.
PSW.6	AC	Auxiliary carry flag. This flag is set to "1" if a carry C_3 is generated from bit 3 of the ALU as a result of executing an arithmetic operation instruction. In all other cases, the flag is reset to "0".
PSW.7	CY	Main carry flag. This flag is set to "1" if a carry C_7 is generated from bit 7 of the ALU as result of executing an arithmetic operation instruction. If a carry C_7 is not generated, the flag is reset to "0".

I/O CONTROL REGISTER (IOCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IOCON	0F8H	WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

BIT LOCATION	FLAG	FUNCTION
IOCON.0	ALF	If CPU power down mode (PD, HPD) is activated with this bit set to "1", the outputs from ports 0, 1, 2 and 3 are switched to floating status. When this bit is "0", ports 0, 1, 2 and 3 are in output mode.
IOCON.1	P1HZ	Port 1 becomes a floating state input port when this bit is "1".
IOCON.2	P2HZ	Port 2 becomes a floating state input port when this bit is "1".
IOCON.3	P3HZ	Port 3 becomes a floating state input port when this bit is "1".
IOCON.4	IZC	The 10 kohm pull-up resistance for ports 1, 2 and 3 is switched off when this bit is "1", leaving only the 100 kohm pull-up resistance.
IOCON.5	SERR	Serial port reception error flag. This flag is set to "1" if an overrun or framing error is generated when data is received at a serial port. The flag is reset by software.
IOCON.6	T32	Timer/counters 0 and 1 are connected serially to from a 32-bit timer/counter when this bit is set to "1". TF1 of TCON is set if a carry is generated in the 32-bit timer/counter.
IOCON.7	WDT	Watchdog timer mode is set when this bit is set to "1". And if TF1 is set to "1" after watchdog timer mode has been set, the CPU is reset and the program is executed from address 0.

TIMER 2 CONTROL REGISTER (T2CON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
T2CON	0C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

BIT LOCATION	FLAG	FUNCTION
T2CON.0	CP/$\overline{RL2}$	Capture mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "1". 16-bit auto reload mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "0". CP/$\overline{RL2}$ is ignored when TCLK + RCLK = "1".
T2CON.1	C/$\overline{T2}$	Timer/counter 2 count clock designation control bit. The internal clocks (XTAL1-2 ÷ 12, XTAL1-2 ÷ 2) are used when this bit is "0", and the external clock applied to the T2 is passed to timer/counter 2 when the bit is "1".
T2CON.2	TR2	Timer/counter 2 counting start and stop control bit. Timer/counter 2 commences counting when this bit is "1" and stops counting when "0".
T2CON.3	EXEN2	T2EX timer/counter 2 external control signal control bit. Input of the T2EX signal is disabled when this bit is "0", and enabled when "1".
T2CON.4	TCLK	Serial port transmit circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port transmit clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.
T2CON.5	RCLK	Serial port receive circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port receive clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.
T2CON.6	EXF2	Timer/counter 2 external flag. This bit is set to "1" when the T2EX timer/counter 2 external control signal level is changed from "1" to "0" while EXEN2 = "1". This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, EXF2 must be reset to "0" by software.
T2CON.7	TF2	Timer/counter 2 carry flag. This bit is set to "1" by a carry signal when timer/counter 2 is in 16-bit auto reload mode or in capture mode. This flag serves as the timer interrupt 2 request signal. if an interrupt is generated, TF2 must be reset to "0" by software.

LIST OF INSTRUCTIONS

LIST OF INSTRUCTION SYMBOLS

A	: Accumulator
AB	: Register pair
AC	: Auxiliary carry flag
B	: Arithmetic operation register
C	: Carry flag
DPTR	: Data pointer
PC	: Program counter
Rr	: Register indicator (r = 0 ~ 7)
SP	: Stack pointer
AND	: Logical product
OR	: Logical sum
XOR	: Exclusive OR
+	: Addition
–	: Substraction
x	: Multiplication
/	: Division
(x)	: Denotes the contents of x
((x))	: Denotes the contents of address determined by the contents of x
#	: Denotes the immediate data
@	: Denotes the indirect address
=	: Equality
≠	: Non equality
←	: Substitution
→	: Substitution
–	: Negation
<	: Smaller than
>	: Larger than
bit address	: RAM and the special function register bit specifier address (b_0 ~ b_7)
code address	: Absolute address (A_0 ~ A_1)
data	: immediate data (I_0 ~ I_7)
relative offset	: Relative jump address offset value (R_0 ~ R_7)
direct address	: RAM and the special function register byte specifier address (a_0 ~ a_7)

INSTRUCTION TABLE

L / H	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	NOP	AJMP address 11 (Page 0)	LJMP address 16	RR A	INC A	INC direct	INC @ RO	INC @ R1
1 0001	JBC bit, rel	ACALL address 11 (Page 0)	LCALL address 16	RRC A	DEC A	DEC direct	DEC @ RO	DEC @ R1
2 0010	JB bit, rel	AJMP address 11 (Page 1)	RET	RL A	ADD A, # data	ADD A, direct	ADD A, @ R0	ADD A, @ R1
3 0011	JNB bit, rel	ACALL adress 11 (Page 1)	RETI	RLC A	ADDC A, # data	ADDC A, direct	ADDC A, @ R0	ADDC A, @ R1
4 0100	JC bit, rel	AJMP address 11 (Page 2)	ORL direct, A	ORL direct, # data	ORL A, # data	ORL A, direct	ORL A, @ R0	ORL A, @ R1
5 0101	JNC rel	ACALL address 11 (Page 2)	ANL direct, A	ANL direct # data	ANL A, # data	ANL A, direct	ANL A, @ R0	ANL A, @ R1
6 0110	JZ rel	AJMP address 11 (Page 3)	XRL direct, A	XRL direct # data	XRL A, # data	XRL A, direct	XRL A, @ R0	XRL A, @ R1
7 0111	JNZ rel	ACALL address 11 (Page 3)	ORL C, bit	JMP @ A + DPTR	MOV A, # data	MOV direct, # data	MOV @ R0, # data	MOV @ R1, # data
8 1000	SJMP rel	AJMP address 11 (Page 4)	ANL C, bit	MOVC A, @ A + PC	DIV AB	MOV direct 1, direct 2	MOV direct, @ R0	MOV direct, @ R1
9 1001	MOV DPTR # data 16	ACALL address 11 (Page 4)	MOV bit, C	MOVC A, @ A + DPTR	SUBB A, # data	SUBB A, direct	SUBB A, @ R0	SUBB A, @ R1
A 1010	ORAL C, bit	AJMP address 11 (Page 5)	MOV C, bit	INC DPTR	MUL AB		MOV @ R0, direct	MOV @ R1, direct
B 1011	ANL C bit,	ACALL address 11 (Page 5)	CPL bit	CPL C	CJNE A, # data, rel	CJNE A, direct, rel	CJNE @ R0, # data, rel	CJNE @ R1, # data, rel
C 1100	PUSH direct	AJMP address 11 (Page 6)	CLR bit	CLR C	SWAP A	XCH A, direct	XCH A, @ R0	XCH A, @ R1
D 1101	POP direct	ACALL address 11 (Page 6)	SETB bit	SETB C	DA A	DJNZ direct, rel	XCHD A, @ R0	XCH A, @ R1
E 1110	MOVX A, @ DPTR	AJMP address 11 (Page 7)	MOVX A, @ R0	MOVX A, @ R1	CLR A	MOV A, direct	MOV A, @ R0	MOV A, @ R1
F 1111	MOVX @ DPTR, A	ACALL address 11 (Page 7)	MOVX @ R0, A	MOVX @ R1, A	CPL A	MOV direct, A	MOV @ R0, A	MOV @ R1, A

2 BYTE		3 BYTE
2 CYCLE	MNEMONIC	4 CYCLE

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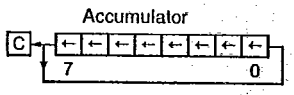
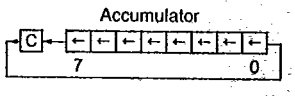
L / H	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111
0 0000	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
1 0001	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
2 0010	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
3 0011	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
4 0100	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5 0101	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6 0110	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
7 0111	MOV R0, # data	MOV R1, # data	MOV R2, # data	MOV R3, # data	MOV R4, # data	MOV R5, # data	MOV R6, # data	MOV R7, # data
8 1000	MOV direct, R0	MOV direct, R1	MOV direct, R2	MOV direct, R3	MOV direct, R4	MOV direct, R5	MOV direct, R6	MOV direct, R7
9 1001	SUBB A, R0	SUBB A, R1	SUBB A, R2	SUBB A, R3	SUBB A, R4	SUBB A, R5	SUBB A, R6	SUBB A, R7
A 1010	MOV R0, direct	MOV R1, direct	MOV R2, direct	MOV R3, direct	MOV R4, direct	MOV R5, direct	MOV R6, direct	MOV R7, direct
B 1011	CJNE R0, # data rel	CJNE R1, # data rel	CJNE R2, # data rel	CJNE R3, # data rel	CJNE R4, # data rel	CJNE R5, # data rel	CJNE R6, # data rel	CJNE R7, # data rel
C 1100	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
D 1101	DJNZ R0, rel	DJNZ R1, rel	DJNZ R2, rel	DJNZ R3, rel	DJNZ R4, rel	DJNZ R5, rel	DJNZ R6, rel	DJNZ R7, rel
E 1110	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7
F 1111	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A

INSTRUCTION SET DETAILS

MNEMONIC	INSTRUCTION CODE D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	BYTES	CYCLES	DESCRIPTION
ARITHMETIC OPERATION INSTRUCTIONS				
ADD A,Rr	0 0 1 0 1 r_2 r_1 r_0	1	1	(AC), (0V), (C), (A) ← (A) + (Rr)
ADD A, direct	0 0 1 0 0 1 0 1	2	1	(AC), (0V), (C), (A) ← (A) + (direct address)
ADD A, @Rr	0 0 1 0 0 1 1 r_0	1	1	(AC), (0V), (C), (A) ← (A) + ((Rr))
ADD A, #data	0 0 1 0 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(AC), (0V), (C), (A) ← (A) + #data
ADDC A, Rr	0 0 1 1 1 r_2 r_1 r_0	1	1	(AC), (0V), (C), (A) ← (A) + (C) + (Rr)
ADDC A, direct	0 0 1 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(AC), (0V), (C), (A) ← (A) + (C) + (direct address)
ADDC A, @Rr	0 0 1 1 0 1 1 r_0	1	1	(AC), (0V), (C), (A) ← (A) + (C) + ((Rr))
ADDC A, #data	0 0 1 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(AC), (0V), (C), (A) ← (A) + (C) + #data
SUBB A, Rr	1 0 0 1 1 r_2 r_1 r_0	1	1	(AC), (0V), (C), (A) ← (A) – (C) – (Rr)
SUBB A, direct	1 0 0 1 0 1 0 1	2	1	(AC), (0V), (C), (A) ← (A) – (C) – (direct address)
SUBB A, @Rr	1 0 0 1 0 1 1 r_0	1	1	(AC), (0V), (C), (A) ← (A) – (C) – ((Rr))
SUBB A, #data	1 0 0 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(AC), (0V), (C), (A) ← (A) – (C) – #data)
MUL AB	1 0 1 0 0 1 0 0	1	4	(AC) ← (A) x (B)
DIV AB	1 0 0 0 0 1 0 0	1	4	(A) quotient (B) remainder ← (A)/B
DA A	1 1 0 1 0 1 0 0	1	1	When the contents of accumulator bits 0 thru 3 are greater than 3, or when auxiliary carry (AC) is 1, 6 added to bits 0 thru 3. Bits 4 thru 7 are then examined and when bits 4 thru 7 following compensation of lower bits 0 thru 3 is greater than 9, or when carry (C) is 1, 6 added to bits 4 thru 7. As a result, the carry flag can be set, but cannot be cleared.
ACCUMULATOR OPERATION INSTRUCTIONS				
CLR A	1 1 1 0 0 1 0 0	1	1	(A) ← 0
CPL A	1 1 1 1 0 1 0 0	1	1	(A) ← $\overline{(A)}$
RL A	0 0 1 0 0 0 1 1	1	1	
RLC A	0 0 1 1 0 0 1 1	1	1	

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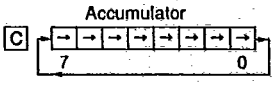
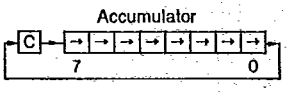
INSTRUCTION SET DETAILS (CONT.)

MNEMONIC		INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	DESCRIPTION
RR	A	0	0	0	0	0	0	1	1	1	1	
RRC	A	0	0	0	1	0	0	1	1	1	1	
SWAP	A	1	1	0	0	0	1	0	0	1	1	$(A_{3-0}) \leftarrow (A_{7-4})$
INCREMENT/DECREMENT												
INC	A	0	0	0	0	0	1	0	0	1	1	(A) ← (A) + 1
INC	Rr	0	0	0	0	1	r_2	r_1	r_0	1	1	(Rr) ← (Rr) + 1
INC	direct	0	0	0	0	0	1	0	1	2	1	(direct address) ← (direct address) + 1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
INC	@Rr	0	0	0	0	0	1	1	r_0	1	1	((Rr)) ← ((Rr)) + 1
INC	DPTR	1	0	1	0	0	0	1	1	1	2	(DPTR) ← (DPTR) + 1
DEC	A	0	0	0	1	0	1	0	0	1	1	(A) ← (A) – 1
DEC	Rr	0	0	0	1	1	r_2	r_1	r_0	1	1	(Rr) ← (Rr) – 1
DEC	direct	0	0	0	1	0	1	0	1	2	1	(direct address) ← (direct address) – 1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
DEC	@Rr	0	0	0	1	0	1	1	r_0	1	1	((Rr)) ← ((Rr)) – 1
LOGICAL OPERATION INSTRUCTIONS												
ANL	A, Rr	0	1	0	1	1	r_2	r_1	r_0	1	1	(A) ← (A) AND (Rr)
ANL	A, direct	0	1	0	1	0	1	0	1	2	1	(A) ← (A) AND (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
ANL	A, @Rr	0	1	0	1	0	1	1	r_0	1	1	(A) ← (A) AND (Rr)
ANL	A,#data	0	1	0	1	0	1	0	0	2	1	(A) ← (A) AND #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
ANL	direct, A	0	1	0	1	0	0	1	0	2	1	(direct address) ← (direct address) AND (A)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
ANL	direct, #data	0	1	0	1	0	0	1	1	3	2	(direct address) ← (direct address) AND #data
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
ORL	A, Rr	0	1	0	0	1	r_2	r_1	r_0	1	1	(A) ← (A) OR (Rr)
ORL	A, direct	0	1	0	0	0	1	0	1	2	1	(A) ← (A) OR (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
ORL	A, @Rr	0	1	0	0	0	1	1	r_0	1	1	(A) ← (A) OR ((Rr))
ORL	A, #data	0	1	0	0	0	1	0	0	2	1	(A) ← (A) OR #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			

INSTRUCTION SET DETAILS (CONT.)

MNEMONIC		INSTRUCTION CODE D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	BYTES	CYCLES	DESCRIPTION
ORL	direct, A	0 1 0 0 0 0 1 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address) OR (A)
ORL	direct, #data	0 1 0 0 0 0 1 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← (direct address OR #data
XRL	A, Rr	0 1 1 0 1 r_2 r_1 r_0	1	1	(A) ← (A) XOR (Rr)
XRL	A, direct	0 1 1 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ← (A) XOR (direct address)
XRL	A, @Rr	0 1 1 0 0 1 1 r_0	1	1	(A) ← (A) XOR ((Rr))
XRL	A, #data	0 1 1 0 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(A) ← XOR #data
XRL	direct, A	0 1 1 0 0 0 1 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address) XOR (A)
XRL	direct, #data	0 1 1 0 0 0 1 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← (direct address) XOR #data
IMMEDIATE DATA SETTING INSTRUCTIONS					
MOV	A, #data	0 1 1 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(A) ← #data
MOV	Rr, #data	0 1 1 1 1 r_2 r_1 r_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(Rr) ← #data
MOV	direct, ← data	0 1 1 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← #data
MOV	@Rr, #data	0 1 1 1 0 1 1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(Rr) ← #data
MOV	DPTR, #data 16	1 0 0 1 0 0 0 0 I_{15} I_{14} I_{13} I_{12} I_{11} I_{10} I_9 I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(DPTR) ← #data 16
CARRY FLAG OPERATION INSTRUCTIONS					
CLR	C	1 1 0 0 0 0 1 1	1	1	(C) ← 0
SETB	C	1 1 0 1 0 0 1 1	1	1	(C) ← 1
CPL	C	1 0 1 1 0 0 1 1	1	1	(C) ← $\overline{(C)}$
ANL	C, bit	1 0 0 0 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) AND (bit address)
ANL	C,/bit	1 0 1 1 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) AND $\overline{\text{(bit address)}}$
ORL	C, bit	0 1 1 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) OR (bit address)
ORL	C,/bit	1 0 1 0 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) OR $\overline{\text{(bit address)}}$
MOV	C, bit	1 0 1 0 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(C) ← (bit address)
MOV	bit, C	1 0 0 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(bit address) ← (C)

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INSTRUCTION SET DETAILS (CONT.)

MNEMONIC	INSTRUCTION CODE D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	BYTES	CYCLES	DESCRIPTION
BIT OPERATION INSTRUCTIONS				
SETB bit	1 1 0 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(bit address) ← 1
CLR bit	1 1 0 0 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(bit address) ← 0
CPL bit	1 0 1 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(bit address) ← ($\overline{\text{bit address}}$)
DATA TRANSFER INSTRUCTIONS				
MOV A, Rr	1 1 1 0 1 r_2 r_1 r_0	1	1	(A) ← (Rr)
MOV A, direct	1 1 1 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ← (direct address)
MOV A, @Rr	1 1 1 0 0 1 1 r_0	1	1	(A) ← ((Rr))
MOV Rr, A	1 1 1 1 1 r_2 r_1 r_0	1	1	(Rr) ← (A)
MOV Rr, direct	1 0 1 0 1 r_2 r_1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(Rr) ← (direct address)
MOV direct, A	1 1 1 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (A)
MOV direct, Rr	1 0 0 0 1 r_2 r_1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(direct address) ← (Rr)
MOV direct 1, direct 2	1 0 0 0 0 1 0 1 a^2_7 a^2_6 a^2_5 a^2_4 a^2_3 a^2_2 a^2_1 a^2_0 a^1_7 a^1_6 a^1_5 a^1_4 a^1_3 a^1_2 a^1_1 a^1_0	3	2	(direct address 1) ← (direct address 2)
MOV direct, @Rr	1 0 0 0 0 1 1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(direct address) ← ((Rr))
MOV @Rr, A	1 1 1 1 0 1 1 r_0	1	1	((Rr)) ← (A)
MOV @Rr, direct	1 0 1 0 0 1 1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	((Rr)) ← (direct address))
CONSTANT CODE INSTRUCTIONS				
MOVC A, @A + DPTR	1 0 0 1 0 0 1 1	1	2	(A) ← ((A) + (DPTR))
MOVC A, @A + PC	1 0 0 0 0 0 1 1	1	2	(PC) ← (PC) + 1 (A) ← ((A) + (PC))
DATA EXCHANGE INSTRUCTIONS				
XCH A, Rr	1 1 0 0 1 r_2 r_1 r_0	1	1	(A) (Rr)
XCH A, direct	1 1 0 0 0 1 0 1 a_7 a_8 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) (direct address)
XCH A, @Rr	1 1 0 0 0 1 1 r_0	1	1	(A) ((Rr))
XCHD A, @Rr	1 1 0 1 0 1 1 r_0	1	1	($A_{0 \sim 3}$) ($(Rr_{0 \sim 3})$)

INSTRUCTION SET DETAILS (CONT.)

MNEMONIC	INSTRUCTION CODE D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	BYTES	CYCLES	DESCRIPTION
SUBROUTINE INSTRUCTIONS				
PUSH direct	1 1 0 0 0 0 0 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(SP) ← (SP) + 1 ((SP)) ← (direct address)
POP direct	1 1 0 1 0 0 0 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(direct address) ← ((SP)) (SP) ← (SP) – 1
ACALL addr 11	A_{10} A_9 A_8 1 0 0 0 1 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	2	2	(PC) ← (PC) + 2 (SP) ← (SP) + 1 ((SP)) ← ($PC_{0 \sim 7}$) (SP) ← (SP) + 1 ((SP)) ← ($PC_{8 \sim 15}$) ($PC_{0 \sim 10}$) ← $A_{0 \sim 10}$
LCALL addr 16	0 0 0 1 0 0 1 0 A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	3	2	(PC) ← (PC) + 3 (SP) ← (SP) + 1 ((SP)) ← ($PC_{0 \sim 7}$) (SP) ← (SP) + 1 ((SP)) ← ($PC_{8 \sim 15}$) ($PC_{0 \sim 15}$) ← $A_{0 \sim 15}$
RET	0 0 1 0 0 0 1 0	1	2	($PC_{8 \sim 15}$) ← ((SP)) (SP) ← (SP) – 1 ($PC_{0 \sim 7}$) ← ((SP)) (SP) ← (SP) – 1
RETI	0 0 1 1 0 0 1 0	1	2	($PC_{8 \sim 15}$) ← ((SP)) (SP) ← (SP) – 1 ($PC_{0 \sim 7}$) ← ((SP)) (SP) ← (SP) – 1
JUMP INSTRUCTIONS				
AJMP addr 11	A_{10} A_9 A_8 0 0 0 0 1 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	2	2	(PC) ← (PC) + 2 ($PC_{0 \sim 10}$) ← $A_{0 \sim 10}$
LJMP addr 16	0 0 0 0 0 0 1 0 A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	3	2	($PC_{0 \sim 15}$) ← $A_{0 \sim 15}$
SJMP rel	1 0 0 0 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC) + 2 (PC) ← (PC) + relative offset
JMP @A + DPTR	0 1 1 1 0 0 1 1	1	2	(PC) ← (A) + (DPTR)
BRANCH INSTRUCTIONS				

CJNE A, direct, rel	1 0 1 1 0 1 0 1
	a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0
	R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
		3	2	(PC) ← (PC) + 3
				IF (A) ≠ (direct address)
				THEN
				(PC) ← (PC) + relative offset
				IF (A) < (direct address)
				THEN
				(C) ← 1
				ELSE
				(C) ← 0

CJNE A, #data, rel	1 0 1 1 0 1 0 0
	I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0
	R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
		3	2	(PC) ← (PC) + 3
				IF (A) ≠ #data
				THEN
				(PC) ← (PC) + relative offset
				IF (A) < #data
				THEN
				(C) ← 1
				ELSE
				(C) ← 0

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INSTRUCTION SET DETAILS (CONT.)

MNEMONIC		INSTRUCTION CODE D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	BYTES	CYCLES	DESCRIPTION

CJNE	Rr, #data, rel	1 0 1 1 1 r_2 r_1 r_0
		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0
		R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
			3	2	(PC) ← (PC) + 3
					IF ((Rr)) ≠ #data
					THEN
					(PC) ← (PC) + relative offset
					IF ((Rr)) < #data
					THEN
					(C) ← 1
					ELSE
					(C) ← 0

CJNE	@Rr, #data, rel	1 0 1 1 0 1 1 r_0
		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0
		R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
			3	2	(PC) ← (PC) + 3
					IF ((Rr)) ≠ #data
					THEN
					(PC) ← (PC) + relative offset
					IF ((Rr)) < #data
					THEN
					(C) ← 1
					ELSE
					(C) ← 0

DJNZ	Rr, rel	1 1 0 1 1 r_2 r_1 r_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC) + 2 (Rr) ← (Rr) – 1 IF (Rr) > 0 or (Rr) < 0 THEN (PC) ← (PC) + relative offset
DJNZ	direct, rel	1 1 0 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC) + 3 (direct address) ← (direct address) – 1 IF (direct address) ≠ 0 THEN (PC) ← (PC) + relative offset
JZ	rel	0 1 1 0 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC) + 2 IF (A) ≠ 0 THEN (PC) ← (PC) + relative offset
JNZ	rel	0 1 1 1 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC) + 2 IF (A) ≠ 0 THEN (PC) ← (PC) + relative offset
JC	rel	0 1 0 0 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC) + 2 IF (C) = 1 THEN (PC) ← (PC) + relative offset
JNC	rel	0 1 0 1 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC) + 2 IF (C) = 0 THEN (PC) ← (PC) + relative offset
JB	bit, rel	0 0 1 0 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC) + 3 IF (bit address) = 1 THEN (PC) ← (PC) + relative offset
JNB	bit, rel	0 0 1 1 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC) + 3 IF (bit address) = 0 THEN (PC) ← (PC) + relative offset
JBC	bit, rel	0 0 0 1 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC) + 3 IF (bit address) = 1 THEN (bit address) ← 0 (PC) ← (PC) + relative offset

INSTRUCTION SET DETAILS (CONT.)

MNEMONIC	INSTRUCTION CODE								BYTES	CYCLES	DESCRIPTION
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
EXTERNAL MEMORY INSTRUCTIONS											
MOVX A, @Rr	1	1	1	0	0	0	1	r_0	1	2	(A) ← ((Rr)) EXTERNAL RAM
MOVX A, @DPTR	1	1	1	0	0	0	0	0	1	2	(A) ← ((DPTR)) EXTERNAL RAM
MOVX @Rr, A	1	1	1	1	0	0	1	r_0	1	2	(Rr) ← (A) EXTERNAL RAM
MOVX @DPTR, A	1	1	1	1	0	0	0	0	1	2	((DPTR)) ← (A) EXTERNAL RAM
OTHER INSTRUCTIONS											
NOP	0	0	0	0	0	0	0	0	1	1	(PC) ← (PC) + 1

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias :
C = commercial ..... 0°C to 70°C
I = industrial ..... – 40°C to + 85°C
Storage Temperature ..... – 65°C to + 150°C
Voltage on V_{CC} to V_{SS} ..... – 0.5 V to + 7 V
Voltage on Any Pin to V_{SS} ..... – 0.5 V to V_{CC} + 0.5 V
Power Dissipation ..... 200 mW

**NOTICE : Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*

DC CHARACTERISTICS

(T_A = – 40°C to 85°C ; VCC = 5 V ± 10 % ; VSS = 0 V ; F = 0 to 16 MHz)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 VCC – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 0.9	VCC + 0.5	V	
VIH1	Input High Voltage (RST and XTAL1)	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6 mA (note 3)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 3.2 mA (note 3)
VOH	Output High Voltage Ports 1, 2, 3	0.9 VCC		V	IOH = – 10 µA
		0.75 VCC		V	IOH = 25 µA
		2.4		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH2	Output High Voltage Port 1, 2, 3 IZC = 1	0.75 VCC		V	IOH = – 2.5 µA
VOH1	Output High Voltage (Port 0 (Port 0, ALE, $\overline{PSEN}$)	0.9 VCC		V	IOH = – 80 µA
		0.75 VCC		V	IOH = – 300 µA
		2.4		V	IOH = – 800 µA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current Ports 1, 2, 3		C – 50	µA	Vin = 0.45 V
			I – 60		
ILI	Input Leakage Current (Port 0, EA)		± 10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650	µA	Vin = 2.0 V
IPD	Power Supply Current (Power Down Mode)		50	µA	VCC = 2.0 V to 5.5 V (note 2)
RRST	RST Pulldown Resistor	50	150	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	f_C = 1 MHz, T_A = 25°C
ICC	Power supply current Active mode 16 MHz Idle mode 16 MHz		32 9	mA mA	(notes 1, 2)

Note 1 :

ICC max is given by :
Active mode : ICCMAX = 2 x FREQ + 4
Idle Mode : ICCMAX = 0.5 x FREQ + 2

where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See *figure 1.*
See *figures 2 through 5* for ICC test conditions.

DC CHARACTERISTICS (AUTOMOTIVE)

(T_A = – 40°C to + 125°C ; VCC = 5 V ± 10 % ; VSS = 0 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 VCC – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 0.9	VCC + 0.5	V	
VIH1	Input High Voltage (RST and XTAL1)	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6 mA (note 3)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 3.2 mA (note 3)
VOH	Output High Voltage Ports 1, 2, 3	0.9 VCC		V	IOH = – 10 µA
		0.75 VCC		V	IOH = 25 µA
		2.4		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0 (Port 0, ALE, $\overline{PSEN}$)	0.9 VCC		V	IOH = – 80 µA
		0.75 VCC		V	IOH = – 300 µA
		2.4		V	IOH = – 800 µA VCC = 5 V ± 10 %
VOH2	Output High Voltage Port 1, 2, 3 IZC = 1	0.75 VCC		V	IOH = – 2.5 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		– 75	µA	Vin = 0.45 V
ILI	Input Leakage Current (Port 0, EA)		± 10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 750	µA	Vin = 2.0 V
IPD	Power Supply Current (Power Down Mode)		75	µA	VCC = 2.0 V to 5.5 V (note 2)
RRST	RST Pulldown Resistor	50	150	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	f_C = 1 MHz, T_A = 25°C
ICC	Power supply current Active mode 12 MHz Idle mode 12 MHz		28 8	mA mA	(notes 1, 2)

Note 2 :

ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC – .5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator is used. Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC – .5 V ; XTAL2 N.C. ; Port 0 = VCC ; EA = RST = VSS.
Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 3 :

Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V with maxi VOL peak 0.6 V.A Schmitt Trigger use is not necessary.

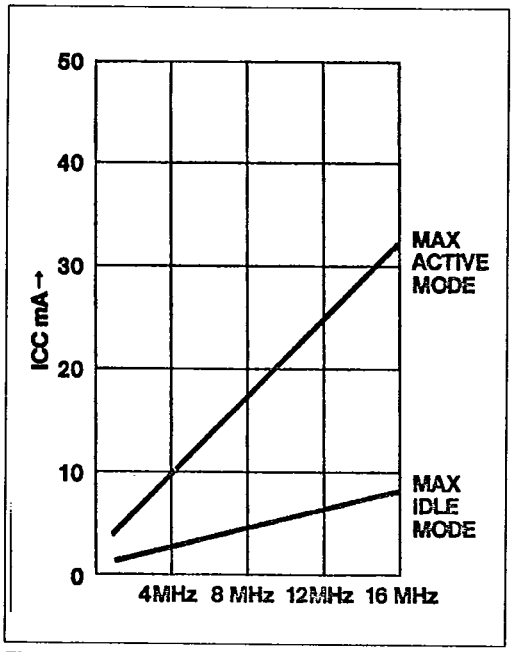

Figure 1 : ICC vs. Frequency. Valid only within frequency specifications of the device under test.

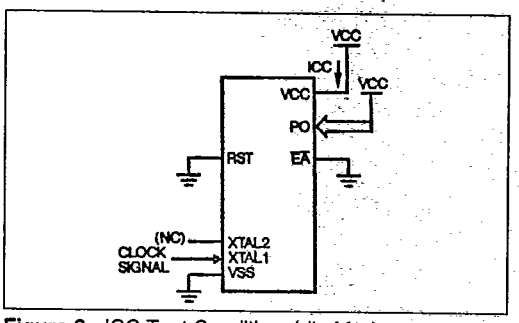

Figure 2 : ICC Test Condition, Idle Mode. All other pins are disconnected.

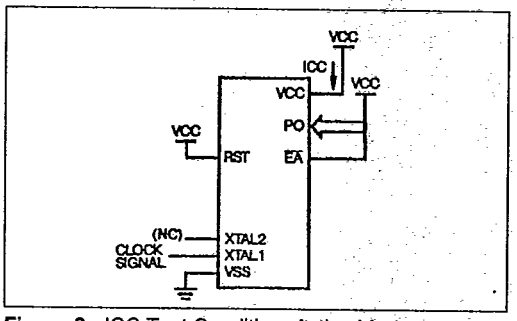

Figure 3 : ICC Test Condition, Active Mode. All other pins are disconnected.

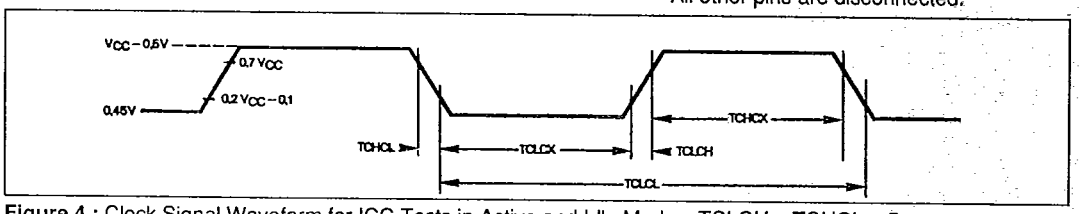

Figure 4 : Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

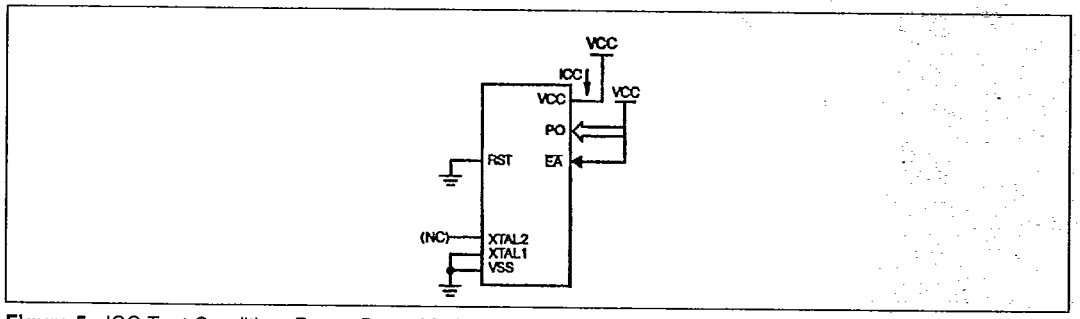

Figure 5 : ICC Test Condition, Power Down Mode. All other pins are disconnected.

EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL1)

SYMBOL	PARAMETER	VARIABLE CLOCK FREQ = 0 to 16 MHz		UNIT
		MIN	MAX	
1/TCLCL	Oscillator Frequency	62.5		ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

*83C154-1/80C154-1 versions only.

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

A.C. PARAMETERS :

TA = 0°C + 70°C ; Vss = 0 V ; Vcc = 5 V ± 10 % (commercial).

TA = – 40°C + 85°C ; Vss = 0 V ; Vcc = 5 V ± 10 % (industrial).

(Load Capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pf ; Load Capacitance for All Other Outputs = 80 pf).

SYMBOL	PARAMETER	MIN	MAX	UNIT
TLHLL	ALE Pulse Width	2TCLCL-40		ns
TAVLL	Address Valid to ALE	TCLCL-40		ns
TLLAX	Address Hold After ALE	TCLCL-35		ns
TLLIV	ALE to Valid Instr in		4TCLCL-100	ns
TLLPL	ALE to $\overline{PSEN}$	TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ to Valid Instr in		3TCLCL-105	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		TCLCL-15	ns
TPXAV	$\overline{PSEN}$ to Address Valid	TCLCL-8		ns
TAVIV	Address to Valid Instr in		5TCLCL-105	ns
TPAZ	$\overline{PSEN}$ Low to Address Float		10	ns
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL-100		ns
TLLAX	Data Address Hold After ALE	TCLCL-35		ns
TRLDV	$\overline{RD}$ to Valid Data in		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL-70	ns
TLLDV	ALE to Valid Data in		8TCLCL-150	ns
TAVDV	Address to Valid Data in		9TCLCL-165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL-60		ns
TQVWH	Data Setup to $\overline{WR}$ High	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL-50		ns
TRLAZ	RD Low to Address Float		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	TCLCL-40	TCLCL+40	ns

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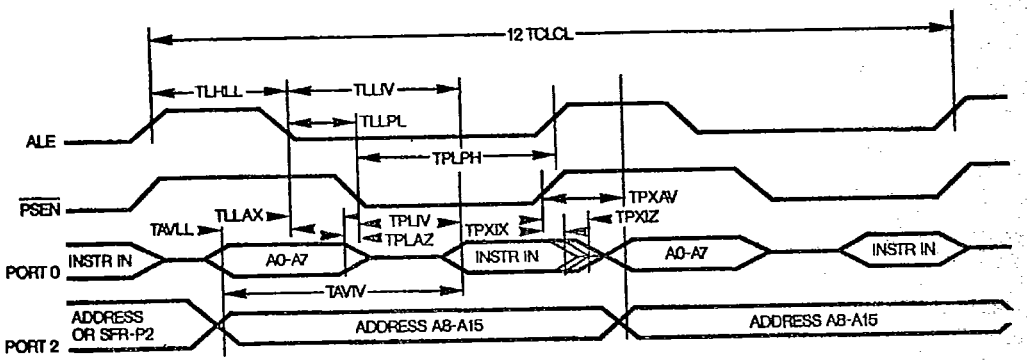
AC PARAMETERS :

TA = – 40°C to + 125°C ; V_{SS} = 0 V ; V_{CC} = 5 V ± 10 % (Automotive)

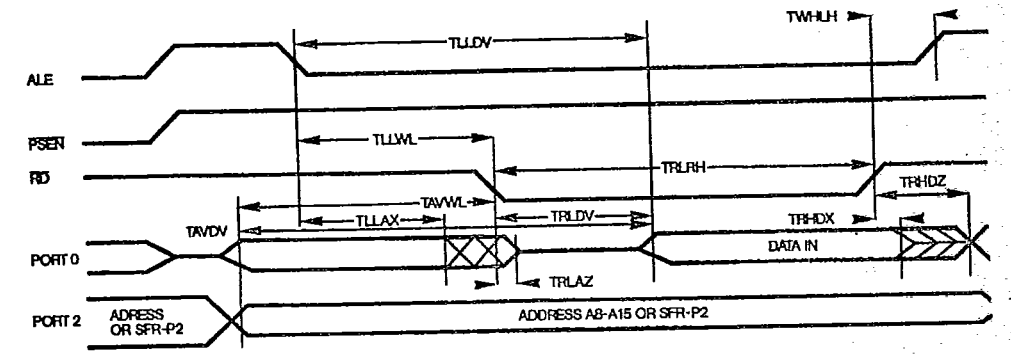
SYMBOL	PARAMETER	MIN	MAX	UNIT
TLHLL	ALE Pulse Width	2TCLCL-55		ns
TAVLL	Address Valid to ALE	TCLCL-70		ns
TLLAX	Address Hold After ALE	TCLCL-35		ns
TLLIV	ALE to Valid Instr in		4TCLCL-115	ns
TLLPL	ALE to $\overline{PSEN}$	TCLCL-55		ns
TPLPH	$\overline{PSEN}$ Pulse Width	3TCLCL-60		ns
TPLIV	$\overline{PSEN}$ to Valid Instr in		3TCLCL-120	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		TCLCL-40	ns
TPXAV	$\overline{PSEN}$ to Address Valid	TCLCL-8		ns
TAVIV	Address to Valid Instr in		5TCLCL-120	ns
TPAZ	$\overline{PSEN}$ Low to Address Float		25	ns
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL-100		ns
TLLAX	Data Address Hold After ALE	TCLCL-50		ns
TRLDV	$\overline{RD}$ to Valid Data in		5TCLCL-185	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL-85	ns
TLLDV	ALE to Valid Data in		8TCLCL-170	ns
TAVDV	Address to Valid Data in		9TCLCL-185	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL-65	3TCLCL+65	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL-145		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL-75		ns
TQVWH	Data Setup to $\overline{WR}$ High	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL-65		ns
TRLAZ	RD Low to Address Float		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	TCLCL-65	TCLCL+65	ns

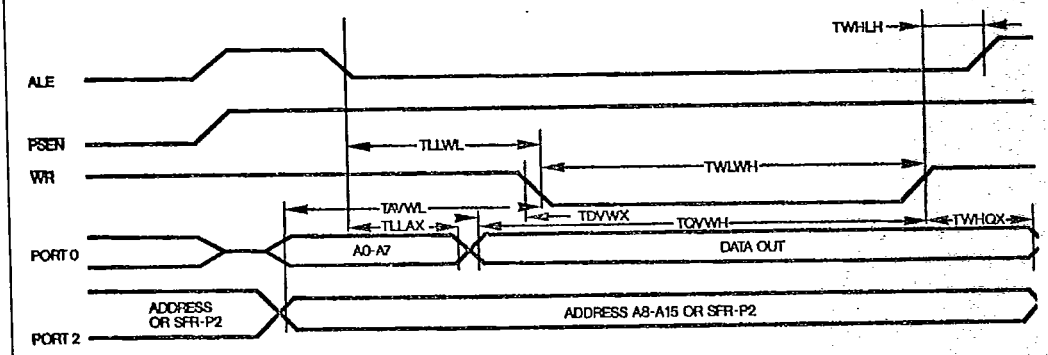
AC TIMING DIAGRAMS

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE





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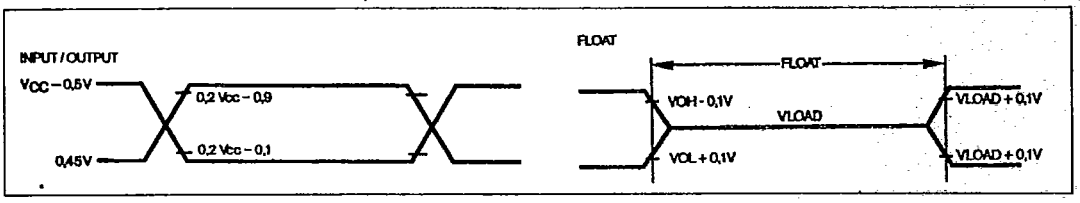
AC TESTING INPUT/OUTPUT, FLOAT WAVEFORMS

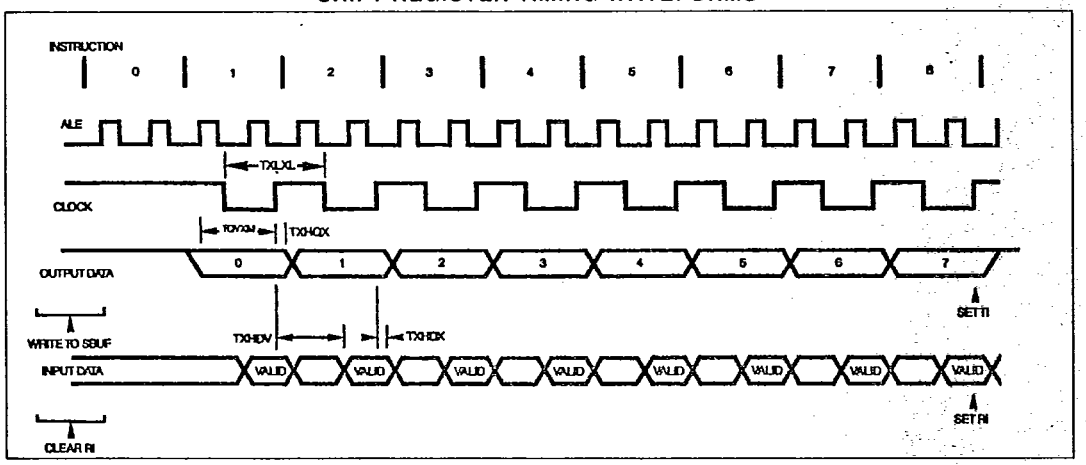


AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0". For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 mA.

SERIAL PORT TIMING - SHIFT REGISTER MODE

SYMBOL	PARAMETER	MIN	MAX	UNIT
TXLXL	Serial Port Clock Cycle Time	12TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL-133		ns
TXHQX	Output Data Hold after Clock Rising Edge	2TCLCL-117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		10TLCL-133	ns

SHIFT REGISTER TIMING WAVEFORMS



EXPLANATION OF THE AC SYMBOLS

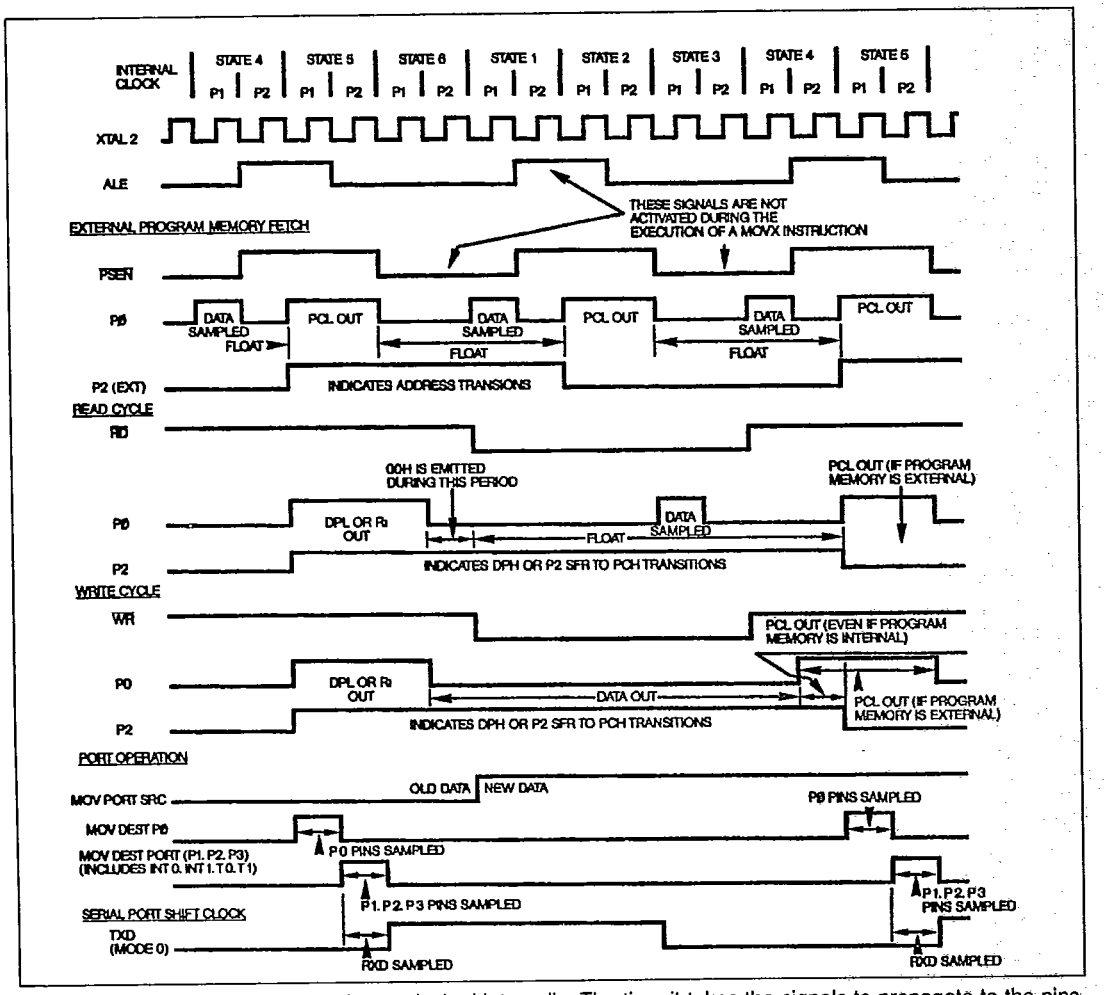
Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL = Time for Address Valid to ALE low.
TLLPL = Time for ALE low to PSEN low.

A : Address.
C : Clock.
D : Input data.
H : Logic level HIGH.
I : Instruction (program memory contents).
L : Logic level LOW, or ALE.
P : PSEN.
Q : Output data.
R : READ signal.
T : Time.
V : Valid.
W : WRITE signal.
X : No longer a valid logic level.
Z : Float.

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

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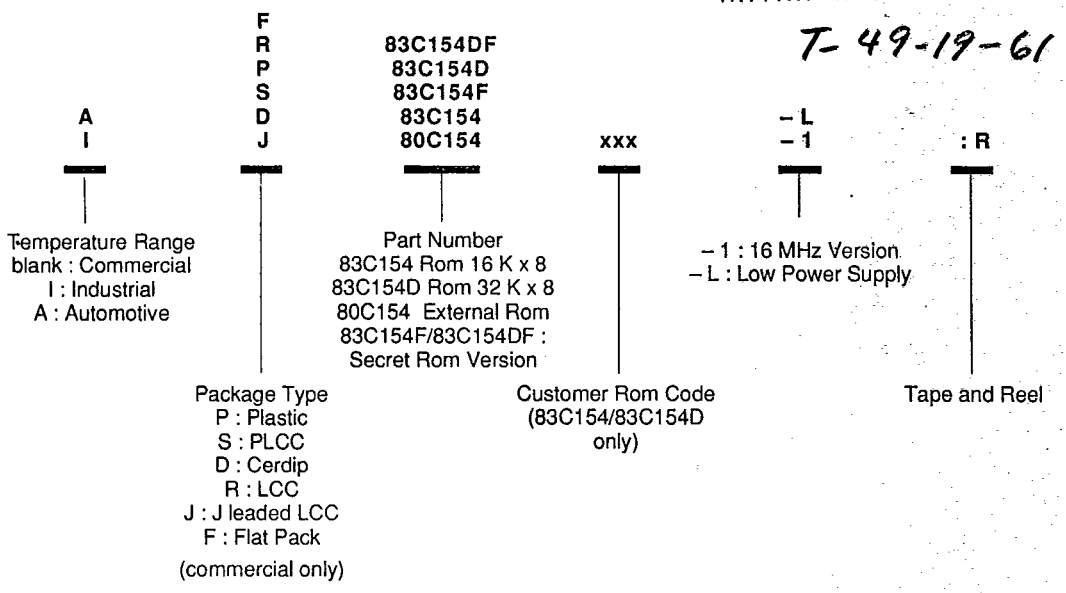
A
I
F
R
P
S
D
J
83C154DF
83C154D
83C154F
83C154
80C154
xxx
– L
– 1
: R
Temperature Range
blank : Commercial
I : Industrial
A : Automotive
Package Type
P : Plastic
S : PLCC
D : Cerdip
R : LCC
J : J leaded LCC
F : Flat Pack
(commercial only)
Part Number
83C154 Rom 16 K x 8
83C154D Rom 32 K x 8
80C154 External Rom
83C154F/83C154DF :
Secret Rom Version
Customer Rom Code
(83C154/83C154D
only)
– 1 : 16 MHz Version
– L : Low Power Supply
Tape and Reel