Am27S15

4096-Bit (512 x 8) Bipolar PROM
with Output Data Latches

DISTINCTIVE CHARACTERISTICS

- On-chip data latches
- Latched true and complemented output enables for easy word expansion
- Predetermined OFF outputs on power-up
- Fast access time — 60 ns commercial and 90 ns military maximum
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Member of generic PROM series utilizing standard programming algorithm

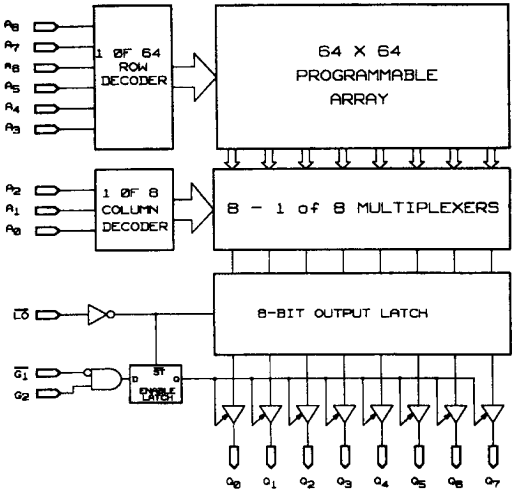
GENERAL DESCRIPTION

The Am27S15 (512-words by 8-bits) is a fully decoded, Schottky array, TTL Programmable Read-Only Memory (PROM), incorporating on-chip data and enable latches. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls.

This device will operate in a transparent mode when the Output Latch Enable signal (LO) is held HIGH. When the Output Latch Enable signal is LOW, the output conditions present at the time of the HIGH-to-LOW transition of LO will be latched into the part.

If LO is LOW upon power-up, the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Part Number	Am27S15	
Address Access Time	60ns	90ns
Operating Range	C	M

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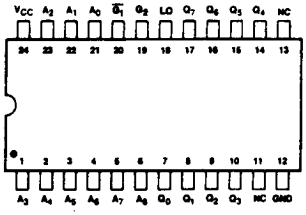
CONNECTION DIAGRAM
Top View



CD001011

Note: Pin 1 is marked for orientation. NC = No Connection.

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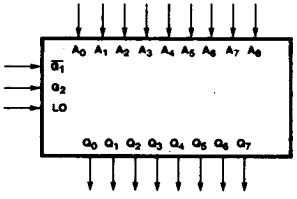
LOGIC SYMBOL



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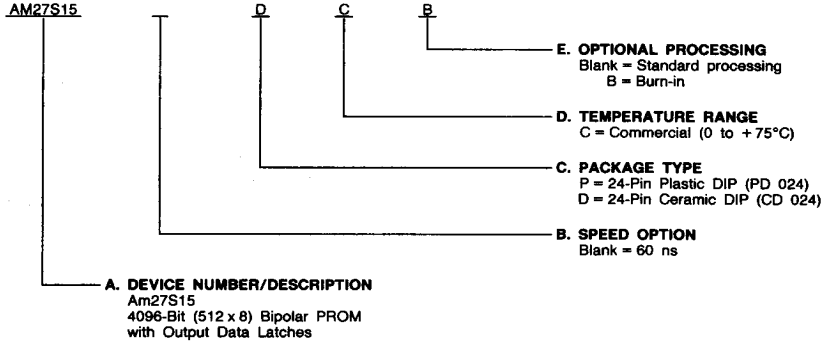
ORDERING INFORMATION (Cont'd.)
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S15	PC, PCB, DC, DCB

Valid Combinations

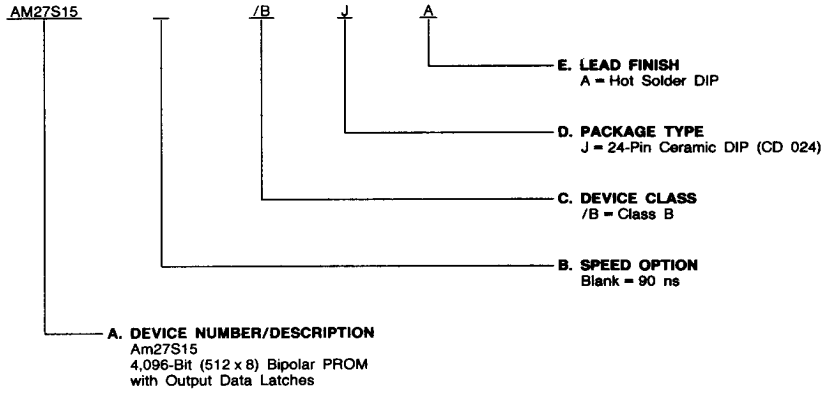
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S15	/BJA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address Inputs
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

LO Output Latch Enable
The LO signal controls both the data and enable latches. The LOW-to-HIGH transition of LO "Opens" the data and enable latches. The HIGH-to-LOW transition of LO "Closes" the data and enable latches.

$Q_0 - Q_7$ Data Output Port
Parallel data output from the data latches. The disabled state of these outputs is floating or high impedance.

$\overline{G_1}$, G_2 Output Enable
Controls the state of the Q-output, three-state drivers in conjunction with LO.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military products 100% tested at case temperature −55°C, +25°C, +125°C.

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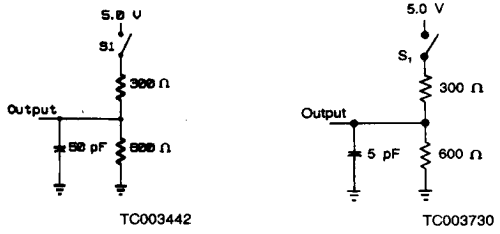
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7			Volts
			MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input Low Level	Guaranteed input logical LOW voltage for all inputs (Note 3)	COM'L			0.85	Volts
			MIL			0.80	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V	COM'L			−0.100	mA
			MIL			−0.150	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−70	mA
			MIL	−15		−65	
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.	COM'L			175	mA
			MIL			185	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max., $V_{\overline{G1}}$ = 2.4 V $V_{\overline{G2}}$ = 0.4 V	V_O = 4.5 V			40	µA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2)			8		

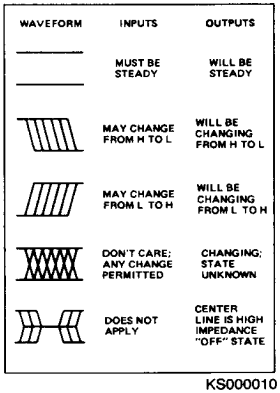
Notes: 1. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
2. These parameters are not 100% tested, but are periodically sampled.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS



KEY TO SWITCHING WAVEFORMS



A. Output Load for All AC Tests Except TGVQZ

B. Output Load for TGVQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.
S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)*

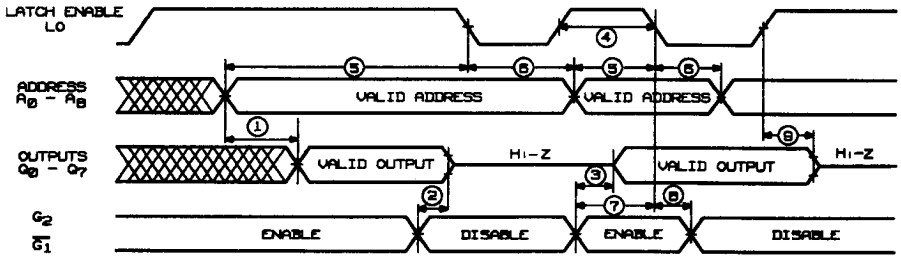
No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid		60		90	ns
2	TG1HQZ TG2LQZ	Delay from Output Enable (HIGH or LOW) to Output Hi-Z (Note 2)		40		50	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid (HIGH or LOW)		40		50	ns
4	TLOHLOL	Latch Enable Pulse Width (HIGH)	30		40		ns
5	TAVLOL	Address Valid to Latch Enable LOW Setup Time	60		90		ns
6	TLOLAX	Latch Enable LOW to Address Change Hold Time	0		5		ns
7	TGVLOL	Output Enable Valid to Latch Enable LOW Setup Time	40		50		ns
8	TLOLGX	Latch Enable LOW to Output Enable Change Hold Time	10		10		ns
9	TLOHQZ	Delay from LO HIGH to Output Disabled (Note 2)		35		45	ns

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TG1HQZ, TG2LQZ, and TLOHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORM



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GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TG1HQZ TG2LQZ	9, 10, 11
3	TGVQV	9, 10, 11
4	TLOHLOL	9, 10, 11
5	TAVLOL	9, 10, 11
6	TLOLAX	9, 10, 11
7	TGVLOL	9, 10, 11
8	TLOLGX	9, 10, 11
9	TLOHQZ	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.