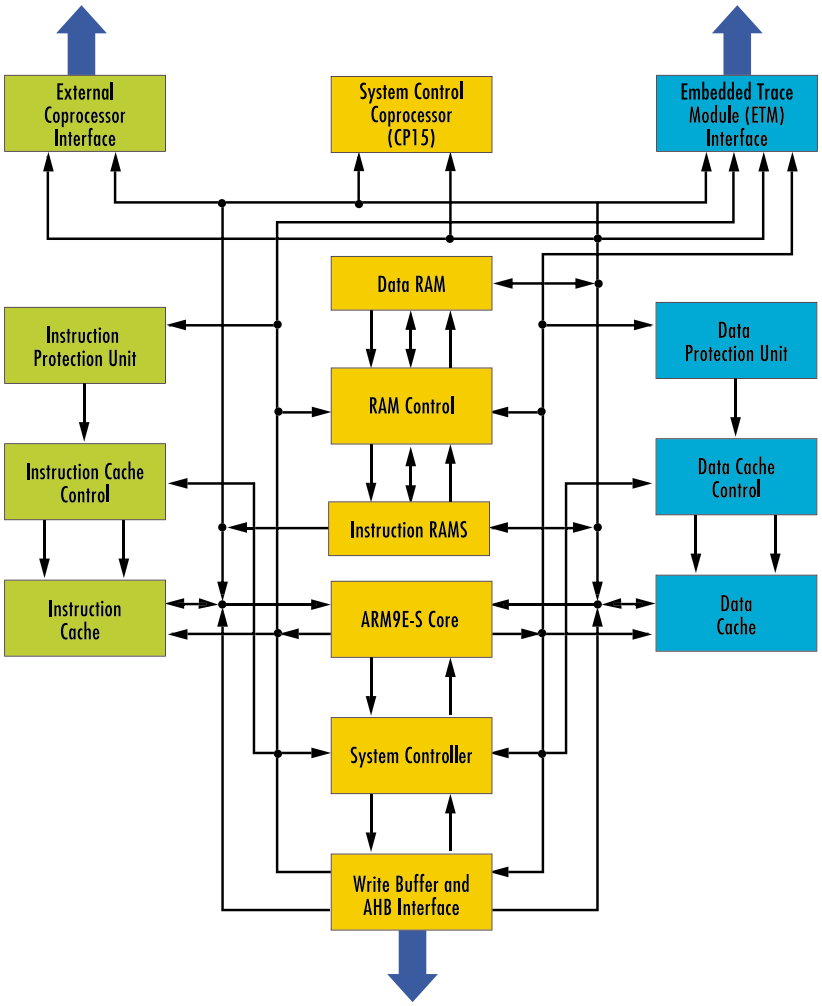
CW001100 - 200 MHz Synthesized ARM946E-S™ Core with Cache Memories

OVERVIEW

The CW001100 processor core is a 200 MHz implementation of the popular ARM946E-S™, synthesized onto LSI Logic's G12P 0.18 micron high performance process technology.

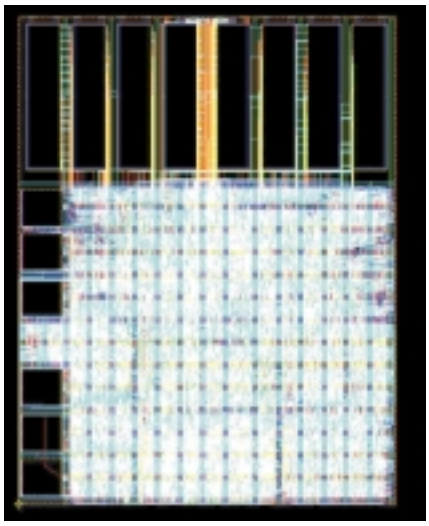
The ARM946E-S, which is based on the five stage pipeline ARM9E-S™ Harvard architecture processor, also contains a complete memory subsystem of instruction and data caches (16 kBytes each), and configurable tightly coupled instruction and data memories (TCMs). The core also includes an Embedded Trace Macrocell (ETM) interface, and an AMBA™ (Advanced Microprocessor Bus Architecture) AHB (Advanced High performance Bus) interface unit. This high level of integration helps ease the task of integrating the core into your System-on-Chip (SoC) design.



ARM946E-S Block Diagram

FEATURES AND BENEFITS

- 200 MHz operating frequency (worst case commercial conditions)
- Implemented on LSI Logic's G12P 0.18 micron, 1.8 V process
- 1.9 mW/MHz power dissipation, (with 0 kBytes TCMs)
- ARM946E-S industry standard architecture
- 16 kByte instruction and data caches (4-way set associative)
- Configurable TCMs
- Synthesized core for optimal timing accuracy and ASIC compatible design flow
- Regional ARM CoreWare design support



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200 MHz ARM946E-S™ Core

The inclusion of both cache memories and TCMs gives this core the flexibility to address a very broad range of system applications. The cache memories offer a convenient cost-effective solution for handling applications with large memory requirements, and the TCMs are ideal for highly deterministic code where precise memory cycle counts are required. The AHB interface provides a write buffer capable of burst transfers and split transactions. The ETM interface, when used with the optional ETM core, provides extensive real-time trace capabilities.

The ARM946E-S has full support for the ARMv5TE instruction set including all of the ARM9E-S family DSP instruction extensions. The core has full support for both the ARM® 32-bit and Thumb® 16-bit instruction sets, making it upwardly code-compatible with both the ARM7TDMI™ and ARM9TDMI™ families. The ability to switch on the fly between ARM® and Thumb® instruction sets allows the user to trade between high performance and code density.

The built in AMBA bus interface of the ARM946E-S core is an ideal standard bus for building a complete CPU subsystem design. LSI Logic offers both an AMBA subsystem reference design, and a library of popular AMBA CPU peripherals for use by customers on SoC designs. Customers can also incorporate their own AMBA-based blocks into this widely used industry standard bus.

The ARM946E-S is supported by a wide array of software development tools available from ARM Limited as well as third party vendors.

The core is implemented in LSI Logic's G12P high performance 0.18 micron (drawn) process, giving a maximum speed of 200 MHz (worst case commercial conditions) and making it ideal for high performance applications. Power consumption for the core is 1.9 mW/MHz (including cache memories but excluding TCMs).

The CW001100 core is synthesized onto the G12P SoC cell library and is provided complete with highly accurate timing models that fully support Static Timing Analysis (STA) through the core. This can be a significant benefit for achieving timing closure on high performance designs. The core is fully compatible with LSI Logic's entire FlexStream™ SoC ASIC design flow making it straightforward to integrate into complex customer designs. The core comes complete with built-in full scan chains for good testability, and is provided with a comprehensive set of deliverables including design files, STA and ATPG scripts, and detailed integration guidelines. To further assist customers with their designs, LSI Logic provides specialized ARM CoreWare® integration support through our team of regionally based field CoreWare engineers.

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