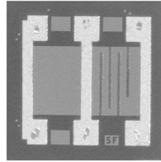


Thin Film, Center-Tapped Resistors



Product may not
be to scale

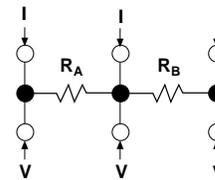
The CTA series resistor chips combine the best tolerances, stability and low shunt capacitance. The CTA offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTAs six bonding pads allows the user increased layout flexibility. The CTAs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTAs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

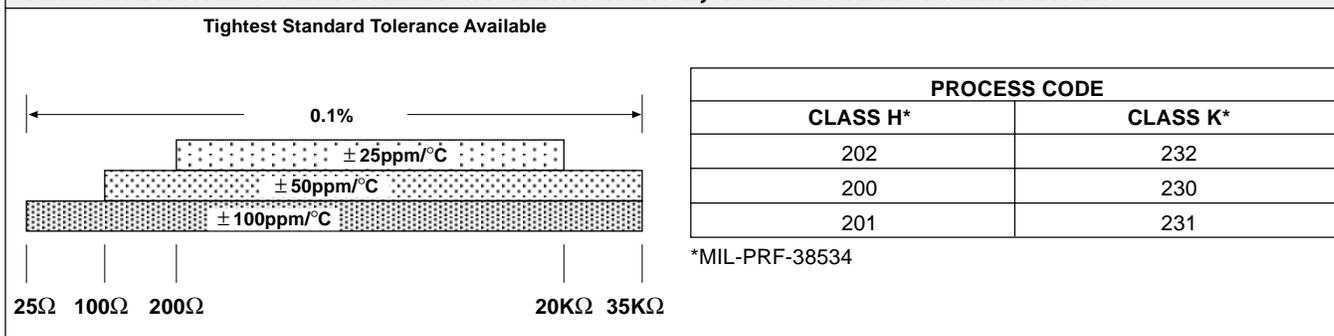
The CTA center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical.

Recommended for hermetic environments where chip is not exposed to moisture.

For lower values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire Kelvin technique. The measuring method is illustrated in the diagram to the right.

**FEATURES**

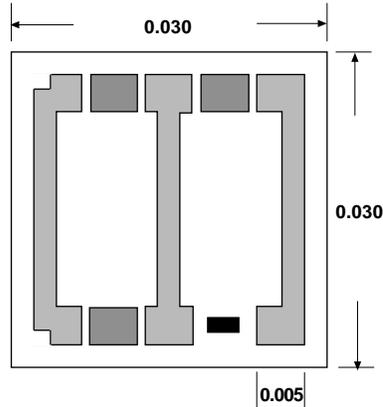
- Center tap feature
- Tight ratio tolerances to: $\pm 0.1\%$
- Chip size: 0.030 inches square
- Resistance range total: 25 Ω to 35k Ω
- Alumina substrate, low shunt capacitance: < 0.2pF
- Resistor material nichrome
- Excellent stability: $\pm 0.025\%$ maximum $\Delta R/R$

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES**STANDARD ELECTRICAL SPECIFICATIONS**

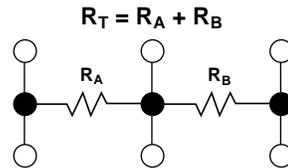
PARAMETER	
TCR tracking between halves (R_A , R_B)	$\pm 2\text{ppm}/^\circ\text{C}^*$
Center tap ratio, R_A/R_B tolerance	$1 \pm 1\%$ standard
Noise, MIL-STD-202, Method 308	- 35dB typical
Moisture resistance, MIL-STD-202 Method 106, (Passivated only)	$\pm 0.5\%$ maximum $\Delta R/R$
Stability, 1000 hours, + 125 $^\circ\text{C}$, 62mW	$\pm 0.025\%$ maximum $\Delta R/R$
Operating temperature range	- 55 $^\circ\text{C}$ to + 125 $^\circ\text{C}$
Thermal shock, MIL-STD-202, Method 107, Test condition F	$\pm 0.1\%$ maximum $\Delta R/R$
High temperature exposure, + 150 $^\circ\text{C}$, 100 hours	$\pm 0.1\%$ maximum $\Delta R/R$
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70 $^\circ\text{C}$ (derated to zero at + 150 $^\circ\text{C}$)	125mW
5 x rated power short-time overload, + 25 $^\circ\text{C}$, 5 seconds	$\pm 0.25\%$ maximum $\Delta R/R$

*10ppm/ $^\circ\text{C}$ for $R < 100$

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 • ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.42.729.0661 FAX: +81.42.729.3400 • SINGAPORE +65.788.6668 FAX: +65.788.0988
 • SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches

STANDARD CONFIGURATION

*Six locations. All pads 0.005 x 0.005

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.050mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% Alumina
Resistor material	Nichrome
Bonding pads	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	25kÅ minimum gold
Backing	None

OPTIONS: Aluminum bonding pads, 10kÅ minimum
 Center-tap ratio tolerances to 0.02%, R > 1kΩ
 Consult Applications Engineer

ORDERING INFORMATION						
Example: 100% visualled, 10kΩ, ± 1%, ± 100ppm/°C TCR, Gold Pads, Class H						
P/N:	W INSPECTION /PACKAGING	CTA PRODUCT FAMILY	201 PROCESS CODE	1000 RESISTANCE VALUE	1 MULTIPLIER CODE	F TOLERANCE CODE
	W = 100% visually inspected parts in matrix tray per MIL-STD-883 X = Sample, visually inspected loaded in matrix trays (4% AQL)		See Process Code table	Use first 4 significant digits of resistance (R _T)	B = 0.01 A = 0.1 0 = 1 1 = 10	A = 0.05% B = 0.1% C = 0.2% D = 0.5% F = 1.0% G = 2.0% H = 2.5% J = 5.0% K = 10% M = 20% L = 25%

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