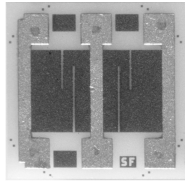


# Thin Film, Center-Tapped Resistors

CHIP RESISTORS



Product may not be to scale

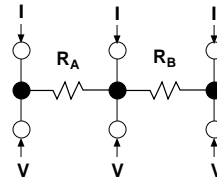
The CTT series resistor chips offer a combination of low shunt capacitance and excellent stability. The CTT offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature. The CTTs six bonding pads allows the user increased layout flexibility. The CTTs tantalum nitride resistor material offers excellent resistance to high moisture environments. The CTTs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTTs are 100% electrically tested and visually inspected to MIL-STD-883

### APPLICATIONS

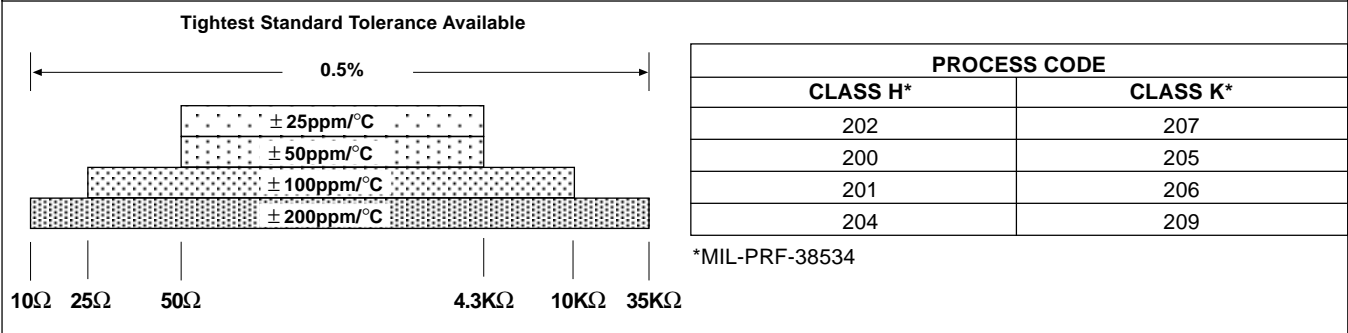
The CTT center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, tracking, low shunt capacitance and better frequency response are necessary. Vishay EFI measures low-value resistors by the four-wire Kelvin technique.

### FEATURES

- Center tap feature
- Chip size: 0.030 inches square
- Resistance range  $R_T$ : 10Ω to 36kΩ
- Alumina substrate, low shunt capacitance: < 0.2pF
- Resistor material: tantalum nitride
- Moisture resistant



### TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES

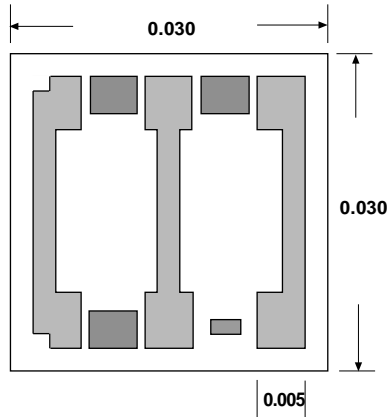


### STANDARD ELECTRICAL SPECIFICATIONS

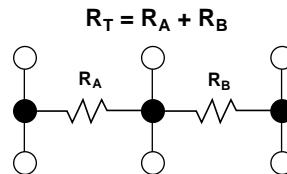
PARAMETER	
TCR tracking between halves ( $R_A$ , $R_B$ )	$\pm 2\text{ppm}/^\circ\text{C}^*$
Center tap ratio, $R_A/R_B$ : Tolerance	$1 \pm 1\%$
Noise, MIL-STD-202, Method 308	- 35dB typical
Moisture resistance, MIL-STD-202 Method 106	$\pm 0.5\%$ maximum $\Delta R/R$
Stability, 1000 hours, + 125°C, 62mW	$\pm 0.25\%$ maximum $\Delta R/R$
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202, Method 107, Test condition F	$\pm 0.1\%$ maximum $\Delta R/R$
High temperature exposure, + 150°C, 100 hours	$\pm 0.2\%$ maximum $\Delta R/R$
Insulation resistance	$10^{12}$ minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at + 150°C)	125mW
5 x rated power short-time overload, 25°C, 5 seconds	$\pm 0.25\%$ maximum $\Delta R/R$

\*10ppm/°C for  $R < 100$

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**DIMENSIONS** in inches

**STANDARD CONFIGURATION**

\*Six locations. All pads 0.005 x 0.005

**SCHEMATIC**


<b>MECHANICAL SPECIFICATIONS</b> in inches	
PARAMETER	
Chip size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.050mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	99.6% Alumina
Resistor material	Tantalum nitride
Bonding pad size	0.005 x 0.005 (0.127 x 0.127mm)
Number of pads	6
Pad material	25kÅ minimum gold
Backing	None

**OPTIONS:** Alphanumeric part marking, up to six characters  
 Aluminum bonding pads, 10kÅ minimum  
 Consult Applications Engineer

<b>ORDERING INFORMATION</b>						
Example: 100% visualled, 10kΩ, ± 1%, ± 100ppm/°C TCR, Gold Pads, Class H						
<b>P/N:</b>	<b>W</b>	<b>CTT</b>	<b>201</b>	<b>1000</b>	<b>1</b>	<b>F</b>
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	<b>W</b> = 100% visually inspected parts per MIL-STD-883 loaded in matrix trays		See Process Code table	Use first 4 significant digits of resistance ( $R_T$ )	<b>B</b> = 0.01 <b>A</b> = 0.1 <b>0</b> = 1 <b>1</b> = 10 <b>2</b> = 100 <b>3</b> = 1000 <b>4</b> = 10000	<b>D</b> = 0.5% <b>F</b> = 1.0% <b>G</b> = 2.0% <b>H</b> = 2.5% <b>J</b> = 5.0% <b>K</b> = 10% <b>M</b> = 20% <b>L</b> = 25%

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