



MATRA M H S

T-46-23-12
September 1990

DATA SHEET

HM 65162

2 k x 8

VERY LOW POWER CMOS SRAM

FEATURES

- ACCESS TIME
MILITARY/INDUSTRIAL : 70/85 ns (max)
COMMERCIAL : 55/70 ns (max)
- VERY LOW POWER CONSUMPTION
ACTIVE : 240 mW (typ)
STANDBY : 2.0 μ W (typ)
DATA RETENTION : 0.8 μ W (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN
RESISTORS ARE REQUIRED

DESCRIPTION

The HM 65162 is a very low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.

The HM 65162 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible standby supply current (typical value = 0.1 μ A) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Easy memory expansion is provided by an active low chip select (CS), an active low output enable (OE) and three state drivers.

All inputs and outputs of the HM-65162 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65162 is processed following the test methods of MIL STD 883C.

PACKAGES

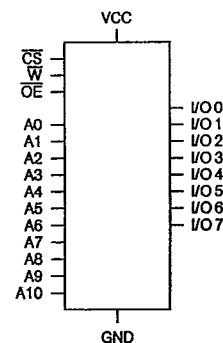
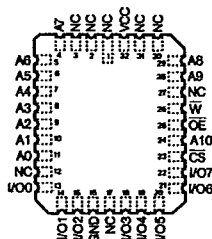
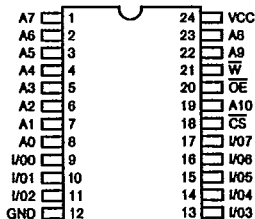
LOGIC SYMBOL

Plastic 600 mils, 24 pins, DIL.
Ceramic 600 mils, 24 pins, DIL.

LCC, 32 pins.

Pinout DIL 24 pins (top view)

Pinout LCC 32 pins (top view)



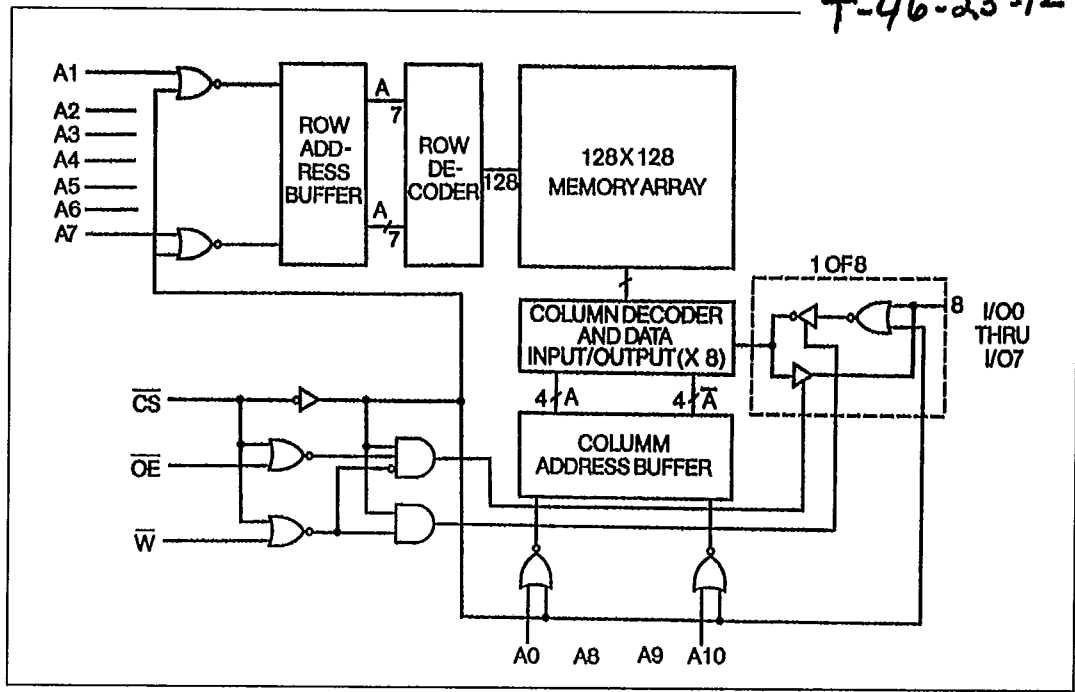
8

HM 65162

MATRA M H S

BLOCK DIAGRAM

T-46-23-12



8

PIN NAMES

A0-A10 : Address inputs	$\overline{CS}$: Chip Select
I/O0-I/O7 : Input/Output	$\overline{OE}$: Output Enable
Vcc : Power	$\overline{W}$: Write enable
GND : Ground	

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : -0.5 V to $+7.0\text{ V}$
 Input or Output voltage applied : (Gnd -0.3 V) to ($V_{cc} + 0.3\text{ V}$)
 Storage temperature : -65°C to $+150^{\circ}\text{C}$

*T-46-23-12***OPERATING RANGE**

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(- 2)	$V_{cc} \pm 10\%$	-55°C to $+125^{\circ}\text{C}$
Industrial	(- 9)	$V_{cc} \pm 10\%$	-40°C to $+85^{\circ}\text{C}$
Commercial	(- 5)	$V_{cc} \pm 10\%$	0°C to $+70^{\circ}\text{C}$

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{cc}	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
V_{IL} (1)	Input low voltage	-0.3	0.0	0.8	V
V_{IH}	Input high voltage	2.2	—	$V_{cc} + 0.3\text{ V}$	V

Note : 1. V_{IL} min = -0.3 V or -1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
C_{in} (2)	Input capacitance	—	—	5	pF
C_{out} (2)	Output capacitance	—	—	7	pF

Note : 2. $T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{cc} = 5.0\text{ V}$, these parameters are not 100% tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

MATRA M H S

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	- 1.0	-	1.0	μ A
IOZ	(3)	Output leakage current	- 1.0	-	1.0	μ A
VOL	(4)	Output low voltage	-	-	0.4	V
VOH	(4)	Output high voltage	2.4	-	-	V

Notes : 3. Gnd < VIN < Vcc, Gnd < Vout < Vcc Output disabled.
 4. Vcc min, IOL = 4.0mA, IOH = - 1.0mA.

T-46-23-12

Consumption for Commercial specification (- 5) :

SYMBOL		PARAMETER	65162 B-5	65162 -5	65162 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	2.0	2.0	mA	max
ICCSB1	(6)	Standby supply current	1.0	1.0	100.0	μ A	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOPI	(8)	Operating supply current	70.0	70.0	70.0	mA	max

Consumption for Industrial specification (- 9) :

SYMBOL		PARAMETER	65162 B-9	65162 -9	65162 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	3.0	3.0	mA	max
ICCSB1	(6)	Standby supply current	5.0	5.0	100.0	μ A	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOPI	(8)	Operating supply current	70.0	70.0	70.0	mA	max

Consumption for Military specification (- 2) :

SYMBOL		PARAMETER	65162 B-2	65162 -2	65162 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	5.0	5.0	5.0	mA	max
ICCSB1	(6)	Standby supply current	50.0	50.0	500.0	μ A	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOPI	(8)	Operating supply current	70.0	70.0	70.0	mA	max

Notes : 5. CS $\geq$ VIH.
 6. CS $\geq$ Vcc - 0.3 V, Iout = 0 mA..
 7. CS $\leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
 8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

DATA RETENTION MODE

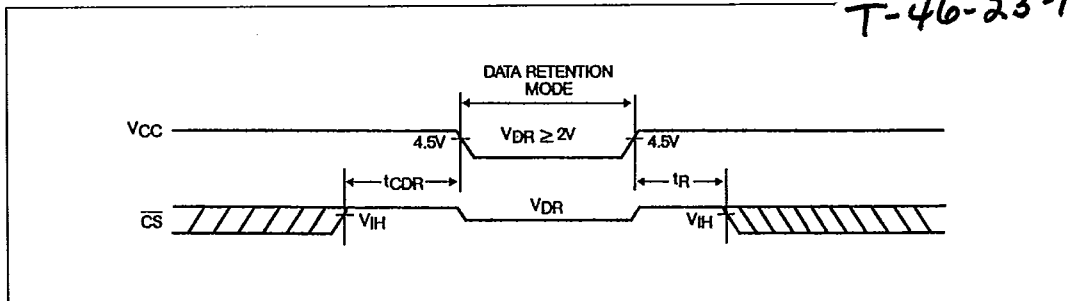
MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within V_{CC} to $V_{CC} + 0.3$ V.
2. Output Enable ($\overline{OE}$) should be held high to keep the

RAM outputs high impedance, minimizing power dissipation.

3. $\overline{CS}$ and $\overline{OE}$ must be kept between $V_{CC} + 0.3$ V and 70% of V_{CC} during the power up and power down transitions.
4. The RAM can begin operation > 55 ns after V_{CC} reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	V_{CC} for data retention	2.0	—	—	V
TCDR	Chip deselect to data retention time	0.0	—	—	ns
TR	Operation recovery time	TAVAV (10)	—	—	ns
ICCDR1 (11)	Data retention current 2.0 V : HM-65162(B)-5	—	0.1	1.0	μA
	HM-65162(B)-9	—	0.1	2.0	μA
	HM-65162(B)-2	—	0.1	20.0	μA
	HM-65162C-5	—	0.1	30.0	μA
	HM-65162C-9	—	0.1	30.0	μA
	HM-65162C-2	—	0.1	200.0	μA
ICCDR2 (11)	Data retention current 3.0 V : HM-65162(B)-5	—	0.3	1.0	μA
	HM-65162(B)-9	—	0.3	3.0	μA
	HM-65162(B)-2	—	0.3	30.0	μA
	HM-65162C-5	—	0.3	50.0	μA
	HM-65162C-9	—	0.3	50.0	μA
	HM-65162C-2	—	0.3	300.0	μA

Notes : 9. $T_A = 25^\circ C$.

10. TAVAV = Read cycle time.

11. $\overline{CS} = V_{CC}$, $V_{in} = Gnd/V_{CC}$, this parameter is only tested to $V_{CC} = 2$ V.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

T-46-23-12

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
 Input rise : 5 ns

Input timing reference levels : 1.5 V
 Output load : 1 TTL gate + 100 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65162 B-5	65162 -5	65162 C-5	UNIT	VALUE
TAVAV	Write cycle time	55	70	70	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	45	50	50	ns	min
TDVWH	Data set-up time	25	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	40	45	45	ns	min
TWLQZ (12)	Write low to high Z	35	40	40	ns	max
TWLWH	Write pulse width	35	40	40	ns	min
TWHAX	Address hold to end of write	10	10	10	ns	min
TWHDX	Data hold time	10	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

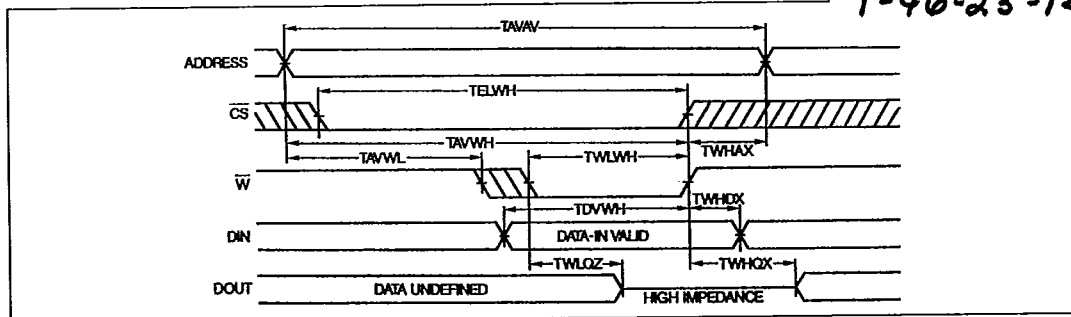
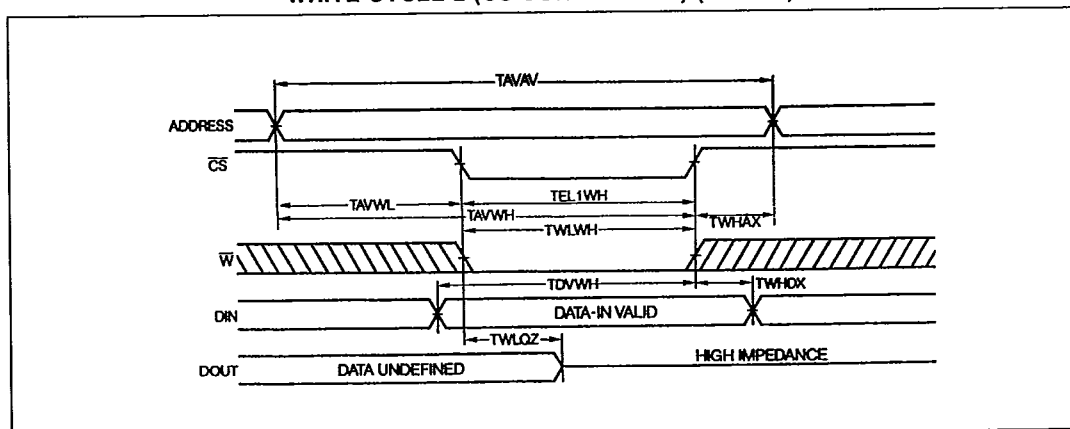
WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65162 B-9/2	65162 -9/2	65162 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	50	65	65	ns	min
TDVWH	Data set-up time	30	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	40	50	50	ns	max
TWLWH	Write pulse width	40	55	55	ns	min
TWHAX	Address hold to end of write	10	10	10	ns	min
TWHDX	Data hold time	10	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (note 13)

T-46-23-12

WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (note 13)

Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.

READ CYCLE : Commercial specification

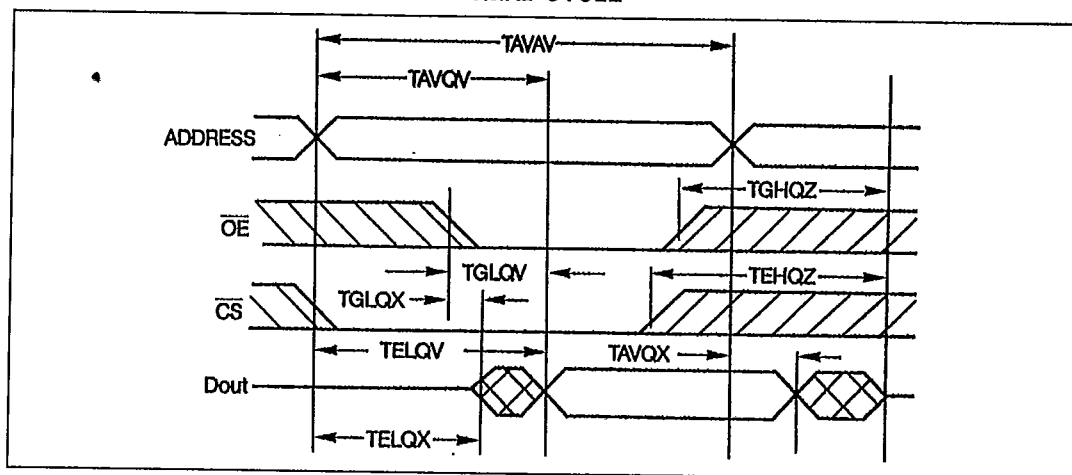
T-46-23-12

SYMBOL	PARAMETER	65162 B-5	65162 -5	65162 C-5	UNIT	VALUE
TAVAV	READ cycle time	55	70	70	ns	min
TAVQV	Address access time	55	70	70	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	55	70	70	ns	max
TELQZ	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	50	50	ns	max
TGLQV	Output enable access time	40	50	50	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	40	40	ns	max

READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65162 B-9/2	65162 -9/2	65162 C-9/2	UNIT	VALUE
TAVAV	READ cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	50	50	ns	max
TGLQV	Output Enable access time	50	65	65	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	40	40	ns	min

READ CYCLE



Addresses must remain stable for the duration of the read cycle. To read OE and CS must be < VIL and VIH. The output buffers can be controlled independently by OE while CS is low. To execute consecu-

tive read cycles, $\overline{CS}$ may be tied low continuously until all desired locations are accessed. When CS is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

HM 65162

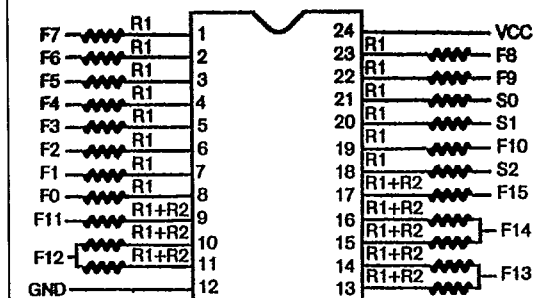
MATRA M H S

ORDERING INFORMATION

T-46-23-12

Package	Device Type	Grade	Level
HM1	65162	B	-5
0 - Chip form 1 - Ceramic 24 pins 600 mils 3 - Plastic 24 pins 600 mils 4 - LCC 32 pins	2 k x 8 very low power static RAM	B = high speed/low current Blank : standard speed/low current C : standard	- 5 : Commercial - 9 : Industrial - 2 : Military - 8 : Military with B.I. (B.I. = Burn-in)

BURN-IN SCHEMATICS



$R1 = 1\text{ K}\Omega$
 $R2 = 2.2\text{ K}\Omega$
 $F_0 = 25\text{ KHz} \pm 20\%$
 $F_n = 1/2 F_{n-1}$
 S_0, S_1, S_2 : programmable signals for write / read cycles
 $VCC = 5.5\text{ V}$