Preliminary

MATRA M H S

September 1990

DATA SHEET

HM 65797

256 K x 1 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCES TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 550 mW
  STANDBY : 193 mW
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000V ELECTROSTATIC DISCHARGE SINGLE 5 VOLT SUPPLY**

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DESCRIPTION

The HM-65797 is a high speed CMOS static RAM organised as 262, 144 X 1 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25ns are available with maximum power consumption of only 550mW.

The HM-65797 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 67 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

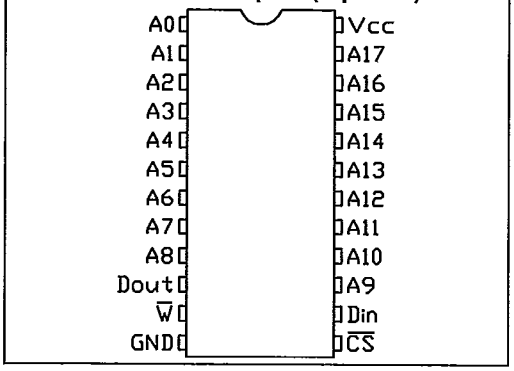
All inputs and outputs of the HM-65797 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65797 is 100 % processed following the test methods of MIL STD 883C.

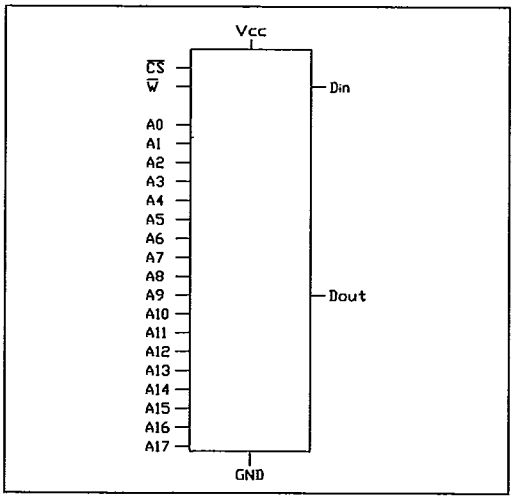
PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
SO/SOJ 300 and 330 mils, 24 pins
LCC 28 pins.
Tape and Reel Service

Pinout DIL 24 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM

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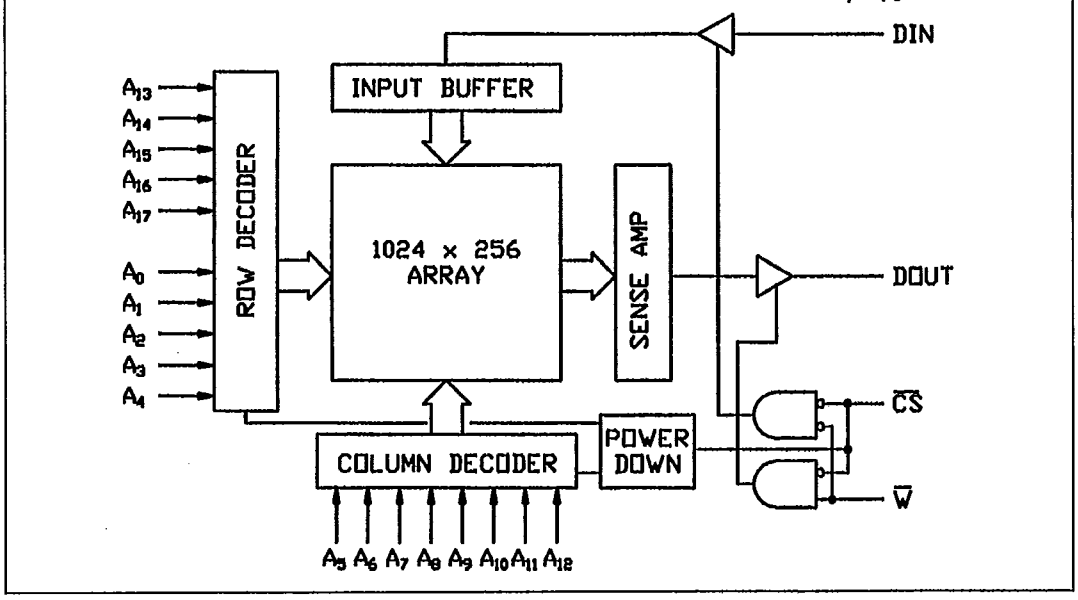

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PIN NAMES

A0-A17	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	Vcc	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip Select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	INPUT	OUTPUT	MODE
H	X	Z	Z	Deselect/Power Down
L	H	Z	Valid	Read
L	L	Valid	Z	Write
		Z	Z	

L = Low, H = High, X = H or L, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... – 0.5 V to + 7.0 V
DC input voltage..... – 3.0 V to + 7.0 V
DC output voltage in high Z state..... – 0.5 V to + 7.0 V
Storage temperature..... – 65°C + 150°C
Output current into outputs (low)..... 20 mA
Electro static discharge voltage ..... > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, V_{CC} = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS

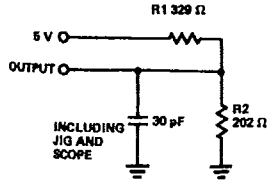


Figure 1a

Equivalent to : THEVENIN EQUIVALENT

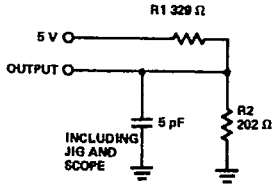


Figure 1b

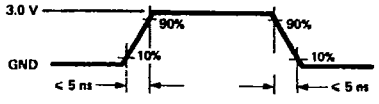
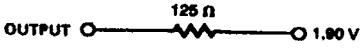
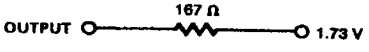


Figure 2



Commercial



Military

ELECTRICAL CHARACTERISTICS DC PARAMETER

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PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 50.0	–	50.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA (military), IOL = 12.0 mA (commercial)
5. Vcc min, IOH = – 4.0 mA.

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CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :

SYMBOL		PARAMETER	65797 H-5	65797 K-5	65797 M-5	65797 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	35	35	35	35	mA	max
ICCSB1	(8)	Standby supply current	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	100	100	100	100	mA	max

CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (-2) SPECIFICATION :

SYMBOL		PARAMETER	65797 K-9/-2	65797 M-9/-2	65797 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	35	35	35	mA	max
ICCSB1	(8)	Standby supply current	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	110	110	110	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ is required to keep the devices unselected during the Vcc power-up. Otherwise IccSB will exceed the above values. Min duty cycle = 100 %.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
8. $\overline{CS} \geq$ Vcc – 0.3V Iout = 0mA.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

WRITE CYCLE specification : Commercial, Industrial and Military

SYMBOL	PARAMETER	65797 H-5/-9/-2	65797 K-5/-9/-2	65797 M-5/-9/-2	65797 N-5/-9/-2	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to write end	20	30	40	50	ns	min
TDVWH	Data set-up time	15	17	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	13	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	35	ns	min
TWHAX	Address hold from write end	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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WRITE CYCLE 1 : $\overline{W}$ controlled (note 9)

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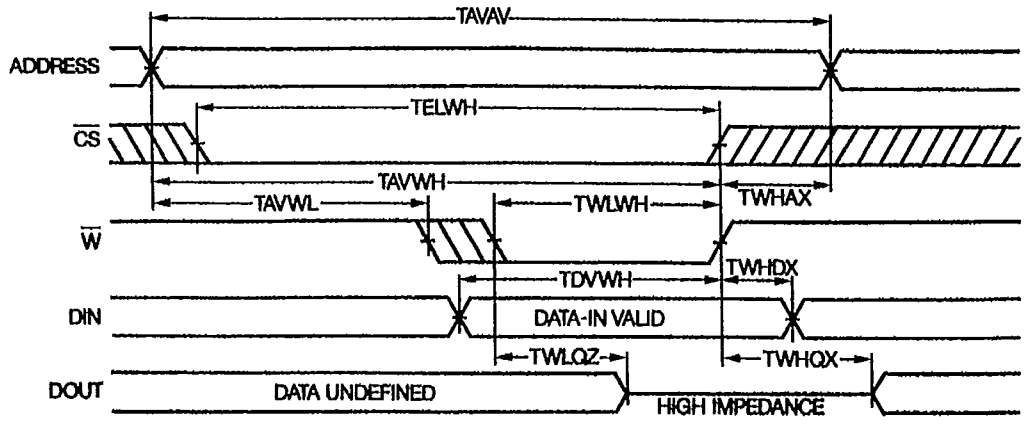
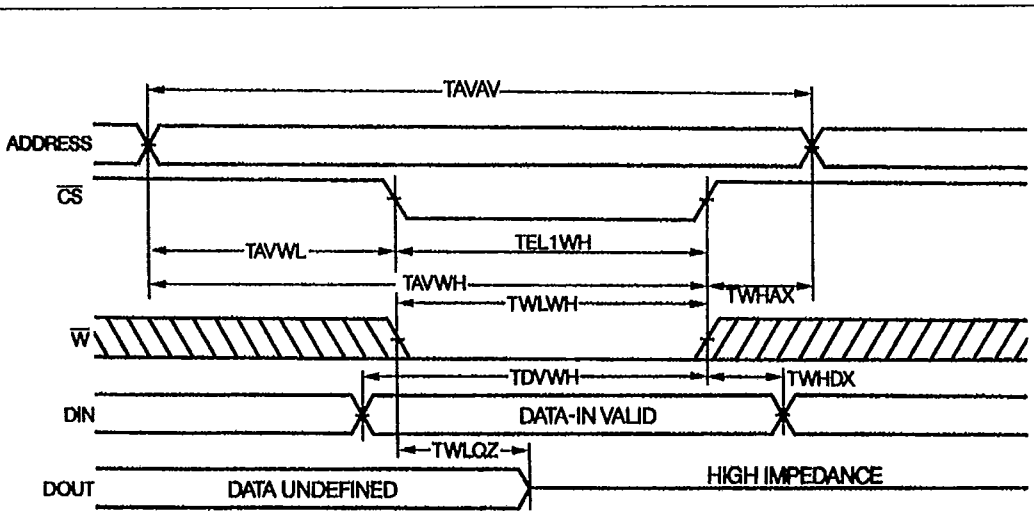


WRITE CYCLE 2 : $\overline{CS}$ controlled (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.

READ CYCLE : specification : Commercial, Industrial and Military

SYMBOL	PARAMETER	65797 H-5/-9/-2	65797 K-5/-9/-2	65797 M-5/-9/-2	65797 N-5/-9/-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	13	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power up	20	25	30	35	ns	max

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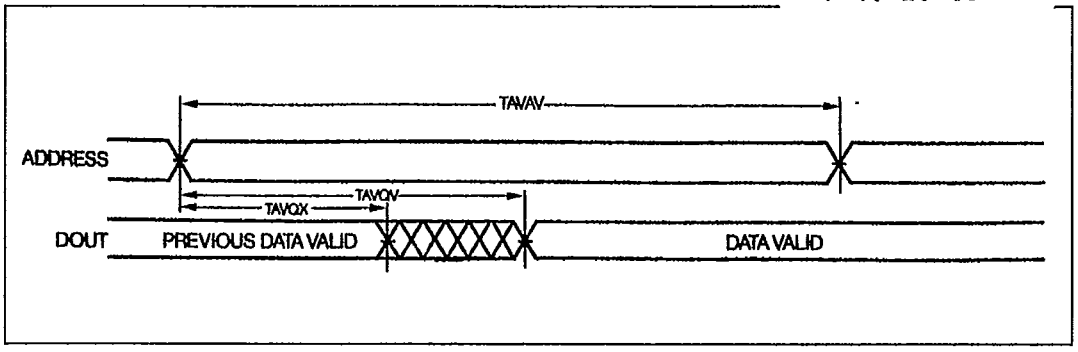
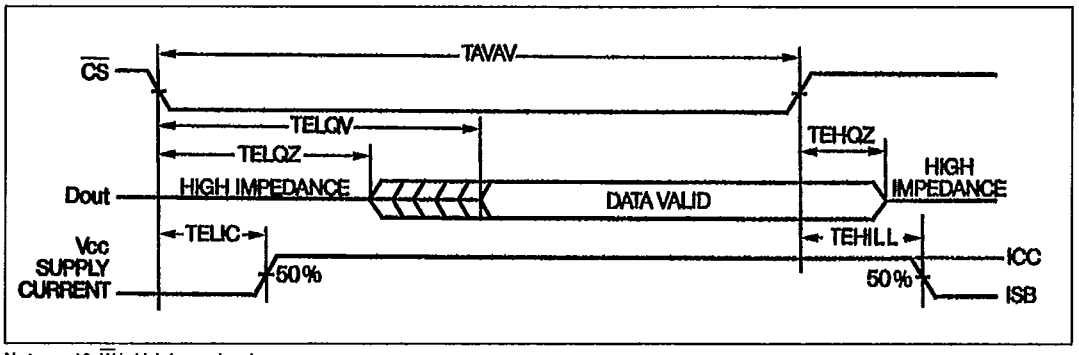
READ CYCLE 1 : (note 10, 11, 12) T-46-23-05



READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL.
12. Address valid prior or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65797	H	–5 : R
0 - Chip form 1 - Ceramic 24 pins 300 mils 3 - Plastic 24 pins 300 mils T - SOIC 24 pins 300 mils U - SOJ 24 pins 4 - LCC 28 pins	256 x 1 high speed static RAM	H = 25 ns K = 35 ns M = 45 ns N = 55 ns	–5 : Commercial –9 : Industrial –2 : Military –8 : Military with B.I Tape & Reel Service (B.I : Burn In)