Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (256K x 4-BIT) REVOLUTIONARY PINOUT

ADVANCE INFORMATION
IDT71B128

FEATURES:

- 256K x 4 advanced high-speed BiCMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise
- Equal access and cycle times
  — Commercial: 10/12/15ns
- One Chip Select plus one Output Enable pin
- Bidirectional data Inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in JEDEC 32-pin Plastic DIP and Plastic SOJ packages

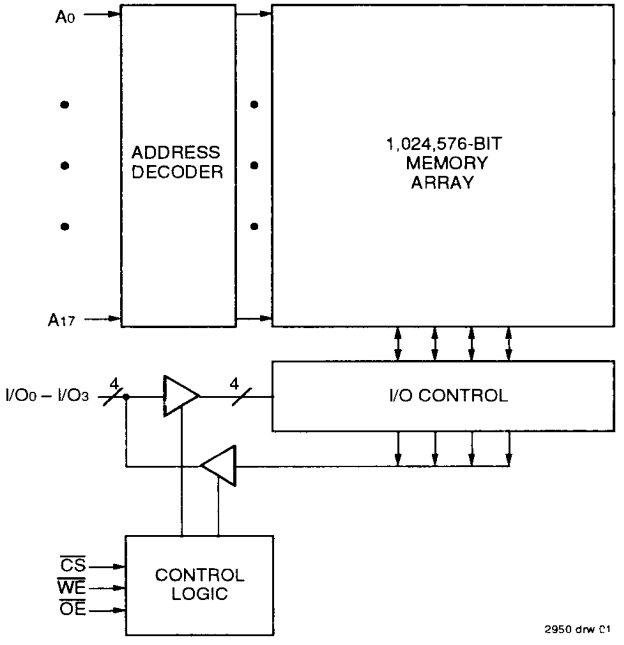
DESCRIPTION:

The IDT71B128 is a 1,024,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center pin power/GND pinout reduces noise generation and improves high speed system performance.

The IDT71B128 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71B128 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71B128 is packaged in 28-pin 400 mil Plastic DIP and 28-pin 400-mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



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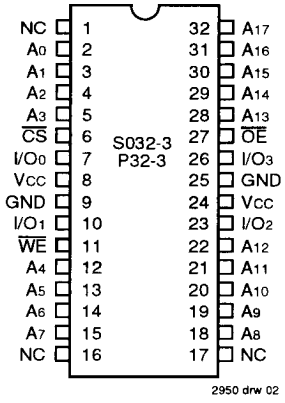
COMMERCIAL TEMPERATURE RANGE **SEPTEMBER 1992**

PIN CONFIGURATION



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2950 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2950 tbl 01
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2950 tbl 03
1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2950 tbl 04
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B128 Min.	IDT71B128 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2950 tbl 05

8

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B128S10 Com'l.	71B128S10 Mil.	71B128S12 Com'l.	71B128S12 Mil.	71B128S15 Com'l.	71B128S15 Mil.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	165	—	155	—	150	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	35	—	30	—	30	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2), $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	12	—	12	—	12	—	mA

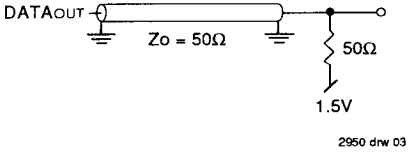
2950 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

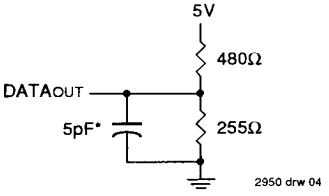
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2950 tbl 07



2950 drw 03

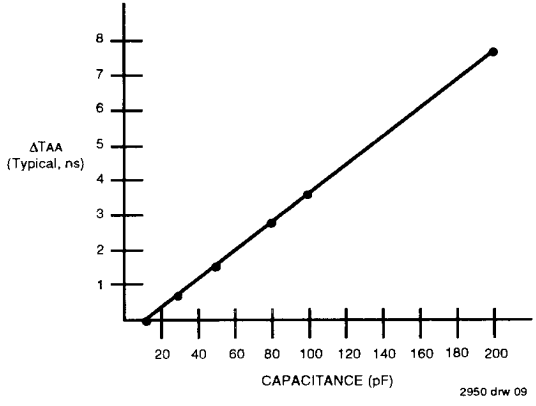
Figure 1. AC Test Load



2950 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})



2950 drw 09

Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B128S10		71B128S12		71B128S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	2	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	0	5	0	6	0	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	0	5	0	6	0	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	ns
t_{CW}	Chip Select to End of Write	8	—	9	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	7	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	0	5	0	6	0	7	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

2950 tbl 08

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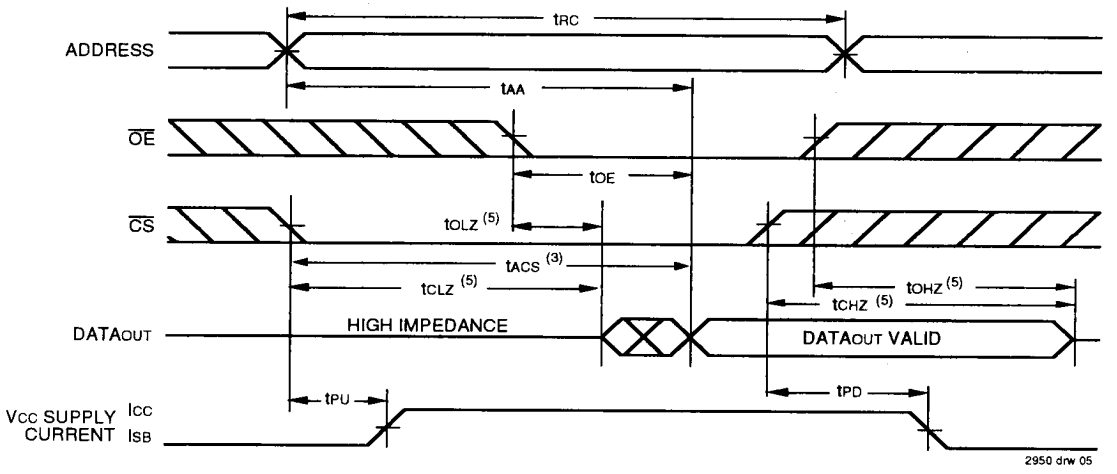
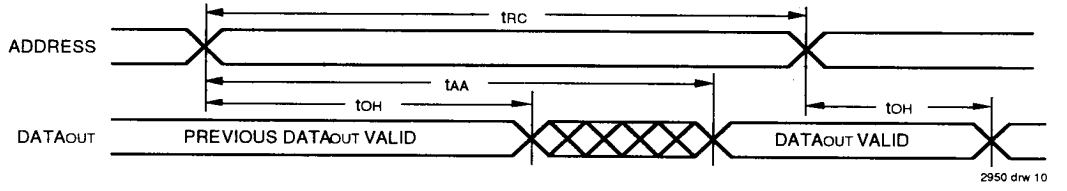
TIMING WAVEFORM OF READ CYCLE NO. 1(1)

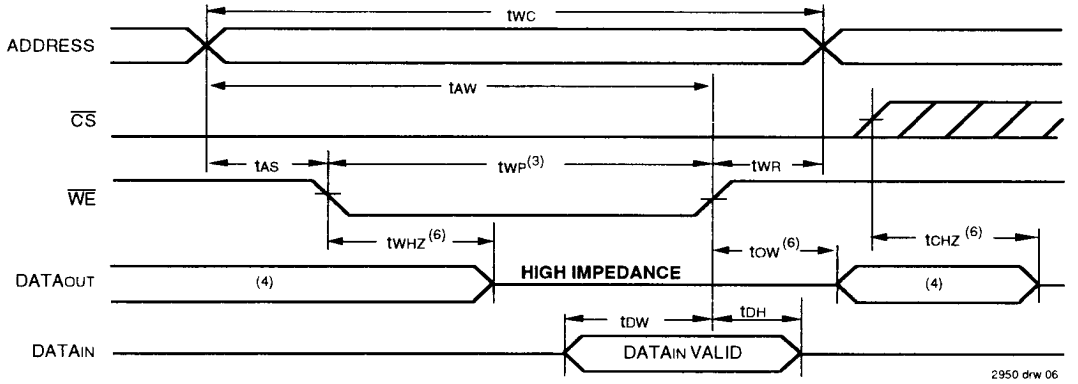


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

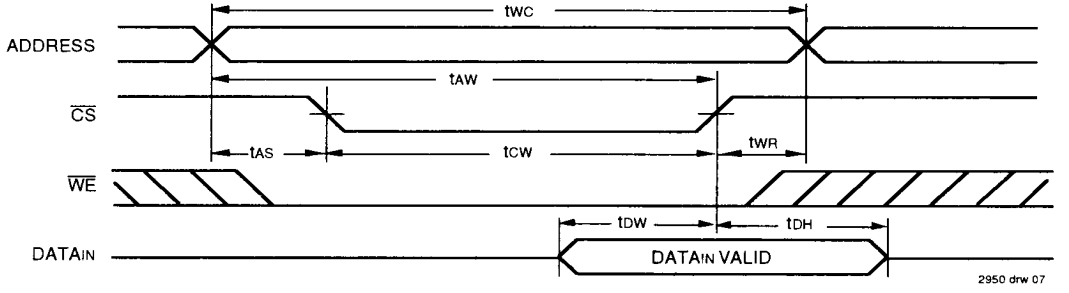


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.

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ORDERING INFORMATION