256Kx16 MONOLITHIC SRAM, SMD 5962-96902

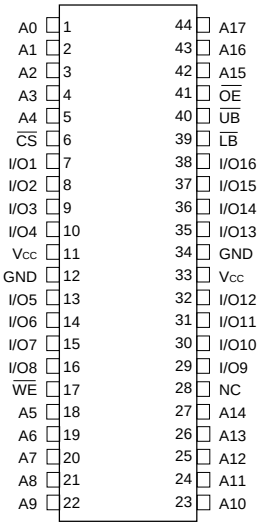
FEATURES

- Access Times 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 44 pin Ceramic SOJ (Package 102)
  - 44 lead Ceramic Flatpack (Package 225)
  - 44 lead Formed Ceramic Flatpack
- Organized as 256Kx16
- Data Byte Control:
  - Lower Byte ($\overline{LB}$) = I/O1-8
  - Upper Byte ($\overline{UB}$) = I/O9-16
- 2V Minimum Data Retention for battery back up operation (WMS256K16L-XXX Low Power Version Only)
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

PIN CONFIGURATION FOR WMS256K16-XXX

44 CSOJ
44 FLATPACK

TOP VIEW



PIN DESCRIPTION

A0-17	Address Inputs
$\overline{LB}$	Lower-Byte Control (I/O1-8)
$\overline{UB}$	Upper-Byte Control (I/O9-16)
I/O1-16	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
GND	Ground
NC	No Connection

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	Data I/O		Power
						I/O_{1-8}	I/O_{9-16}	
H	X	X	X	X	Not Select	High Z	High Z	Standby
L	H	H	X	X	Output Disable	High Z	High Z	Active
L	X	X	H	H				
L	H	L	L	H	Read	Data Out	High Z	Active
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	Active
			H	L		High Z	Data In	
			L	L		Data In	Data In	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	20	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		275	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		17	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

LOW POWER DATA RETENTION CHARACTERISTICS (WMS256K16L-XXX ONLY)

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		1.0	8.0	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		35		ns
Address Access Time	t_{AA}		17		20		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns
Chip Select Access Time	t_{ACS}		17		20		25		35	ns
Output Enable to Output Valid	t_{OE}		10		12		15		20	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		9		10		12		15	ns
Output Disable to Output in High Z	t_{OHZ}[1]		9		10		12		15	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}		10		12		14		17	ns
$\overline{LB}$, $\overline{UB}$ Enable to Low Z Output	t_{BLZ}[1]	0		0		0		0		ns
$\overline{LB}$, $\overline{UB}$ Disable to High Z Output	t_{BHZ}[1]		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

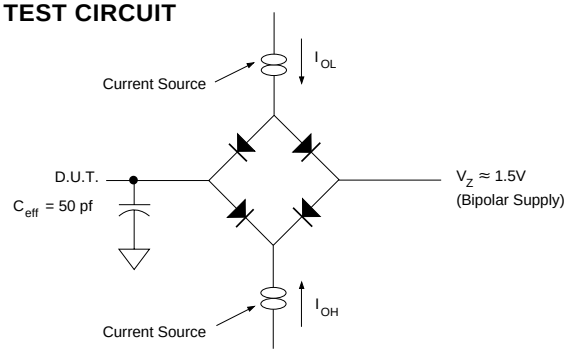
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		35		ns
Chip Select to End of Write	t_{CW}	14		17		20		25		ns
Address Valid to End of Write	t_{AW}	14		17		20		25		ns
Data Valid to End of Write	t_{DW}	10		12		15		20		ns
Write Pulse Width	t_{WP}	14		17		20		25		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	2		2		2		2		ns
Output Active from End of Write	t_{OW}[1]	0		0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}[1]		9		10		10		15	ns
Data Hold Time	t_{DH}	0		0		0		0		ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	14		17		20		25		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

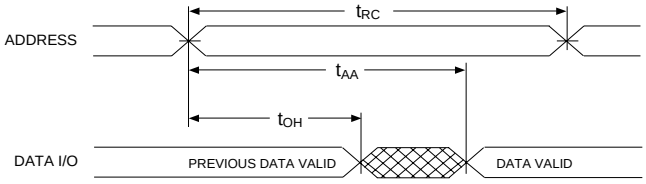


AC TEST CONDITIONS

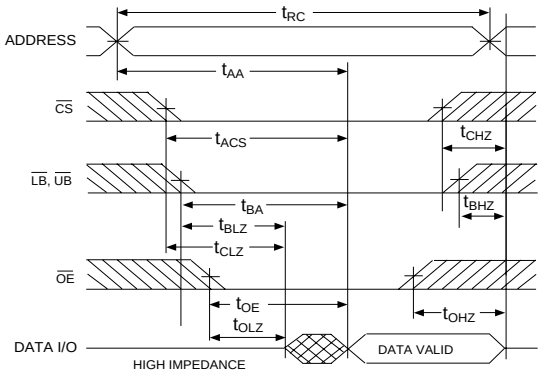
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

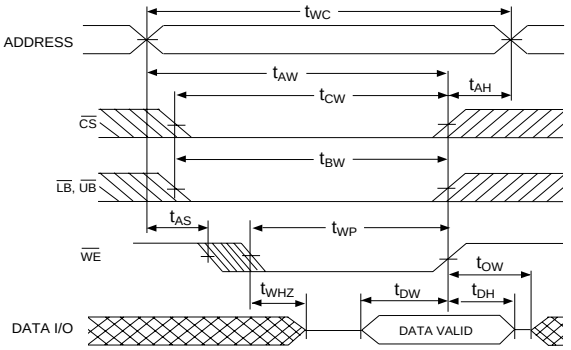


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{WE}$ = V_{IH})



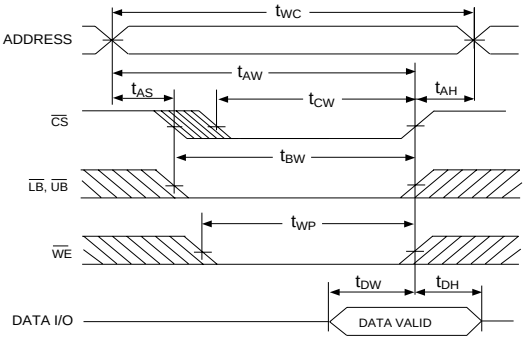
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



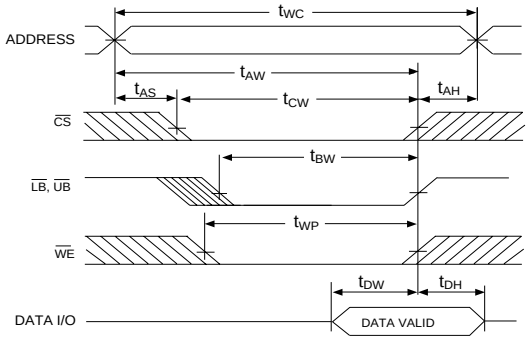
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



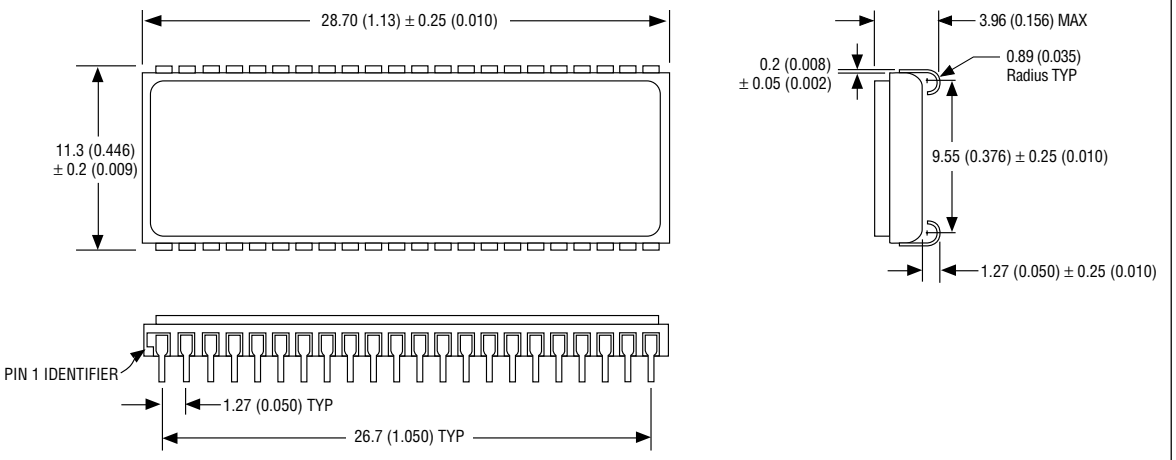
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

WRITE CYCLE - $\overline{LB}$, $\overline{UB}$ CONTROLLED



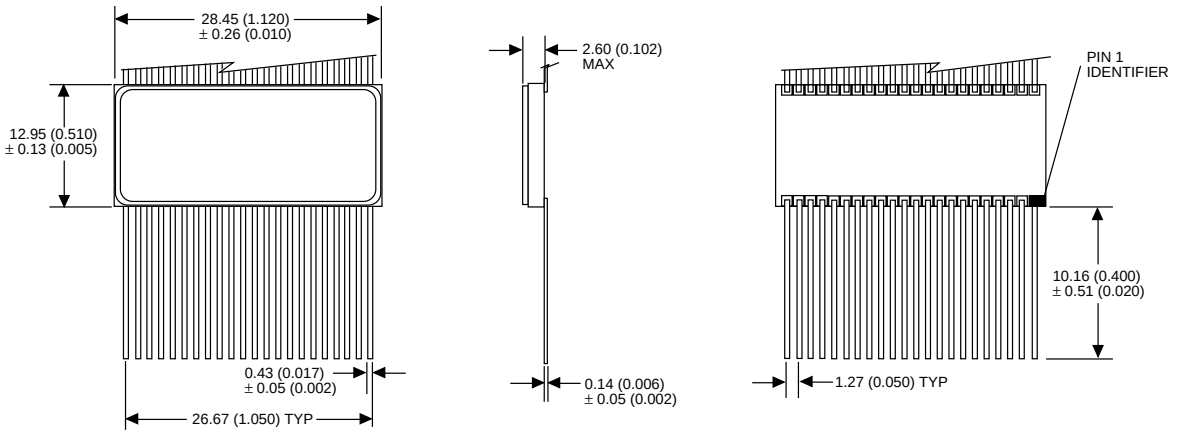
WRITE CYCLE 3, $\overline{LB}$, $\overline{UB}$ CONTROLLED

PACKAGE 102: 44 LEAD, CERAMIC SOJ



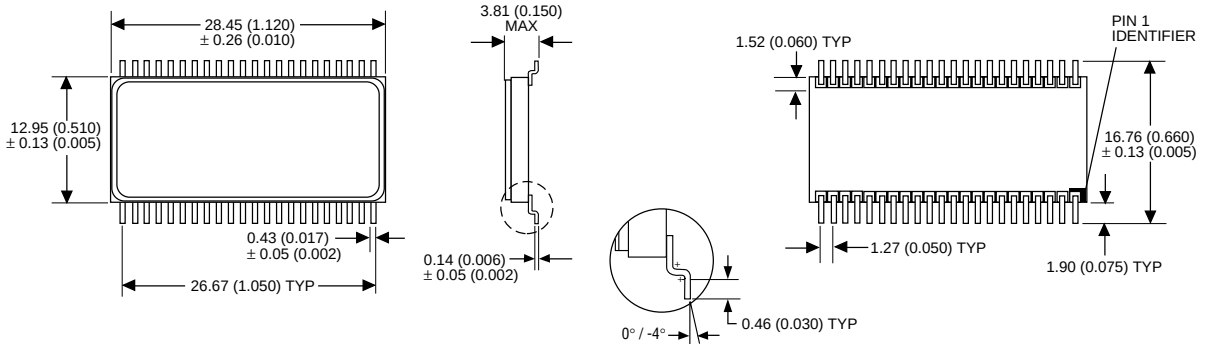
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 225: 44 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 211: 44 LEAD FORMED, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M S 256K16 X - XXX X X X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:
- DL = 44 Lead Ceramic SOJ (Package 102)
- FL = 44 Lead Ceramic Flatpack (Package 225)
- FG = 44 Lead Formed Ceramic Flatpack

ACCESS TIME (ns)

IMPROVEMENT MARK:
- Blank = Standard Power
- L = Low Power Data Retention

ORGANIZATION, 256K x 16

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
256K x 16 SRAM Monolithic	35ns	44 lead SOJ (DL)	5962-96902 01HMX
256K x 16 SRAM Monolithic	25ns	44 lead SOJ (DL)	5962-96902 02HMX
256K x 16 SRAM Monolithic	20ns	44 lead SOJ (DL)	5962-96902 03HMX
256K x 16 SRAM Monolithic	17ns	44 lead SOJ (DL)	5962-96902 04HMX
256K x 16 SRAM Monolithic	35ns	44 lead Flatpack (FL)	5962-96902 01HNX
256K x 16 SRAM Monolithic	25ns	44 lead Flatpack (FL)	5962-96902 02HNX
256K x 16 SRAM Monolithic	20ns	44 lead Flatpack (FL)	5962-96902 03HNX
256K x 16 SRAM Monolithic	17ns	44 lead Flatpack (FL)	5962-96902 04HNX
256K x 16 SRAM Monolithic	35ns	44 lead Formed Flatpack (FG)	5962-96902 01HTX
256K x 16 SRAM Monolithic	25ns	44 lead Formed Flatpack (FG)	5962-96902 02HTX
256K x 16 SRAM Monolithic	20ns	44 lead Formed Flatpack (FG)	5962-96902 03HTX
256K x 16 SRAM Monolithic	17ns	44 lead Formed Flatpack (FG)	5962-96902 04HTX