PowerPC 403GCX 32-Bit RISC Embedded Controller

Data Sheet

Features

- PowerPC™ RISC CPU and instruction set architecture
- Glueless interfaces to DRAM, SRAM, ROM, and peripherals, including byte and half-word devices
- 16KB instruction cache and 8KB write-back data cache, two-way set-associative
- Memory management unit
  –64-entry, fully associative TLB array
  –Variable page size (1KB-16MB)
  –Flexible TLB management
- Individually programmable on-chip controllers for:
  – Four DMA channels
  – DRAM, SRAM, and ROM banks
  – External interrupts
- DRAM controller supports EDO DRAM
- Flexible interface to external bus masters
- CPU core can run at 2X the external bus speed

Applications

- Set-top boxes and network computers
- Consumer electronics and video games
- Telecommunications and networking
- Office automation (printers, copiers, fax)

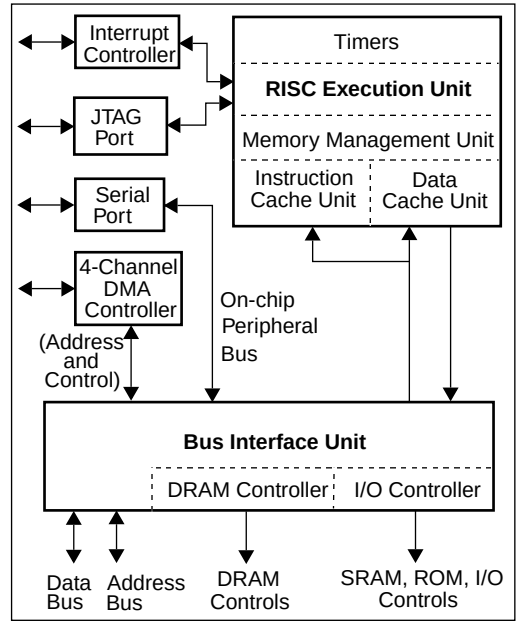
Specifications

- CPU core frequency of 76 MHz, I/Os to 38 MHz
- Interfaces to both 3V and 5V technologies
- Low-power 3.3V operation with built-in power management and stand-by mode
- Low-cost 160 lead PQFP package
- 0.45 µm triple-level-metal CMOS

Overview

The PowerPC 403GCX 32-bit RISC embedded controller offers high performance and functional integration with low power consumption. The 403GCX RISC CPU executes at sustained speeds approaching one cycle per instruction. On-chip caches and integrated DRAM and SRAM control functions reduce chip count and design complexity in systems, while improving system throughput.

External I/O devices or SRAM/DRAM memory banks can be directly attached to the 403GCX bus interface unit (BIU). Interfaces for up to eight memory banks and I/O devices, including a maximum of four DRAM banks, can be configured individually, allowing the BIU to manage devices or memory banks with differing control, timing, or bus width requirements.



The 403GCX RISC controller consists of a pipelined RISC processor core and several peripheral interface units: BIU, DMA controller, asynchronous interrupt controller, serial port, and JTAG debug port.

The RISC processor core includes the internal 16KB instruction cache and 8KB data cache, reducing overhead for data transfers to or from external memory. The instruction queue logic manages branch prediction, folding of branch and condition register logical instructions, and instruction prefetching to minimize pipeline stalls.The integrated memory management unit provides robust memory management and protection functions, optimized for embedded environments.

RISC CPU

The RISC core comprises four tightly coupled functional units: the execution unit (EXU), the memory management unit (MMU), the data cache unit (DCU), and the instruction cache unit (ICU). Each cache unit consists of a data array, tag array, and control logic for cache management and addressing. The execution unit consists of general purpose registers (GPR), special purpose registers (SPR), ALU, multiplier, divider, barrel shifter, and the control logic required to manage data flow and instruction execution within the EXU. The 403GCX core can operate at either 1X or 2X the speed of the external buses, which run at the SysClk input rate.

The EXU handles instruction decoding and execution, queue management, branch prediction, and branch folding. The instruction cache unit passes instructions to the queue in the EXU or, in the event of a cache miss, requests a fetch from external memory through the bus interface unit. The MMU provides translation and memory protection for instruction and data accesses, using a unified 64-entry, fully associative TLB array.

General Purpose Registers

Data transfers to and from the EXU are handled through the bank of 32 GPRs, each 32 bits wide. Load and store instructions move data operands between the GPRs and the data cache unit, except in the cases of noncacheable data or cache misses. In such cases the DCU passes the address for the data read or write to the BIU.When noncacheable operands are being transferred, data can pass directly between the EXU and the BIU, which interfaces to the external memory being accessed.

Special Purpose Registers

Special purpose registers are used to control debug facilities, timers, interrupts, the protection mechanism, memory cacheability, and other architected processor resources. SPRs are accessed using move to/from special purpose register (mtspr/mfspr) instructions, which move operands between GPRs and SPRs.

Supervisory programs can write the appropriate SPRs to configure the operating and interface modes of the execution unit. The condition register (CR) and machine state register (MSR) are written by internal control logic with program execution status and machine state, respectively. Status of external interrupts is maintained in the external interrupt status register (EXISR). Fixed-point arithmetic exception status is available from the exception register (XER).

Device Control Registers

Device control registers (DCR) are used to manage I/O interfaces, DMA channels, SRAM and DRAM memory configurations and timing, and status/address information regarding bus errors. DCRs are accessed using move to/from device control register (mtdcr/mfdcr) instructions, which move operands between GPRs and DCRs.

Instruction Set

Table 1 summarizes the 403GCX instruction set by categories of operations. Most instructions execute in a single cycle, with the exceptions of load/store multiple, load/store string, multiply, and divide instructions.

Bus Interface Unit

The bus interface unit integrates the functional controls for data transfers and address operations other than those which the DMA controller handles. DMA transfers use the address logic in the BIU to output the memory addresses being accessed.

Control functions for direct-connect I/O devices and for DRAM, SRAM, or ROM banks are provided by the BIU. Burst access for SRAM, ROM, and page-mode DRAM devices is supported for cache fill and flush operations.

The BIU controls the transfer of data between the external bus and the instruction cache, the data cache, or registers internal to the processor core. The BIU also arbitrates among external bus master and DMA transfers, the internal buses to the cache units and the register banks, and the serial port on the on-chip peripheral bus (OPB).

Memory Addressing Regions

The 403GCX can address an effective range of 4GB, mapped to 3.5GB (256MB for SRAM/ROM or other I/O, 256MB DRAM, and 3GB OPB/ reserved) of physical address space containing twenty-eight 128MB regions. Cacheability with respect to the instruction or data cache is programmed via the instruction and data cache control registers, respectively.

Within the DRAM and SRAM/ROM regions, a total of eight banks of devices are supported. Each bank can be configured for 8-, 16-, or 32-bit devices.

For individual DRAM banks, the number of wait states, bank size, $\overline{RAS}$-to-$\overline{CAS}$ timing, use of an external address multiplexer (for external bus masters), and refresh rate are user-programmable. For each SRAM/ROM bank, the bank size, bank location, number of wait states, and timings of chip selects, byte enables, and output enables are all user-programmable.

Memory Management Unit

The memory management unit (MMU) supports address translation and protection functions for embedded applications. When used with appropriate system level software, the MMU provides the following functions: translation of 4GB logical address space into physical addresses, independent enabling of instruction and data translation/ protection, page level cacheability and access control via the translation mechanism, software control of page replacement strategy, and additional control over protection via zones.

The fully associative 64-entry TLB array handles both instruction and data accesses. The translation for any virtual address can be placed in any one of the 64 entries, allowing maximum flexibility by TLB management software. Each TLB entry contains a translation for a page that can be any one of eight sizes from 1KB to 16MB, incrementing by powers of 4.

The TLB can simultaneously contain any mix of page sizes. This feature enables the use of small pages when maximum granularity is required, reducing the amount of wasted memory when compared to the more common fixed 4KB page size.

Table 1. 403GCX Instructions by Category

Category	Base Instructions
Data Movement	load, store
Arithmetic / Logical	add, subtract, negate, multiply, divide, and, or, xor, nand, nor, xnor, sign extension, count leading zeros
Comparison	compare, compare logical, compare immediate
Branch	branch, branch conditional
Condition	condition register logical
Rotate/Shift	rotate, rotate and mask, shift left, shift right
Cache Control	invalidate, touch, zero, flush, store
Interrupt Control	write to external interrupt enable bit, move to/from machine state register, return from interrupt, return from critical interrupt
Processor Management	system call, synchronize, move to/from device control registers, move to/ from special purpose registers

Instruction Cache Unit

The instruction cache unit (ICU) is a two-way set-associative 16KB cache memory unit with enhancements to support branch prediction and folding. The ICU is organized as 512 sets of 2 lines, each line containing 16 bytes. A separate bypass path is available to handle cache-inhibited instructions and to improve performance during line fill operations.

The cache can send two cached instructions per cycle to the execution unit, allowing instructions to be folded out of the queue without interrupting normal instruction flow. When a branch instruction is folded and executed in parallel with another instruction, the ICU provides two more instructions to replace both of the instructions just executed so that bandwidth is balanced between the ICU and the execution unit.

Data Cache Unit

The data cache unit is provided to minimize the access time of frequently used data items in main store. The 8KB cache is organized as a two-way set associative cache. There are 256 sets of 2 lines, each line containing 16 bytes of data. The cache features byte-writeability to improve the performance of byte and halfword store operations.

Cache operations are performed using a write-back strategy. A write-back cache only updates locations in main storage that corresponds to changed locations in the cache. Data is flushed from the cache to main storage whenever changed data needs to be removed from the cache to make room for other data.

The data cache may be disabled for a 128MB memory region via control bits in the data cache control register or on a per-page basis if the MMU is enabled for data translation. A separate bypass path is available to handle cache-inhibited data operations and to improve performance during line fill operations.

Cache flushing and filling are triggered by load, store, and cache control instructions executed by the processor. Cache blocks are loaded starting at the requested fullword, continuing to the end of the block and then wrapping around to fill the remaining fullwords at the beginning of the block.

DMA Controller

The four-channel DMA controller manages block data transfers in buffered, fly-by and memory-to-memory transfer modes with options for burst-mode operation. In fly-by and buffered modes, the DMA controller supports transactions between memory and peripheral devices.

Each DMA channel provides a control register, a source address register, a destination address register, a transfer count register, and a chained count register. Peripheral set-up cycles, wait cycles, and hold cycles can be programmed into each DMA channel control register. Each channel supports chaining operations. The DMA status register holds the status of all four channels.

Exception Handling

Table 2 summarizes the 403GCX exception priorities, types, and classes. Exceptions are generated by interrupts from internal and external peripherals, instructions, the internal timer facility, debug events or error conditions. Six external interrupt signals are provided on the 403GCX: one critical and five general-purpose, all individually maskable.

All exceptions fall into three basic classes: asynchronous imprecise exceptions, synchronous precise exceptions, and asynchronous precise exceptions. Asynchronous exceptions are caused by events external to processor execution, while synchronous exceptions are caused by instructions.

Except for a system reset or machine check, all 403GCX exceptions are handled precisely. Precise handling implies that the address of the excepting instruction (synchronous exceptions other than system call) or the address of the next sequential instruction (asynchronous exceptions and system call) is passed to the exception handling routine. Precise handling also implies that all instructions prior to the excepting instruction have completed execution and have written back their results.

Asynchronous imprecise exceptions include system resets and machine checks. Synchronous precise exceptions include most debug exceptions, program exceptions, data storage violations, TLB misses, system calls, and alignment error exceptions. Asynchronous precise exceptions include the critical interrupt exception, external interrupts, and internal timer facility exceptions and some debug events.

Only one exception is handled at a time. If multiple exceptions occur simultaneously, they are handled in priority order.

The 403GCX processes exceptions as reset, critical, or noncritical. Four exceptions are defined as critical: machine check exceptions, debug exceptions, exceptions caused by an active level on the critical interrupt pin, and the first time-out from the watchdog timer.

When a noncritical exception is taken, special purpose register Save/Restore 0 (SRR0) is loaded with the address of the excepting instruction (synchronous exceptions other than system call) or the next sequential instruction to be processed (asynchronous exceptions and system call). If the 403GCX is executing a multicycle instruction (load/store multiple, load/store string, multiply or divide), the instruction is terminated and its address stored in SRR0. Save/Restore Register 1 (SRR1) is loaded with the contents of the machine state register. The MSR is then updated to reflect the new context of the machine. The new MSR contents take effect beginning with the first instruction of the exception handling routine.

At the end of the exception handling routine, execution of a return from interrupt (rfi) instruction forces the contents of SRR0 and SRR1 to be loaded into the program counter and the MSR, respectively. Execution then begins at the address in the program counter.

The four critical exceptions are processed in a similar manner. When a critical exception is taken, SRR2 and SRR3 hold the next sequential address to be processed when returning from the exception and the contents of the machine state register, respectively. After the critical exception handling routine, return from critical interrupt (rfci) forces the contents of SRR2 and SRR3 to be loaded into the program counter and the MSR, respectively.

Timers

The 403GCX contains four timer functions: a time base, a programmable interval timer (PIT), a fixed interval timer (FIT), and a watchdog timer. The time base is a 64-bit counter incremented at the timer clock rate. The timer clock may be driven by either an internal signal equal to the processor clock rate or by a separate external timer clock pin. No interrupts are generated when the time base rolls over.

Table 2. 403GCX Exception Priorities, Types and Classes

Priority	Exception Type	Exception Class
1	System Reset	Asynchronous imprecise
2	Machine Check	Asynchronous imprecise
3	Debug	Synchronous precise (except UDE and EXC)
4	Critical Interrupt	Asynchronous precise
5	WatchdogTimer Time-out	Asynchronous precise
6	Program Exception, Data Storage Exception,TLB Miss, and System Calls	Synchronous precise
7	Alignment Exceptions	Synchronous precise
8	External Interrupts	Asynchronous precise
9	Fixed Interval Timer	Asynchronous precise
10	Programmable Interval Timer	Asynchronous precise

The programmable interval timer is a 32-bit register that is decremented at the same rate as the time base is incremented. The user preloads the PIT register with a value to create the desired delay. When the register is decremented to zeros, the timer stops decrementing, a bit is set in the timer status register (TSR), and a PIT interrupt is generated. Optionally, the PIT can be programmed to reload automatically the last value written to the PIT register, after which the PIT begins decrementing again.The timer control register (TCR) contains the interrupt enable for the PIT interrupt.

The fixed interval timer generates periodic interrupts based on selected bits in the time base. Users may select one of four intervals for the timer period by setting the correct bits in the TCR. When the selected bit in the time base changes from 0 to 1, a bit is set in the TSR and a FIT interrupt is generated. The FIT interrupt enable is contained in the TCR.

The watchdog timer generates a periodic interrupt based on selected bits in the time base. Users may select one of four time periods for the interval and the type of reset generated if the watchdog timer expires twice without an intervening clear from software. If enabled, the watchdog timer generates a system reset unless an exception handler updates the watchdog timer status bit before the timer has completed two of the selected timer intervals.

Serial Port

The 403GCX serial port is capable of supporting RS232 standard serial communication, as well as high-speed execution (bit speed at a maximum of one-sixteenth of the SysClk processor clock rate). The serial clock which drives the serial port can come from the internal SysClk or an external clock source at the external serial clock pin (maximum of one-half the SysClk rate).

The 403GCX serial port contains many features found only on advanced communications controllers, including the capability of being a peripheral for DMA transfers. An internal loopback mode supports diagnostic testing without requiring external hardware. An auto echo mode is included to retransmit received bits to the external device. Auto-resynchronization after a line break and false start bit detection are also provided, as well as operating modes that allow the serial port to react to handshaking line inputs or control handshaking line outputs without software interaction. Program generation mode allows the serial port transmitter to be used for pulse width modulation with duty cycle variation controlled by frame size, baud rate, and data pattern.

JTAG Port

The JTAG port has been enhanced to allow it to be used as a debug port. Through the JTAG test access port, debug software on a workstation or PC can single-step the processor and interrogate internal processor state to facilitate software debugging. The standard JTAG boundary-scan register allows testing of circuitry external to the chip, primarily the board interconnect. Alternatively, the JTAG bypass register can be selected when no other test data register needs to be accessed during a board-level test operation.

Real-Time Debug Port

The real-time debug port supports tracing the instruction stream being executed out of the instruction cache in real time. The trace status signals provide trace information while in real-time trace debug mode. This mode does not alter the performance of the processor.

P/N Code

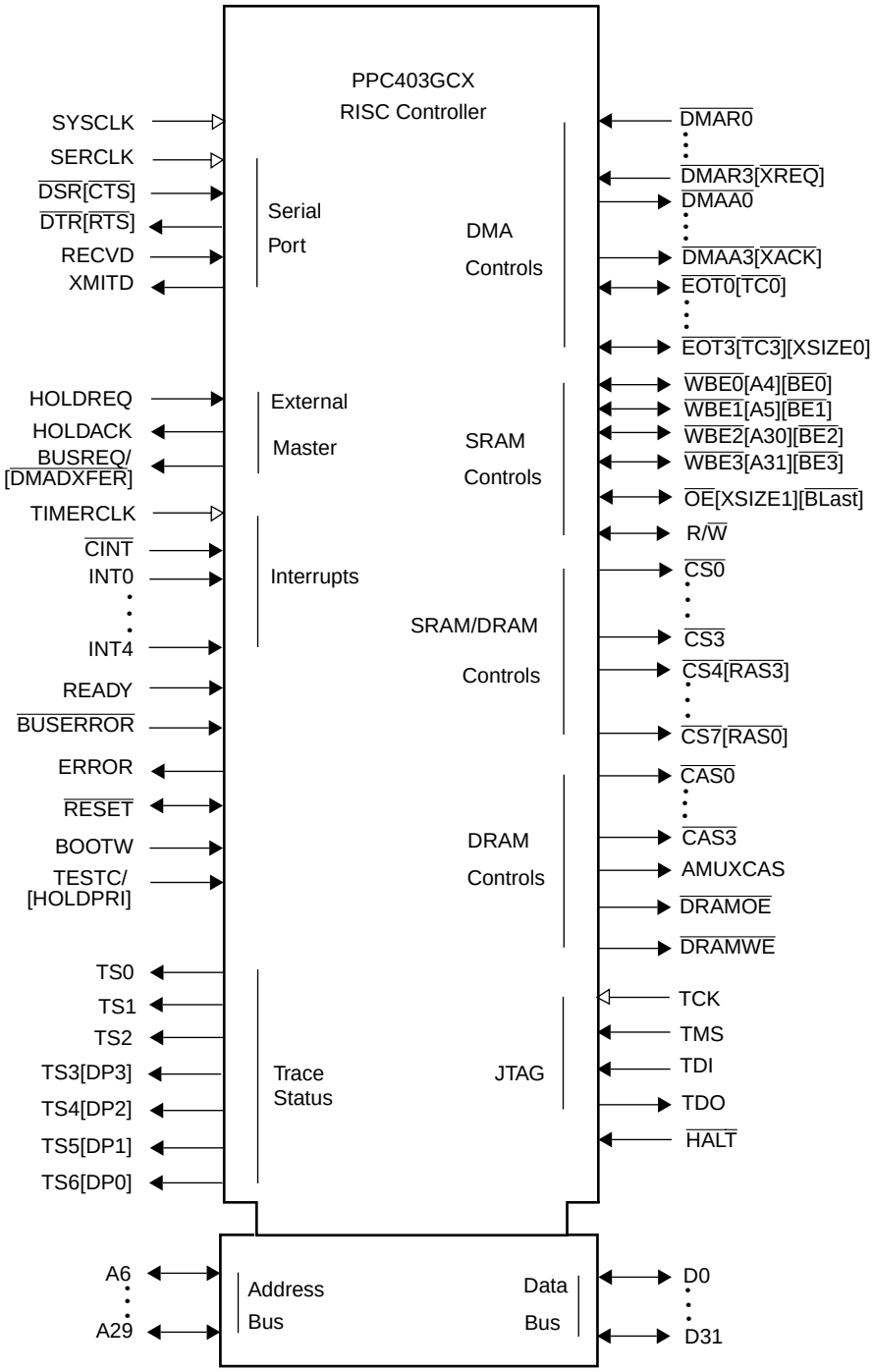
Table 3. PPC403GCX Part Number

MHz	Part Number	Package
76	403GCX-3JC76C2	PQFP

Note: The characters following the dash indicate reliability grade (3), package type (J), revision level (C), maximum internal CPU core clock rate (76), commercial version (C), and the ratio of internal CPU core clock rate to external bus speed (2 times the maximum external bus clock rate).

Logic Symbol

Signals in brackets are multiplexed.



Pin/Ball Functional Descriptions

Active-low signals are shown with overbars: $\overline{\text{DMAR0}}$. Multiplexed signals are alphabetized under the first (unmultiplexed) signal names on the same pins/balls. The logic symbol on the preceding page shows all 403GCX signals arranged by functional groups.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
A6	92	K12	I/O	Address Bus Bit 6. When the 403GCX is bus master, this is an address output from the 403GCX. When the 403GCX is not bus master, this is an address input from the external bus master, to determine bank register usage.
A7	93	K11	I/O	Address Bus Bit 7. See description of A6.
A8	94	J13	I/O	Address Bus Bit 8. See description of A6.
A9	95	J14	I/O	Address Bus Bit 9. See description of A6.
A10	96	J12	I/O	Address Bus Bit 10. See description of A6.
A11	97	J11	I/O	Address Bus Bit 11. See description of A6.
A12	98	H13	O	Address Bus Bit 12. When the 403GCX is bus master, this is an address output from the 403GCX.
A13	99	H14	O	Address Bus Bit 13. See description of A12.
A14	103	G14	O	Address Bus Bit 14. See description of A12.
A15	104	G13	O	Address Bus Bit 15. See description of A12.
A16	105	G11	O	Address Bus Bit 16. See description of A12.
A17	106	F14	O	Address Bus Bit 17. See description of A12.
A18	107	F12	O	Address Bus Bit 18. See description of A12.
A19	108	F13	O	Address Bus Bit 19. See description of A12.
A20	109	F11	O	Address Bus Bit 20. See description of A12.
A21	110	E14	O	Address Bus Bit 21. See description of A12.
A22	112	E13	I/O	Address Bus Bit 22. When the 403GCX is bus master, this is an address output from the 403GCX. When the 403GCX is not bus master, this is an address input from the external bus master, to determine page crossings.
A23	113	E11	I/O	Address Bus Bit 23. See description of A22.
A24	114	D14	I/O	Address Bus Bit 24. See description of A22.
A25	115	D12	I/O	Address Bus Bit 25. See description of A22.
A26	116	D13	I/O	Address Bus Bit 26. See description of A22.
A27	117	C14	I/O	Address Bus Bit 27. See description of A22.
A28	118	C12	I/O	Address Bus Bit 28. See description of A22.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
A29	119	C13	I/O	Address Bus Bit 29. See description of A22.
AMuxCAS	139	A8	O	DRAM External Address Multiplexer Select. AMuxCAS controls the select logic on an external multiplexer. If AMuxCAS is low, the multiplexer should select the row address for the DRAM and when AMuxCAS is 1, the multiplexer should select the column address.
BootW	11	E1	I	Boot-up ROM Width Select. BootW is sampled while the $\overline{\text{Reset}}$ pin is active and again after $\overline{\text{Reset}}$ becomes inactive to determine the width of the boot-up ROM. If this pin is tied to logic 0 when sampled on reset, an 8-bit boot width is assumed. If BootW is tied to 1, a 32-bit boot width is assumed. For 16-bit boot widths, this pin should be tied to the $\overline{\text{RESET}}$ pin.
$\overline{\text{BusError}}$	12	E3	I	Bus Error Input. A logic 0 input to the $\overline{\text{BusError}}$ pin by an external device signals to the 403GCX that an error occurred on the bus transaction. $\overline{\text{BusError}}$ is only sampled during the data transfer cycle or the last wait cycle of the transfer.
BusReq/ $\overline{\text{DMADXFER}}$	135	A9	O	Bus Request. While HoldAck is active, BusReq is active when the 403GCX has a bus operation pending and needs to regain control of the bus. DMA Data Transfer. When HoldAck is not active, $\overline{\text{DMADXFER}}$ indicates a valid data transfer cycle. For DMA use, $\overline{\text{DMADXFER}}$ controls burst-mode fly-by DMA transfers between memory and peripherals. $\overline{\text{DMADXFER}}$ is not meaningful unless a DMA Acknowledge signal ($\overline{\text{DMAA0:3}}$) is active. For transfer rates slower than one transfer per cycle, $\overline{\text{DMADXFER}}$ is active for one cycle when one transfer is complete and the next one starts. For transfer rates of one transfer per cycle, $\overline{\text{DMADXFER}}$ remains active throughout the transfer.
$\overline{\text{CAS0}}$	142	C8	O	DRAM Column Address Select 0. $\overline{\text{CAS0}}$ is used with byte 0 of all DRAM banks.
$\overline{\text{CAS1}}$	143	A7	O	DRAM Column Address Select 1. $\overline{\text{CAS1}}$ is used with byte 1 of all DRAM banks.
$\overline{\text{CAS2}}$	144	B7	O	DRAM Column Address Select 2. $\overline{\text{CAS2}}$ is used with byte 2 of all DRAM banks.
$\overline{\text{CAS3}}$	145	D7	O	DRAM Column Address Select 3. $\overline{\text{CAS3}}$ is used with byte 3 of all DRAM banks.
$\overline{\text{CINT}}$	36	L2	I	Critical Interrupt. To initiate a critical interrupt, the user must maintain a logic 0 on the $\overline{\text{CINT}}$ pin for a minimum of one SysClk clock cycle followed by a logic 1 on the $\overline{\text{CINT}}$ pin for at least one SysClk cycle.
$\overline{\text{CS0}}$	155	C4	O	SRAM Chip Select 0. Bank register 0 controls an SRAM bank, $\overline{\text{CS0}}$ is the chip select for that bank.
$\overline{\text{CS1}}$	154	A4	O	SRAM Chip Select 1. See description of $\overline{\text{CS0}}$ but controls bank 1.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
$\overline{CS2}$	153	D5	O	SRAM Chip Select 2. See description of $\overline{CS0}$ but controls bank 2.
$\overline{CS3}$	152	B5	O	SRAM Chip Select 3. See description of $\overline{CS0}$ but controls bank 3.
$\overline{CS4}/\overline{RAS3}$	151	C5	O	Chip Select 4/ DRAM Row Address Select 3. When bank register 4 is configured to control an SRAM bank, $\overline{CS4}/\overline{RAS3}$ functions as a chip select. When bank register 4 is configured to control a DRAM bank, $\overline{CS4}/\overline{RAS3}$ is the row address select for that bank.
$\overline{CS5}/\overline{RAS2}$	148	B6	O	Chip Select 5/ DRAM Row Address Select 2. See description of $\overline{CS4}/\overline{RAS3}$ but controls bank 5.
$\overline{CS6}/\overline{RAS1}$	147	C6	O	Chip Select 6/ DRAM Row Address Select 1. See description of $\overline{CS4}/\overline{RAS3}$ but controls bank 6.
$\overline{CS7}/\overline{RAS0}$	146	A6	O	Chip Select 7/ DRAM Row Address Select 0. See description of $\overline{CS4}/\overline{RAS3}$ but controls bank 7.
D0	42	N2	I/O	Data bus bit 0 (most significant bit).
D1	43	P2	I/O	Data bus bit 1.
D2	44	N3	I/O	Data bus bit 2.
D3	45	P3	I/O	Data bus bit 3.
D4	46	N4	I/O	Data bus bit 4.
D5	47	M4	I/O	Data bus bit 5.
D6	48	P4	I/O	Data bus bit 6.
D7	51	P5	I/O	Data bus bit 7.
D8	52	M5	I/O	Data bus bit 8.
D9	53	L5	I/O	Data bus bit 9.
D10	54	N6	I/O	Data bus bit 10.
D11	55	P6	I/O	Data bus bit 11.
D12	56	M6	I/O	Data bus bit 12.
D13	57	L6	I/O	Data bus bit 13.
D14	58	N7	I/O	Data bus bit 14.
D15	62	M7	I/O	Data bus bit 15.
D16	63	P8	I/O	Data bus bit 16.
D17	64	N8	I/O	Data bus bit 17.
D18	65	L8	I/O	Data bus bit 18.
D19	66	P9	I/O	Data bus bit 19.
D20	67	M9	I/O	Data bus bit 20.
D21	68	N9	I/O	Data bus bit 21.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
D22	71	M10	I/O	Data bus bit 22.
D23	72	N10	I/O	Data bus bit 23.
D24	73	L10	I/O	Data bus bit 24.
D25	74	P11	I/O	Data bus bit 25.
D26	75	M11	I/O	Data bus bit 26.
D27	76	N11	I/O	Data bus bit 27.
D28	77	P12	I/O	Data bus bit 28.
D29	78	M12	I/O	Data bus bit 29.
D30	79	N12	I/O	Data bus bit 30.
D31	82	N13	I/O	Data bus bit 31.
$\overline{\text{DMAA0}}$	156	B4	O	DMA Channel 0 Acknowledge. $\overline{\text{DMAA0}}$ has an active level when a transaction is taking place between the 403GCX and a peripheral.
$\overline{\text{DMAA1}}$	157	A3	O	DMA Channel 1 Acknowledge. See description of $\overline{\text{DMAA0}}$.
$\overline{\text{DMAA2}}$	158	C3	O	DMA Channel 2 Acknowledge. See description of $\overline{\text{DMAA0}}$.
$\overline{\text{DMAA3}}$/ $\overline{\text{XACK}}$	159	B3	O	DMA Channel 3 Acknowledge / External Master Transfer Acknowledge. When the 403GCX is bus master, this signal is DMAA3; see description of DMAA0. When the 403GCX is not the bus master, this signal is $\overline{\text{XACK}}$, an output from the 403GCX which has an active level when data is valid during an external bus master transaction.
$\overline{\text{DMAR0}}$	2	B2	I	DMA Channel 0 Request. External devices request a DMA transfer on channel 0 by putting a logic 0 on $\overline{\text{DMAR0}}$.
$\overline{\text{DMAR1}}$	3	B1	I	DMA Channel 1 Request. See description of $\overline{\text{DMAR0}}$.
$\overline{\text{DMAR2}}$	4	C2	I	DMA Channel 2 Request. See description of $\overline{\text{DMAR0}}$.
$\overline{\text{DMAR3}}$/ $\overline{\text{XREQ}}$	5	C1	I	DMA Channel 3 Request. When the 403GCX is the bus master, external devices request a DMA transfer on channel 3 by putting a logic 0 on $\overline{\text{DMAR3}}$. See description of $\overline{\text{DMAR0}}$. When the 403GCX is not the bus master, $\overline{\text{DMAR3}}$ is used as the $\overline{\text{XREQ}}$ input. The external bus master places a logic 0 on $\overline{\text{XREQ}}$ to initiate a transfer to the DRAM controlled by the 403GCX DRAM controller.
$\overline{\text{DRAMOE}}$	137	D9	O	DRAM Output Enable. $\overline{\text{DRAMOE}}$ has an active level when either the 403GCX or an external bus master is reading from a DRAM bank. This signal enables the selected DRAM bank to drive the data bus.
$\overline{\text{DRAMWE}}$	138	B8	O	DRAM Write Enable. $\overline{\text{DRAMWE}}$ has an active level when either the 403GCX or an external bus master is writing to a DRAM bank.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
$\overline{DSR}/\overline{CTS}$	28	J2	I	Data Set Ready / Clear to Send. The function of this pin as either $\overline{DSR}$ or $\overline{CTS}$ is selectable via the Serial Port Configuration bit in the IOCR.
$\overline{DTR}/\overline{RTS}$	88	L14	O	Data Terminal Ready / Request to Send. The function of this pin as either $\overline{DTR}$ or $\overline{RTS}$ is selectable via the Serial Port Configuration bit in the IOCR.
$\overline{EOT0}/\overline{TC0}$	128	A11	I/O	End of Transfer 0 / Terminal Count 0. The function of the $\overline{EOT0}/\overline{TC0}$ is controlled via the $\overline{EOT}/\overline{TC}$ bit in the DMA Channel 0 Control Register. When $\overline{EOT0}/\overline{TC0}$ is configured as an End of Transfer pin, external users may stop a DMA transfer by placing a logic 0 on this input pin. When configured as a Terminal Count pin, the 403GCX signals the completion of a DMA transfer by placing a logic 0 on this pin.
$\overline{EOT1}/\overline{TC1}$	131	A10	I/O	End of Transfer 1 / Terminal Count 1. See description of $\overline{EOT0}/\overline{TC0}$.
$\overline{EOT2}/\overline{TC2}$	132	C10	I/O	End of Transfer 2 / Terminal Count 2. See description of $\overline{EOT0}/\overline{TC0}$.
$\overline{EOT3}/\overline{TC3}$/ XSize0	133	D10	I/O	End of Transfer 3 / Terminal Count 3 / External Master Transfer Size 0. When the 403GCX is bus master, this pin has the same function as $\overline{EOT0}/\overline{TC0}$. When the 403GCX is not bus master, $\overline{EOT3}/\overline{TC3}$/XSize0 is used as one of two external transfer size input bits, XSize0:1.
Error	136	C9	O	System Error. Error goes to a logic 1 whenever a machine check error is detected in the 403GCX. The Error pin then remains a logic 1 until the machine check error is cleared in the Exception Syndrome Register and/or Bus Error Syndrome Register.
GND	1	G7		Ground. All ground pins must be used.
	10	E2		Ground. All ground pins must be used.
	15	F1		Ground. All ground pins must be used.
	29	J4		Ground. All ground pins must be used.
	30	K1		Ground. All ground pins must be used.
	41	H7		Ground. All ground pins must be used.
	50	N5		Ground. All ground pins must be used.
	59	P7		Ground. All ground pins must be used.
	60	L7		Ground. All ground pins must be used.
	70	P10		Ground. All ground pins must be used.
	81	H8		Ground. All ground pins must be used.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
GND	90	K13		Ground. All ground pins must be used.
	101	G12		Ground. All ground pins must be used.
	102	H12		Ground. All ground pins must be used.
	111	E12		Ground. All ground pins must be used.
	121	G8		Ground. All ground pins must be used.
	130	B10		Ground. All ground pins must be used.
	141	C7		Ground. All ground pins must be used.
	150	A5		Ground. All ground pins must be used.
$\overline{\text{Halt}}$	9	D4	I	Halt from external debugger, active low.
HoldAck	134	B9	O	Hold Acknowledge. HoldAck outputs a logic 1 when the 403GCX relinquishes its external buses to an external bus master. HoldAck outputs a logic 0 when the 403GCX regains control of the bus.
HoldReq	14	F2	I	Hold Request. External bus masters can request the 403GCX bus by placing a logic1 on this pin. The external bus master relinquishes the bus to the 403GCX by deasserting HoldReq.
INT0	31	K3	I	Interrupt 0. INT0 is an interrupt input to the 403GCX and users may program the pin to be either edge-triggered or level-triggered and may also program the polarity to be active high or active low. The IOCR contains the bits necessary to program the trigger type and polarity.
INT1	32	K2	I	Interrupt 1. See description of INT0.
INT2	33	K4	I	Interrupt 2. See description of INT0.
INT3	34	L1	I	Interrupt 3. See description of INT0.
INT4	35	L3	I	Interrupt 4. See description of INT0.
IVR	39	M2	I	Reserved for manufacturing test. Tied high for normal operation.
$\overline{\text{OE}}$/XSize1/ $\overline{\text{BLast}}$	126	B11	O/I/O	Output Enable / External Master Transfer Size 1. When the 403GCX is bus master, $\overline{\text{OE}}$ enables the selected SRAMs to drive the data bus. The timing parameters of $\overline{\text{OE}}$ relative to the chip select, $\overline{\text{CS}}$, are programmable via bits in the 403GCX bank registers. When the 403GCX is not bus master, $\overline{\text{OE}}$/XSize1 is used as one of two external transfer size input bits, XSize0:1. In Byte Enable mode, Burst Last ($\overline{\text{BLast}}$) goes active to indicate the last transfer of a memory access, whether burst or nonburst.
Ready	13	E4	I	Ready. Ready is used to insert externally generated (device-paced) wait states into bus transactions. The Ready pin is enabled via the Ready Enable bit in 403GCX bank registers.
RecvD	27	J3	I	Serial Port Receive Data.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
$\overline{\text{Reset}}$	91	K14	I/O	$\overline{\text{Reset}}$. A logic 0 input placed on this pin for one SysClk cycle causes the 403GCX to begin a system reset. When a system reset is invoked, the $\overline{\text{Reset}}$ pin becomes a logic 0 output for 2048 SysClk cycles.
R/$\overline{\text{W}}$	127	C11	I/O	Read / Write. When the 403GCX is bus master, R/$\overline{\text{W}}$ is an output which is high when data is read from memory and low when data is written to memory. When the 403GCX is not bus master, R/$\overline{\text{W}}$ is an input from the external bus master which indicates the direction of data transfer.
SerClk	26	J1	I	Serial Port Clock. Through the Serial Port Clock Source bit in the Input/Output Configuration register (IOCR), users may choose the serial port clock source from either the input on the SerClk pin or processor SysClk. The maximum allowable input frequency into SerClk is half the SysClk frequency.
SysClk	22	G3	I	SysClk is the processor system clock input. The 403GCX can also be programmed to operate at a 2X internal clock rate while the external bus interface runs at the SysClk input rate.
TCK	6	D2	I	JTAG Test Clock Input. TCK is the clock source for the 403GCX test access port (TAP). The maximum clock rate into the TCK pin is one half of the processor SysClk clock rate.
TDI	8	D1	I	Test Data In. The TDI is used to input serial data into the TAP. When the TAP enables the use of the TDI pin, the TDI pin is sampled on the rising edge of TCK and this data is input to the selected TAP shift register.
TDO	16	F3	O	Test Data Output. TDO is used to transmit data from the 403GCX TAP. Data from the selected TAP shift register is shifted out on TDO.
TestA	23	H1	I	Reserved for manufacturing test. Tied low for normal operation.
$\overline{\text{TestB}}$	24	H2	I	Reserved for manufacturing test. Tied high for normal operation.
TestC/Hold-Pri	37	M1	I	TestC. Reserved for manufacturing test during the reset interval. While Reset is active, this signal should be tied low for normal operation. HoldReq Priority. When Reset is not active, this signal is sampled to determine the priority of the external bus master signal HoldReq. If HoldPri = 0 then the HoldReq signal is considered high priority, otherwise HoldReq is considered low priority.
TestD	38	M3	I	Reserved for manufacturing test. Tied low for normal operation.
TimerClk	25	H4	I	Timer Facility Clock. Through the Timer Clock Source bit in the Input/Output Configuration register (IOCR), users may choose the clock source for the Timer facility from either the input on the TimerClk pin or processor CoreClk. The maximum input frequency into TimerClk is half the CoreClk frequency.

Table 4. 403GCX Signal Descriptions

Signal Name	Pin	Ball	I/O Type	Function
TMS	7	D3	I	Test Mode Select. The TMS pin is sampled by the TAP on the rising edge of TCK. The TAP state machine uses the TMS pin to determine the mode in which the TAP operates.
TS0	17	F4	O	Trace Status 0.
TS1	18	G2	O	Trace Status 1.
TS2	19	G1	O	Trace Status 2.
TS3/DP3	86	L13	O/I/O	Trace Status 3 / Data Parity 3. When parity checking and generation are enabled, this signal represents odd parity for read/write operations using byte 3 (D24:31) of the data bus. The Parity Error status bit is set in the BESR when a parity error is detected.
TS4/DP2	85	M14	O/I/O	Trace Status 4 / Data Parity 2 for byte 2 (D16:23). See TS3/DP3 description above.
TS5/DP1	84	M13	O/I/O	Trace Status 5 / Data Parity 1 for byte 1 (D8:15). See TS3/DP3 description above.
TS6/DP0	83	N14	O/I/O	Trace Status 6 / Data Parity 0 for byte 0 (D0:7). See TS3/DP3 description above.
V_{DD}	20	G4		Power. All power pins must be connected to 3.3V supply.
	21	H3		Power. All power pins must be connected to 3.3V supply.
	40	N1		Power. All power pins must be connected to 3.3V supply.
	49	L4		Power. All power pins must be connected to 3.3V supply.
	61	M8		Power. All power pins must be connected to 3.3V supply.
	69	L9		Power. All power pins must be connected to 3.3V supply.
	80	P13		Power. All power pins must be connected to 3.3V supply.
	89	L11		Power. All power pins must be connected to 3.3V supply.
	100	H11		Power. All power pins must be connected to 3.3V supply.
	120	B14		Power. All power pins must be connected to 3.3V supply.
	129	D11		Power. All power pins must be connected to 3.3V supply.
	140	D8		Power. All power pins must be connected to 3.3V supply.
	149	D6		Power. All power pins must be connected to 3.3V supply.
	160	A2		Power. All power pins must be connected to 3.3V supply.

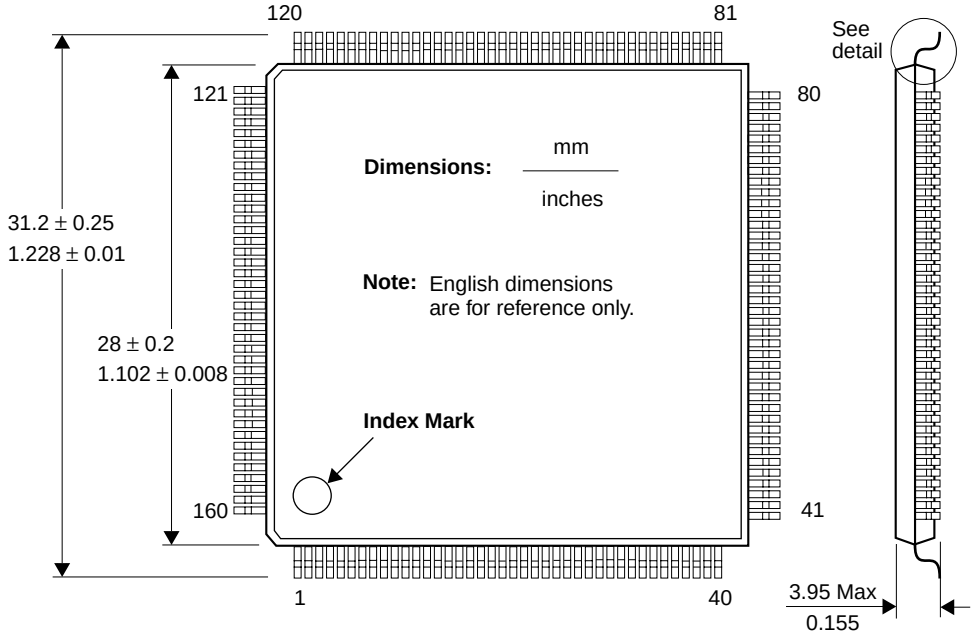
Table 4. 403GCX Signal Descriptions

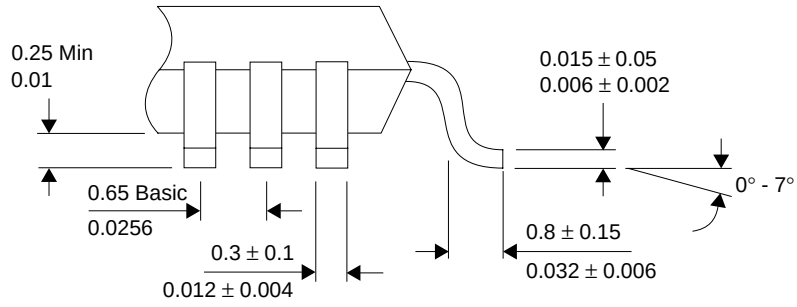
Signal Name	Pin	Ball	I/O Type	Function
$\overline{\text{WBE0}}$/A4/ $\overline{\text{BE0}}$	122	B13	O/I/O	Write Byte Enable 0 / Address Bus Bit 4 / Byte Enable 0. When the 403GCX is bus master, the write byte enable outputs, $\overline{\text{WBE0:3}}$, select the active byte(s) in a memory write access to SRAM. The byte enables can also be programmed as read/write byte enables, depending on the mode set in the IOCR. Note 5 on page 35 summarizes the functional and timing differences in these signals when programmed as read/write byte enables. For 8-bit memory regions, $\overline{\text{WBE2}}$ and $\overline{\text{WBE3}}$ become address bits 30 and 31 and $\overline{\text{WBE0}}$ is the byte-enable line. For 16-bit memory regions, $\overline{\text{WBE2}}$ and $\overline{\text{WBE3}}$ become address bits 30 and 31 and $\overline{\text{WBE0}}$ and $\overline{\text{WBE1}}$ are the high byte and low byte enables, respectively. For 32-bit memory regions, $\overline{\text{WBE0:3}}$ are byte enables for bytes 0-3 on the data bus, respectively. When the 403GCX is not bus master, $\overline{\text{WBE0:1}}$ are used as the A4:5 inputs (for bank register selection) and $\overline{\text{WBE2:3}}$ are used as the A30:31 inputs (for byte selection and page crossing detection).
$\overline{\text{WBE1}}$/A5/ $\overline{\text{BE1}}$	123	A13	O/I/O	Write Byte Enable 1 / Address Bus Bit 5 / Byte Enable 1. See description of $\overline{\text{WBE0}}$ / A4 above.
$\overline{\text{WBE2}}$/A30/ $\overline{\text{BE2}}$	124	B12	O/I/O	Write Byte Enable 2 / Address Bus Bit 30 / Byte Enable 2. See description of $\overline{\text{WBE0}}$ / A4 above.
$\overline{\text{WBE3}}$/A31/ $\overline{\text{BE3}}$	125	A12	O/I/O	Write Byte Enable 3 / Address Bus Bit 31 / Byte Enable 3. See description of $\overline{\text{WBE0}}$ / A4 above.
XmitD	87	L12	O	Serial port transmit data.

Table 5. PQFP Package Signals Ordered by Pin Number

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	GND	33	INT2	65	D18	97	A11	129	V_{DD}
2	$\overline{\text{DMAR0}}$	34	INT3	66	D19	98	A12	130	GND
3	$\overline{\text{DMAR1}}$	35	INT4	67	D20	99	A13	131	$\overline{\text{EOT1}}/\overline{\text{TC1}}$
4	$\overline{\text{DMAR2}}$	36	$\overline{\text{CINT}}$	68	D21	100	V_{DD}	132	$\overline{\text{EOT2}}/\overline{\text{TC2}}$
5	$\overline{\text{DMAR3}}/\overline{\text{XREQ}}$	37	TestC/HoldPri	69	V_{DD}	101	GND	133	$\overline{\text{EOT3}}/\overline{\text{TC3}}$/XSize0
6	TCK	38	TestD	70	GND	102	GND	134	HoldAck
7	TMS	39	IVR	71	D22	103	A14	135	BusReq/ $\overline{\text{DMADXFER}}$
8	TDI	40	V_{DD}	72	D23	104	A15	136	Error
9	$\overline{\text{Halt}}$	41	GND	73	D24	105	A16	137	$\overline{\text{DRAMOE}}$
10	GND	42	D0	74	D25	106	A17	138	$\overline{\text{DRAMWE}}$
11	BootW	43	D1	75	D26	107	A18	139	AMuxCAS
12	$\overline{\text{BusError}}$	44	D2	76	D27	108	A19	140	V_{DD}
13	Ready	45	D3	77	D28	109	A20	141	GND
14	HoldReq	46	D4	78	D29	110	A21	142	$\overline{\text{CAS0}}$
15	GND	47	D5	79	D30	111	GND	143	$\overline{\text{CAS1}}$
16	TDO	48	D6	80	V_{DD}	112	A22	144	$\overline{\text{CAS2}}$
17	TS0	49	V_{DD}	81	GND	113	A23	145	$\overline{\text{CAS3}}$
18	TS1	50	GND	82	D31	114	A24	146	$\overline{\text{CS7}}/\overline{\text{RAS0}}$
19	TS2	51	D7	83	TS6/DP0	115	A25	147	$\overline{\text{CS6}}/\overline{\text{RAS1}}$
20	V_{DD}	52	D8	84	TS5/DP1	116	A26	148	$\overline{\text{CS5}}/\overline{\text{RAS2}}$
21	V_{DD}	53	D9	85	TS4/DP2	117	A27	149	V_{DD}
22	SysClk	54	D10	86	TS3/DP3	118	A28	150	GND
23	TestA	55	D11	87	XmitD	119	A29	151	$\overline{\text{CS4}}/\overline{\text{RAS3}}$
24	$\overline{\text{TestB}}$	56	D12	88	$\overline{\text{DTR}}/\overline{\text{RTS}}$	120	V_{DD}	152	$\overline{\text{CS3}}$
25	TimerClk	57	D13	89	V_{DD}	121	GND	153	$\overline{\text{CS2}}$
26	SerClk	58	D14	90	GND	122	$\overline{\text{WBE0}}$/A4/$\overline{\text{BE0}}$	154	$\overline{\text{CS1}}$
27	RecvD	59	GND	91	$\overline{\text{Reset}}$	123	$\overline{\text{WBE1}}$/A5/$\overline{\text{BE1}}$	155	$\overline{\text{CS0}}$
28	$\overline{\text{DSR}}/\overline{\text{CTS}}$	60	GND	92	A6	124	$\overline{\text{WBE2}}$/A30/$\overline{\text{BE2}}$	156	$\overline{\text{DMAA0}}$
29	GND	61	V_{DD}	93	A7	125	$\overline{\text{WBE3}}$/A31/$\overline{\text{BE3}}$	157	$\overline{\text{DMAA1}}$
30	GND	62	D15	94	A8	126	$\overline{\text{OE}}$/XSize1/ $\overline{\text{BLast}}$	158	$\overline{\text{DMAA2}}$
31	INT0	63	D16	95	A9	127	R/$\overline{\text{W}}$	159	$\overline{\text{DMAA3}}/\overline{\text{XACK}}$
32	INT1	64	D17	96	A10	128	$\overline{\text{EOT0}}/\overline{\text{TC0}}$	160	V_{DD}

PQFP Mechanical Drawing (Top View)





Package Thermal Specifications

The 403GCX is designed to operate within the case temperature range from -40˚C to 120˚C. Thermal resistance values are shown in Table 6:

Table 6. Thermal Resistance (˚C/Watt)

Parameter	Airflow-ft/min (m/sec)		
	0 (0)	100 (0.51)	200 (1.02)
θ_{JC} Junction to case	2	2	2
θ_{CA} Case to ambient PQFP (no heatsink)	37.2	31.6	29.8

Notes:
1. Case temperature Tm_C is measured at top center of case surface with device soldered to circuit board.
2. $Tm_A = Tm_C - P \times \theta_{CA}$, where Tm_A is ambient temperature.
3. $Tm_{CMax} = Tm_{JMax} - P \times \theta_{JC}$, where Tm_{JMax} is maximum junction temperature and P is power consumption.
4. The above assumes that the chip is mounted on a card with at least one signal and two power planes.

Electrical Specifications

Absolute Maximum Ratings

The absolute maximum ratings in Table 7 below are stress ratings only. Operation at or beyond these maximum ratings may cause permanent damage to the device.

Table 7. 403GCX Maximum Ratings

Parameter	Maximum Rating
Supply voltage with respect to GND	-0.5V to +3.8V
Voltage on other pins with respect to GND	-0.5V to +5.5V
Case temperature under bias	-40˚C to +120˚C
Storage temperature	-65˚C to +150˚C

Operating Conditions

The 403GCX can interface to either 3V or 5V technologies. The range for supply voltages is specified for five-percent margins relative to a nominal 3.3V power supply.

Device operation beyond the conditions specified in Table 8 is not recommended. Extended operation beyond the recommended conditions may affect device reliability:

Table 8. Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage: 403GCX-3JC76	3.14	3.47	V
F_C	Clock frequency[1]: 403GCX-3JC76	24	38	MHz
Tm_C	Case temperature under bias: 403GCX-3JC76	-40	85	°C

Note:

These frequencies do not account for T_{CS}. See Table 11.

Power Considerations

Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements. Typical power dissipation is 0.49 W at 38/76 MHz, with an average 50pF capacitive load.

Derating curves are provided in the section, "Output Derating for Capacitance and Voltage," on page 29.

Recommended Connections

Power and ground pins should all be connected to separate power and ground planes in the circuit board to which the 403GCX is mounted. Unused input pins must be tied inactive, either high or low.

The IVR pin should be tied to V_{DD} for normal operation.

DC Specifications

Table 9. 403GCX DC Characteristics

Symbol	Parameter	Min	Max	Units
V_{IL}	Input low voltage (except for SysClk)	GND - 0.1	0.8	V
V_{ILC}	Input low voltage for SysClk	GND - 0.1	0.8	V
V_{IH}	Input high voltage (except for SysClk)	2.0	5.1	V
V_{IHC}	Input high voltage for SysClk	2.0	5.1	V
V_{OL}	Output low voltage		0.4	V
V_{OH}	Output high voltage	2.4	V_{DD}	V
I_{OH}	Output high current		2	mA
I_{OL}	Output low current		4	mA
I_{LI}	Input leakage current[3]		150	µA
I_{LO}	Output leakage current		10	µA
I_{CC}	Supply current ($I_{CC\ Max}$ at F_{Core} of 76MHz)		305	mA

Notes:
1. The 403GCX drives its outputs to the level of V_{DD} and, when not driving, the 403GCX outputs can be pulled up to 5V by other devices in a system.
2. $I_{CC\ Max}$ is measured at worst-case recommended operating conditions for temperature, frequency and voltage as specified in Table 8 on page 20, and a capacitive load of 50 pF.
3. The Input leakage current is dependent on the applied. See "Input Leakage Current," on page 32 for details.

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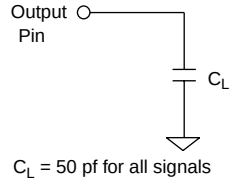
Table 10. 403GCX I/O Capacitance

Symbol	Parameter	Min	Max	Units
C_{IN}	Input capacitance (except for SysClk)		5	pF
C_{INC}	Input capacitance for SysClk		15	pF
C_{OUT}	Output capacitance[1]		7	pF
$C_{I/O}$	I/O pin capacitance		8	pF

Note:
1. C_{Out} is specified as the load capacitance of a floating output in high impedance.

AC Specifications

Clock timing and switching characteristics are specified in accordance with recommended operating conditions in Table 8 on page 20. AC specifications are characterized at V_{DD} = 3.14V and T_J = 85˚C with the 50pF test load shown in the figure at right. Derating of outputs for capacitive loading is shown in the figure "Output Derating for Capacitance and Voltage," on page 29.



SysClk Timing

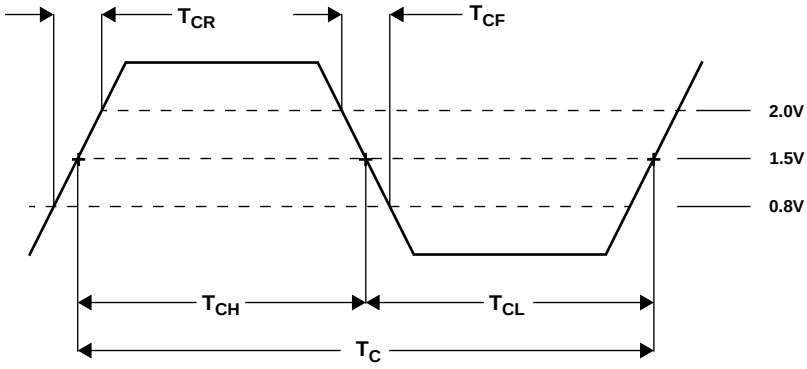


Table 11. 403GCX System Clock Timing

Symbol	Parameter	38 MHz		Units
		Min	Max	
F_C	SysClk clock input frequency[1]	24	38	MHz
T_C	SysClk clock period[1]	27.8	41.7	ns
T_{CS}	Clock edge stability[2]		0.2	ns
T_{CH}	Clock input high time	11		ns
T_{CL}	Clock input low time	11		ns
T_{CR}	Clock input rise time[3]	0.5	2.5	ns
T_{CF}	Clock input fall time[3]	0.5	2.5	ns

Notes:
1. These values do not include the allowable tolerance for clock edge instability represented by T_{CS}.
2. Cycle-to-cycle jitter allowed between any two edges.
3. Rise and fall times measured between 0.8V and 2.0V.

Serial Clock Timing Characteristics

Table 12. 403GCX Serial Clock Timings

Symbol	Parameter	Min	Max	Units
F_{SC}	SerClk input frequency		0.5 F_C	MHz
T_{SC}	SerClk period	2T_C		ns
T_{SCH}	SerClk input high time	T_C		ns
T_{SCL}	SerClk input low time	T_C		ns

Timer Clock Timing Characteristics

Table 13. 403GCX Timer Clock Timings

Symbol	Parameter	IOCR[2xC] = 1 CoreClk Doubled Mode		IOCR[2xC] = 0 CoreClk Non-Doubled Mode		Units
		Min	Max	Min	Max	
F_{TC}	TimerClk input frequency		F_C		0.5 F_C	MHz
T_{TC}	TimerClk period	T_C		2 T_C		ns
T_{TCH}	TimerClk input high time	0.5 T_C		T_C		ns
T_{TCL}	TimerClk input low time	0.5 T_C		T_C		ns

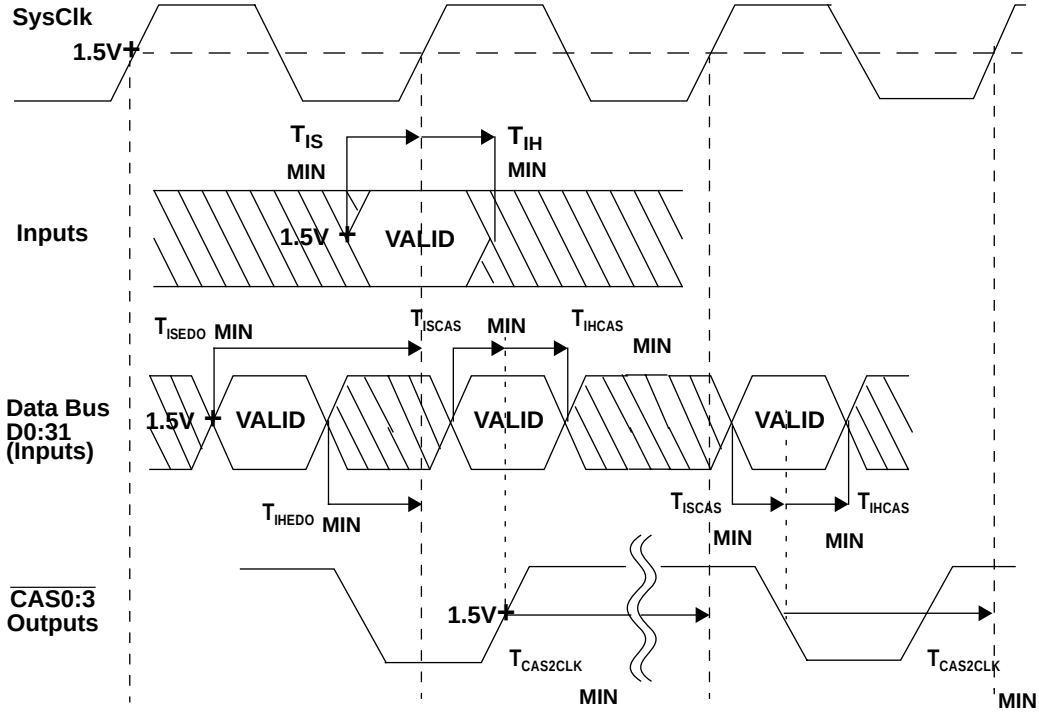
Table 14. 403GCX Serial Port Output Timings

Symbol	Parameter		38 MHz		Units
			T_{OHMin}	T_{OVMax}	
T_{OH}, T_{OV}	Output hold, output valid				
	T_{OHSP1}, T_{OVSP1}	$\overline{DTR}/\overline{RTS}$		12	ns
	T_{OHSP2}, T_{OVSP2}	$\overline{XmitD}$		10	

Note:

1. Output times are measured with a standard 50 pF capacitive load, unless otherwise noted.

Input Setup and Hold Waveform



Notes:

1. The 403GCX may be programmed to latch data from the data bus with respect to SysClk, or with respect to $\overline{CAS}$. When IOCR[DRC] = 1, the 403GCX is programmed to latch data on the rise of $\overline{CAS}$. When IOCR[EDO] = 1, the 403GCX is programmed to latch data on either the fall of $\overline{CAS}$ or the fall of the internal duty cycle corrected SysClk, depending on the parameters set in the bank register and the type of transfer. When neither of these special modes are set, the 403GCX will latch data on the rise of SysClk. Note that it is invalid to concurrently set IOCR[DRC] = 1 and IOCR[EDO] = 1.
2. $T_{CAS2CLK} \geq 13.5$ ns. When IOCR[DRC] = 1 or IOCR[EDO] = 1, the capacitive load on the $\overline{CAS}$ outputs must not delay the $\overline{CAS}$ transition such that the period from the $\overline{CAS}$ data latching edge to the next SysClk rising edge becomes less than 13.5 ns. The maximum value of $\overline{CAS}$ capacitive loading can be determined by using the output time for $\overline{CAS}$ from Table 17 on page 27, and applying the appropriate derating factor for your application. See the figure, "Output Derating for Capacitance and Voltage," on page 29.

All T_{IS} and T_{IH} timings in Table 15 are specified with respect to the rise of the external SysClk signal. Internal system clocks are duty-cycle corrected so the falling edge of the external SysClk signal may not be the same as the falling edge of the internally corrected system clock.

Table 15. 403GCX Synchronous Input Timings

Symbol	Parameter		38 MHz Min	38 MHz Max	Units
T_{IS}	Input setup:				
	T_{IS1}	A4:11,A22:31	3		
	T_{IS2}	$\overline{\text{BusError}}$	5		
	T_{IS3}	D0:31 (to SysClk)[3]	4		
	T_{ISEDO}	D0:31 (to SysClk)[4,5]	16.2		
	T_{ISCAS}	D0:31 (to $\overline{\text{CAS}}$)[5]	3		
	T_{IS4}	HoldPri	3		ns
	T_{IS5}	HoldReq	3		
	T_{IS6}	R/$\overline{\text{W}}$	3		
	T_{IS7}	Ready	5		
	T_{IS8}	Ready(SOR mode)	10		
	T_{IS9}	$\overline{\text{XReq}}$	4		
	T_{IS10}	XSize0:1	3		
T_{IH}	Input hold:				
	T_{IH1}	A4:11,A22:31	2		
	T_{IH2}	$\overline{\text{BusError}}$	2		
	T_{IH3}	D0:31 (after SysClk)[3]	3		
	T_{IHEDO}	D0:31 (after SysClk)[4,5]	-10.2		
	T_{IHCAS}	D0:31 (after $\overline{\text{CAS}}$)[5]	3		
	T_{IH4}	HoldPri	2		ns
	T_{IH5}	HoldReq	2		
	T_{IH6}	R/$\overline{\text{W}}$	2		
	T_{IH7}	Ready	2		
	T_{IH8}	Ready(SOR mode)	2		
	T_{IH9}	$\overline{\text{XReq}}$	2		
	T_{IH10}	XSize0:1	2		
T_R,T_F	Input rise/fall time		0.5	2.5	ns

Notes:

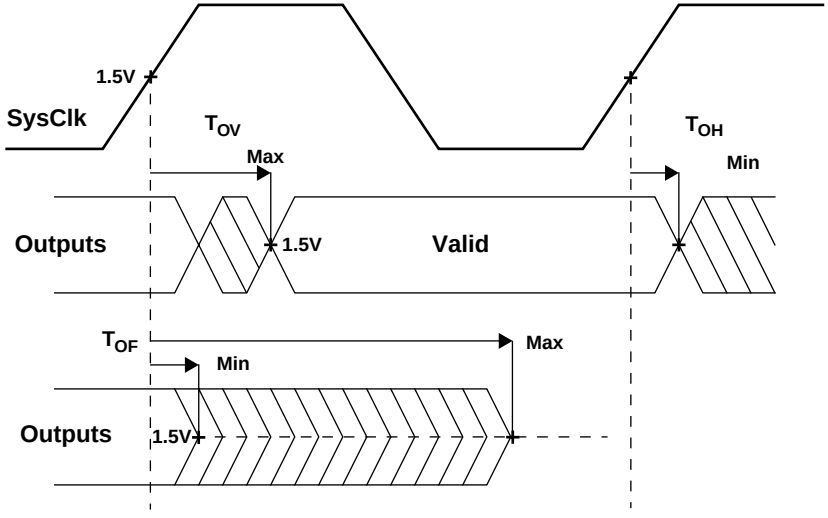
1. Parity setup and hold times are the same as for the data bus.
2. For detailed EDO DRAM timing waveforms, refer to "EDO DRAM 2-1-1-1 Burst Read Followed by Single Transfer Read," on page 42 and "EDO DRAM 3-1-1-1 Burst Read Followed by Single Transfer Read," on page 44.
3. Data bus input setup and hold times T_{IS3} and T_{IH3} are the specifications to use for all modes except DRAM Read on CAS and EDO DRAM read modes (controlled via IOCR[DRC] and IOCR[EDO], respectively).
4. In EDO mode, the data bus input setup and hold times with respect to SysClk. Use the following equations to determine the minimum input setup and hold times for this signal: $T_{ISEDO}Min = Tc/2 + 3$; $T_{IHEDO}Min = -Tc/2 + 3$. Valid for Tc greater than 25ns and less than 41.7 ns.
5. Guaranteed by design and not tested.

Table 16. 403GCX Asynchronous Input Timings

Symbol	Parameter		38 MHz Min	38 MHz Max	Units
T_{IS}	Input setup time				
	T_{IS11}	$\overline{CINT}$	3		ns
	T_{IS12}	$\overline{DMAR0:3}$	3		
	T_{IS13}	$\overline{EOT0:3}$	3		
	T_{IS14}	$\overline{HALT}$	3		
	T_{IS15}	INT0:4	4		
	T_{IS16}	$\overline{Reset}$	8		
	T_{IS17}	Ready	5		
T_{IH}	Input hold time				
	T_{IH11}	$\overline{CINT}$	T_C		
	T_{IH12}	$\overline{DMAR0:3}$	T_C		
	T_{IH13}	$\overline{EOT0:3}$	T_C		
	T_{IH14}	$\overline{HALT}$	T_C		
	T_{IH15}	INT0:4	T_C		
	T_{IH16}	$\overline{Reset}$	Note 1,2		
	T_{IH17}	Ready	T_C		

Notes:
1. During a system-initiated reset, $\overline{Reset}$ must be taken low for a minimum of 2048 SysClk cycles.
2. The BootW input has a maximum rise time requirement of 10 ns when it is tied to $\overline{Reset}$.
3. Input hold times are measured at 3.47V and $T_J = 0^{\circ}C$.

Output Delay and Float Timing Waveform



All T_{OH} and T_{OV} timings in Table 17 are specified with respect to the rise of the SysClk input signal. Internal system clocks are duty-cycle corrected so the falling edge of the external SysClk signal may not be the same as the falling edge of the internally corrected system clock. T_{OHxr}/T_{OVxr} specifications are for signals which transition relative to the rising edge of SysClk, while T_{OHxf}/T_{OVxf} apply to falling edge transitions. Refer to the appropriate timing diagram to determine the appropriate clock edge for signal transitions.

Table 17. 403GCX Synchronous Output Timings

Symbol	Parameter		38 MHz		Units
			T_{OHMin}	T_{OVMax}	
T_{OH}, T_{OV}	Output hold, output	valid			
	T_{OH1r}, T_{OV1r}	A6:31	3	10	ns
	T_{OH1f}, T_{OV1f}	A6:31[2,3,8]	16.2	23.2	
	T_{OH2}, T_{OV2}	AMuxCAS	3	9	
	T_{OH3}, T_{OV3}	BusReq	3	9	
	T_{OH4r}, T_{OV4r}	$\overline{CAS0:3}$[8]	3	9	
	T_{OH4f}, T_{OV4f}	$\overline{CAS0:3}$[2,3]	16.2	22.3	
	T_{OH5}, T_{OV5}	$\overline{CS0:7}$	3	9	
	T_{OH6}, T_{OV6}	D0:31	3	12	
	T_{OH7}, T_{OV7}	$\overline{DMAA0:3}$	3	9	
	T_{OH8}, T_{OV8}	$\overline{DMADXFER}$	3	10	
	T_{OH9r}, T_{OV9r}	$\overline{DRAMOE}$	3	9	
	T_{OH9f}, T_{OV9f}	$\overline{DRAMOE}$[2,3,8]	16.2	23.2	
	T_{OH10}, T_{OV10}	$\overline{DRAMWE}$	3	9	
	T_{OH11}, T_{OV11}	Error	3	10	
	T_{OH12}, T_{OV12}	HoldAck	3	9	
	T_{OH13}, T_{OV13}	$\overline{OE}$	3	10	
	T_{OH14r}, T_{OV14r}	$\overline{RAS0:3}$(turn-off)[8]	3	9	
	T_{OH14f}, T_{OV14f}	$\overline{RAS0:3}$(turn-on)[3]	16.2	23.2	
	T_{OH15}, T_{OV15}	$\overline{RAS0:3}$(Early, turn-on)[4]	10	16.9	
	T_{OH16}, T_{OV16}	$\overline{Reset}$	2	10	
	T_{OH17}, T_{OV17}	R/$\overline{W}$	3	9	
	T_{OH18}, T_{OV18}	$\overline{TC0:3}$	3	10	
	T_{OH19}, T_{OV19}	Parity(DMA)[5,8]	4	13	
	T_{OH20}, T_{OV20}	$\overline{WBE0:3}$[$\overline{BE0:3}$]	3	9	
	T_{OH21}, T_{OV21}	$\overline{XAck}$	3	10	
	T_{OH22}, T_{OV22}	$\overline{BLast}$[8]	4	14	
T_{OF}	Output float time		**Min**	**Max**	
	T_{OF1}	A6:31	2	8	ns
	T_{OF4}	$\overline{CAS0:3}$	3	10	
	T_{OF5}	$\overline{CS0:7}$	3	10	
	T_{OF6}	D0:31	3	10	
	T_{OF9}	$\overline{DRAMOE}$	3	9	
	T_{OF10}	$\overline{DRAMWE}$	3	9	
	T_{OF13}	$\overline{OE}$	3	9	
	T_{OF14}	$\overline{RAS0:3}$	3	10	
	T_{OF16}	$\overline{Reset}$	2	9	
	T_{OF17}	R/$\overline{W}$	3	9	
	T_{OF20}	$\overline{WBE0:3}$[$\overline{BE0:3}$]	3	9	

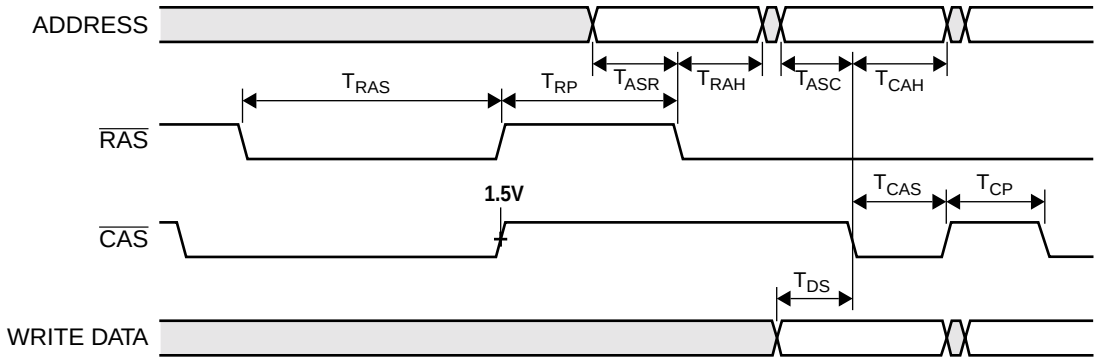
Notes:
1. For all output timing, T_{OH} and T_{OV} are relative to the rising edge of SysClk.
2. For detailed EDO DRAM timing waveforms, refer to "EDO DRAM 2-1-1-1 Burst Read Followed by Single Transfer Read," on page 42 and "EDO DRAM 3-1-1-1 Burst Read Followed by Single Transfer Read," on page 44.
3. The Address bus, $\overline{RAS}$, $\overline{CAS}$ and $\overline{DRAMOE}$ output timings (with respect to the falling edge of the internal duty cycle corrected SysClk) vary with the 403GCX operating frequency. Use the following equations to determine the worst-case output delay and hold times for these signals: $T_{OVf}Max = Tc/2 + T_{OVr}Max$; $T_{OHf}Min = Tc/2 + T_{OHr}Min$, where $T_{OVr}Max$ and $T_{OHr}Min$ correspond to the specifications for the speed grade of the part. Valid for Tc greater than 25 ns and less than 41.7 ns.
4. In early $\overline{RAS}$ mode, the $\overline{RAS}$ output delay varies with the 403GCX operating frequency. Use the following equation to determine the worst-case output delay for this signal: $T_{OV15}Max = Tc/4 + T_{OH15}Min$, where $T_{OH15}Min$ corresponds to the specification for the speed grade of the part. $T_{OH}Min$ remains unchanged. Valid for Tc greater than 25 ns and less than 41.7 ns.
5. Parity timings are for DMA buffered mode. For normal memory accesses, use the data bus timings for parity.
6. Output times are measured with a standard 50 pF capacitive load, unless otherwise noted. Output hold times are measured as T_{OVmin} at 3.47V and Tj=0°C.
7. All output hold and float times are guaranteed by design and not tested.
8. Noted output valid times guaranteed by design and not tested.

Table 18. 403GCX DRAM Interface Timing Relationships

Symbol	Parameter	38 MHz	Units
		Min	
T_{ASR}	Row Address Setup Time to $\overline{RAS}$:		
	BRn[ERM] = 0	$0.5T_C$ -4.0	ns
	BRn[ERM] = 1	$0.25T_C$ -2.5	
T_{RAH}	Row Address Hold Time:		
	BRn[ERM] = 0	$0.5T_C$ -1.5	ns
	BRn[ERM] = 1	$0.67T_C$ -0.5	
T_{ASC}	Column Address Setup Time to $\overline{CAS}$	$0.5T_C$ -4.0	ns
T_{CAH}	Column Address Hold Time	$0.5T_C$ -2.0	ns
T_{CAS}	Available $\overline{CAS}$ Access Time:		
	2-1-1-1 access	$0.5T_C$ -2.5	ns
	3-2-2-2 access	$1.5T_C$ -2.5	
	3-1-1-1 access	$0.5T_C$ -2.5	
T_{CP}	CAS Precharge Time	$0.5T_C$ -2.5	ns
T_{DS}	Write Data Setup Time to $\overline{CAS}$	$0.5T_C$ -4.0	ns
T_{RP}	RAS Precharge Time:		
	BRn[ERM] = 0 and BRn[PCC] = 0	$1.5T_C$ -2.5	ns
	BRn[ERM] = 0 and BRn[PCC] = 1	$2.5T_C$ -2.5	
	BRn[ERM] = 1 and BRn[PCC] = 0	$1.25T_C$ -1.0	
	BRn[ERM] = 1 and BRn[PCC] = 1	$2.25T_C$ -1.0	
T_{RAS}	RAS Active During Refresh:		
	BR[RAR] = 0	$1.5T_C$ -1.5	ns
	BR[RAR] = 1	$2.5T_C$ -1.5	

Note:
1. Relationships are guaranteed by design and are not tested. Relationships also assume 50 pF capacitive loading on interface signals.
2. For detailed DRAM interface timing waveforms, refer to "DRAM Interface Timing Diagram," on page 29.

DRAM Interface Timing Diagram

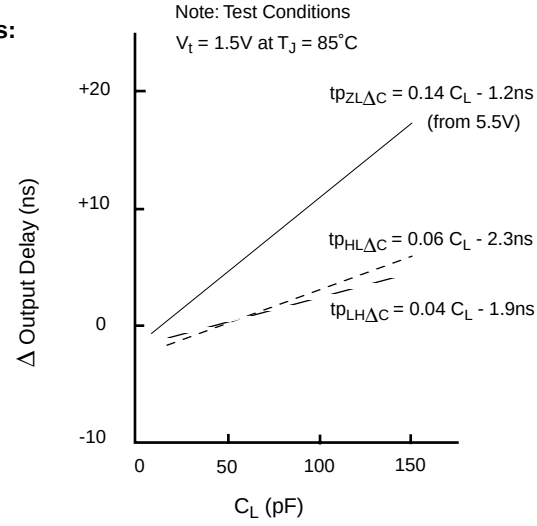


Output Derating for Capacitance and Voltage

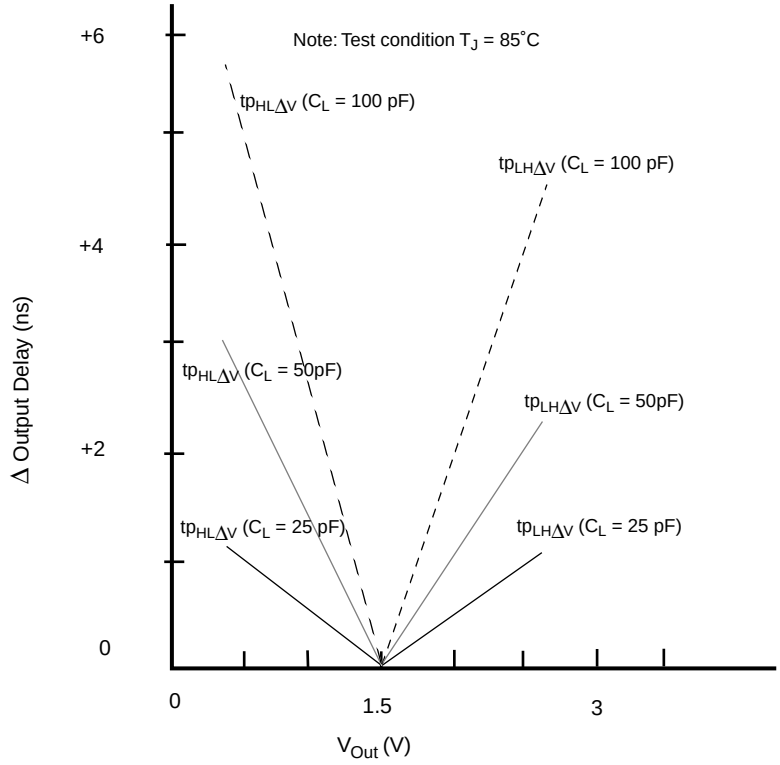
Derating Equations for Output Delays:

1. $\Delta tp_{LH}(C_L, V) = tp_{LH\Delta C} + tp_{LH\Delta V}$
2. $\Delta tp_{HL}(C_L, V) = tp_{HL\Delta C} + tp_{HL\Delta V}$
3. $\Delta tp_{ZL5V}(C_L, V) = tp_{ZL\Delta C} + tp_{HL\Delta V}$

Output Propagation Delay Derating

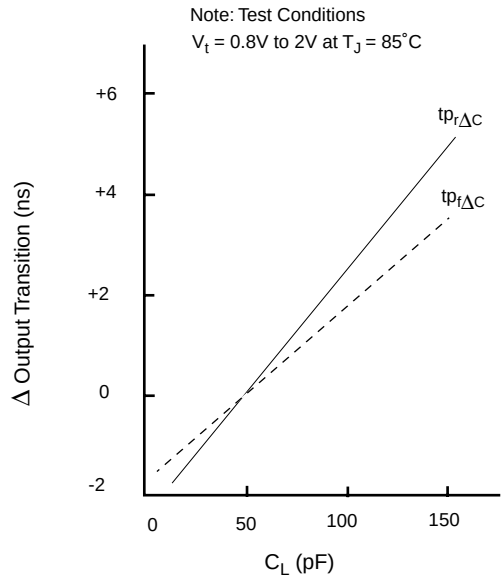


Output Propagation Delay Derating vs Output Voltage Level



Output Rise and Fall Time Derating

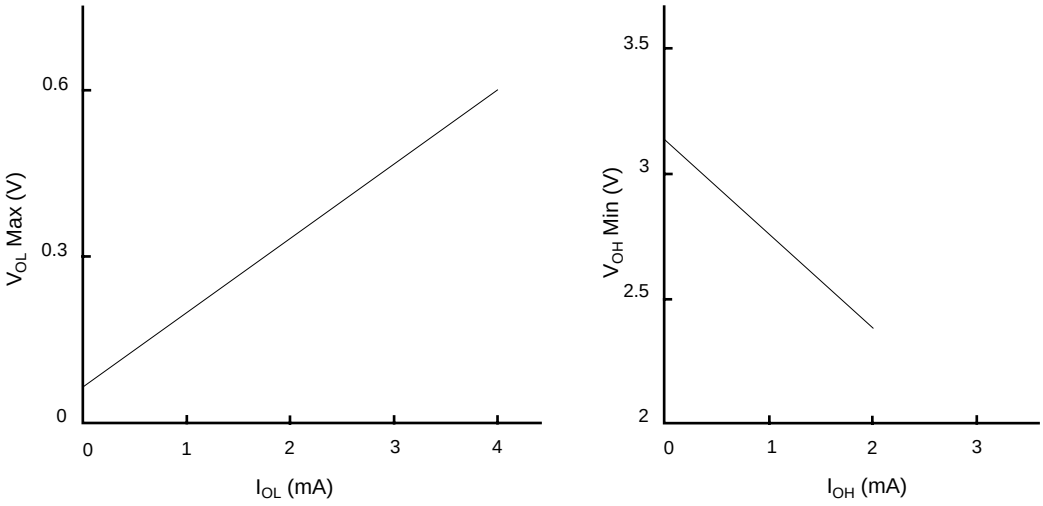
Output Transition Time Derating



Derating Equations for Output Rise and Fall Times:

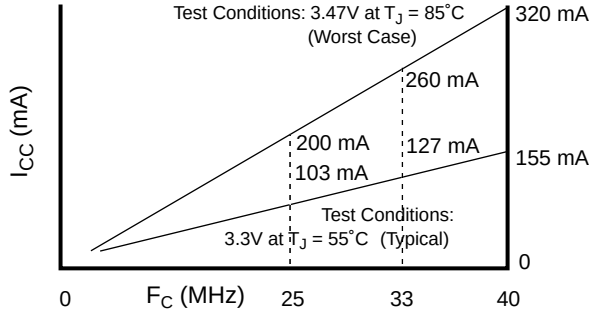
4. $t_R(C_L) = 2ns + tp_{r\Delta C}$
5. $t_F(C_L) = 2.5ns + tp_{f\Delta C}$

Output Voltage vs Output Current

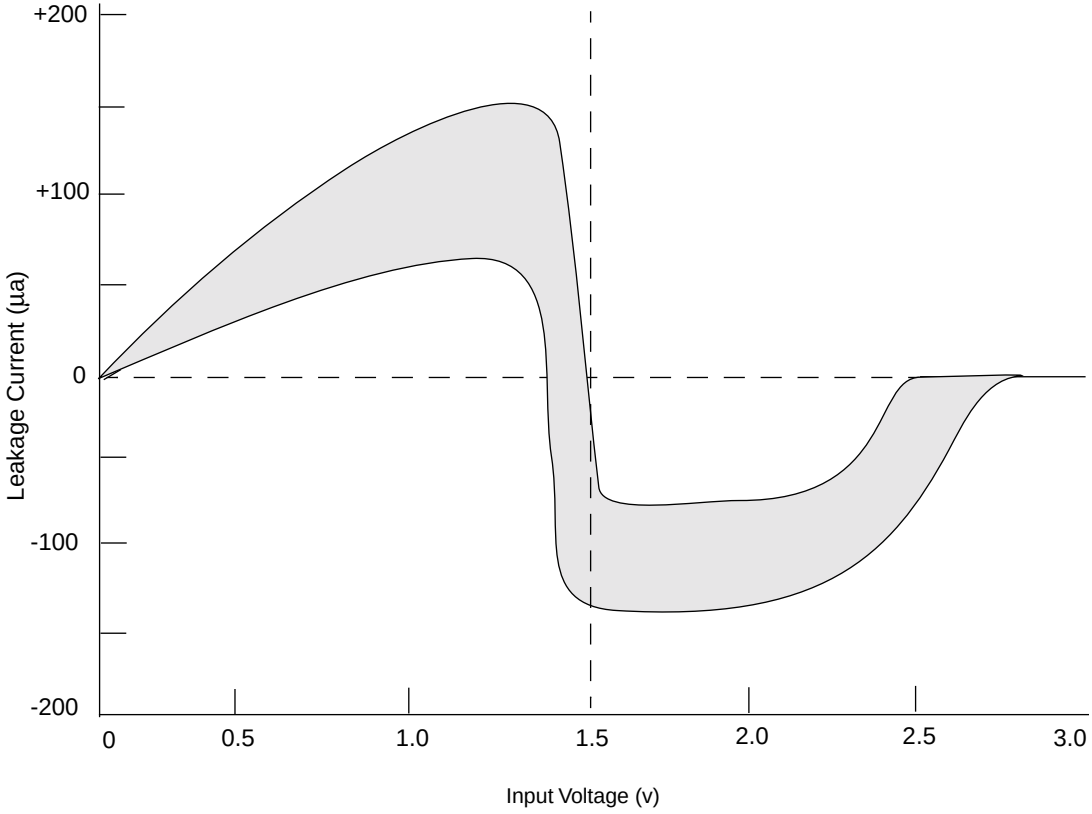


Note: Test conditions 3.14V at T_J = 85˚C

Supply Current vs Operating Frequency



Input Leakage Current



See Note 3 in "403GCX DC Characteristics," on page 21.

Reset and HoldAck

The following table summarizes the states of signals on output pins when Reset or HoldAck is active.

Table 19. Signal States During Reset or Hold Acknowledge

Signal Names	State When Reset Active	State When HoldAck Active
A6:29	Floating	Floating (set to input mode)
AMuxCAS	Inactive (low)	Operable (see note 1)
BusReq	Inactive (low)	Operable (see note 1)
CAS0:3	Inactive (high)	Operable (see notes 1 and 2)
CS0:3	Floating	Floating
CS4:7/RAS3:0	Floating	CS floating, RAS operable (notes 1 and 2)
D0:31	Floating	Floating (external master drives bus)
DMAA0:3	Inactive (high)	Inactive (high)
XAck	Inactive (high)	Operable (see note 1)
DRAMOE	Inactive (high)	Operable (see notes 1 and 2)
DRAMWE	Inactive (high)	Operable (see notes 1 and 2)
Error	Inactive (low)	Operable (see note 1)
HoldAck	Inactive (low)	Active
OE	Floating	Floating (input for XSize1)
Reset	Floating unless initiating system reset	Floating unless initiating system reset
R/W	Floating	Floating (set to input)
TC0:2	Floating (set to input)	Inactive (high)
TC3	Floating (set to input)	Floating (input for XSize0)
TDO	Floating	Operable (see note 1)
TS0:2	Inactive (low)	Operable (see note 1)
TS3:6[DP3:0]	Floating	Operable (see note 1)[floating when parity mode is enabled]
WBE0:3[BE0:3]	Floating	Operable (inputs for A4:5, A30:31)
XmitD	Inactive (high)	Operable (see note 1)

Note:

1. Signal may be active while HoldAck is asserted, depending on the operation being performed by the 403GCX.
2. Signal may be placed in high impedance, depending on DRAM 3-state control setting in IOCR.

Bus Waveforms

The waveforms in this section represent external bus operations, including SRAM and DRAM accesses, DMA transfers, and external master operations.

Write Byte Enable Encoding

The 403GCX provides four write byte enable signals (WBE0:3) to support 8-, 16-, and 32-bit devices, as shown in Table 20. For an eight-bit memory region, WBE2:3 are encoded as A30:31 and WBE0 is the byte-enable line. For a 16-bit region, WBE0 is the high-byte enable, WBE1 is the low-byte enable and WBE2:3 are encoded as A30:31. For a 32-bit region, address bits 6:29 select the word address and WBE0:3 select data bytes 0:3, respectively.

Table 20. Write Byte Enable Encoding

	Transfer Size	Address	$\overline{WBE0}$ = $\overline{WE}$	$\overline{WBE1}$ = 1	$\overline{WBE2}$ = A30	$\overline{WBE3}$ = A31
8-Bit Bus Width	Byte	0	0	1	0	0
	Byte	1	0	1	0	1
	Byte	2	0	1	1	0
	Byte	3	0	1	1	1
	Transfer Size	Address	$\overline{WBE0}$ = $\overline{BHE}$	$\overline{WBE1}$ = $\overline{BLE}$	$\overline{WBE2}$ = A30	$\overline{WBE3}$ =A31
16-Bit Bus Width	Half-word	0	0	0	0	0
	Half-word	2	0	0	1	0
	Byte	0	0	1	0	0
	Byte	1	1	0	0	1
	Byte	2	0	1	1	0
	Byte	3	1	0	1	1
	Transfer Size	Address	$\overline{WBE0}$	$\overline{WBE1}$	$\overline{WBE2}$	$\overline{WBE3}$
32-Bit Bus Width	Word	0	0	0	0	0
	Half-word	0	0	0	1	1
	Half-word	2	1	1	0	0
	Byte	0	0	1	1	1
	Byte	1	1	0	1	1
	Byte	2	1	1	0	1
	Byte	3	1	1	1	0

Address Bus Multiplexing

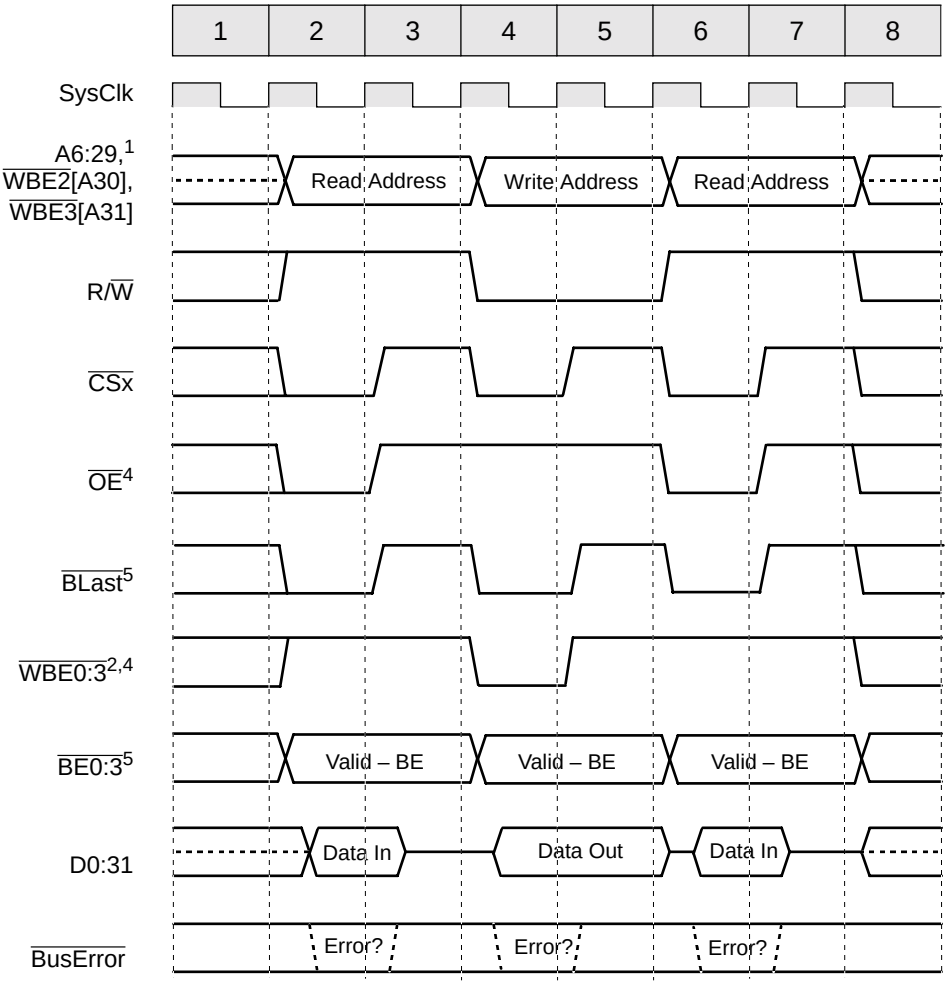
To support DRAM memories with differing configurations and bus widths, the 403GCX provides an internally multiplexed address bus controlled by the BIU. Table 21 shows the multiplexed address outputs referenced by waveforms later in this section.

Table 21. Multiplexed Address Outputs

Address Pins	**A11**	**A12**	**A13**	**A14**	**A15**	**A16**	**A17**	**A18**	**A19**	**A20**	**A21**	**A22**	**A23**	**A24**	**A25**	**A26**	**A27**	**A28**	**A29**
Addr Bits Out in $\overline{RAS}$ Cycle	a6	a7	a8	a9	a10	a11	a12	a13	a12	a13	a14	a15	a16	a17	a18	a19	a20	a21	a22
Addr Bits Out in $\overline{CAS}$ Cycle	xx	a6	a7	a8	a9	a10	a11	a12	a21	a22	a23	a24	a25	a26	a27	a28	a29	a30	a31

When the 403GCX is bus master and there are no bus operations in progress, the states of the address bus outputs are determined by the setting of IOCR[ATC]. If this bit is set to zero, the address bus will be placed in high impedance. If this bit is set to one, the last address held in the BIU address register will be driven out on the address bus until bus operations resume.

SRAM Read-Write-Read with Zero Wait and One Hold



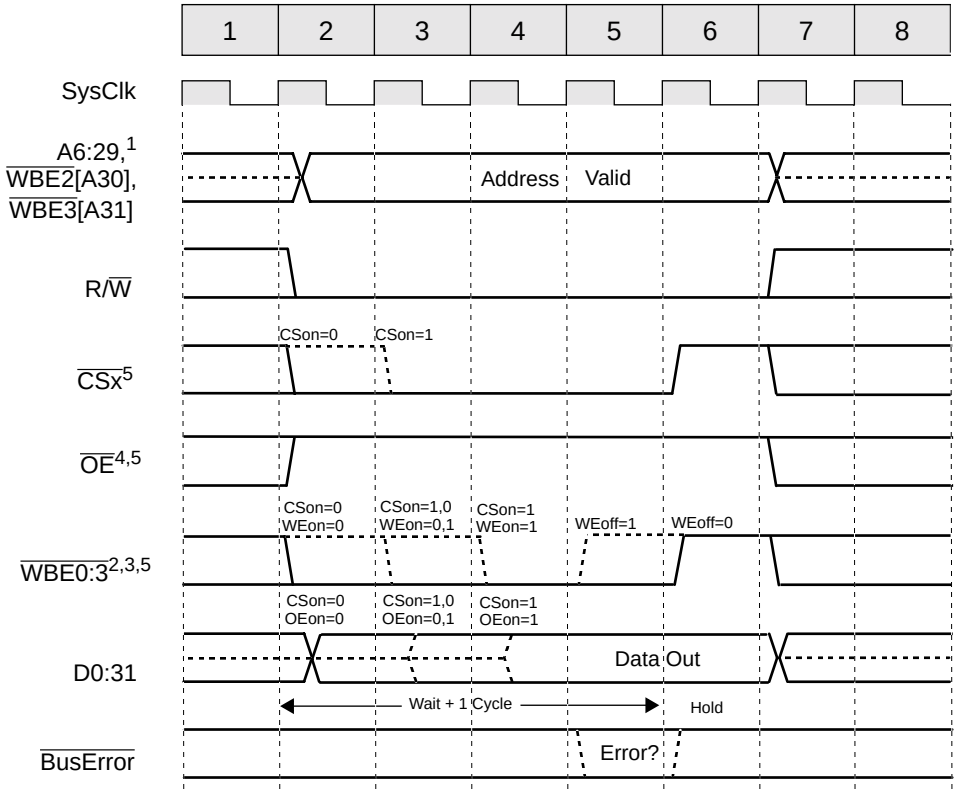
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	0	xx	0	00 0000	0	0	0	0	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 20 on page 34 for WBE signal definitions based on bus width.
3. Byte Enable Mode IOCR[BEM] = 1. WBE0:3/BE0:3 are byte enables and BLast is the signal which appears on the multiplexed OE[XSize1][BLast] output.
4. When in Byte Enable Mode IOCR[BEM] = 1, the BLast signal appears on the multiplexed OE[XSize1][BLast] output, as described in Table 4 on page 8.
5. Not Byte Enable Mode IOCR[BEM] = 0. WBE0:3/BE0:3 are write byte enables and OE is the signal which appears on the multiplexed OE[XSize1][BLast] output.

SRAM, ROM, or I/O Write Request with Wait and Hold



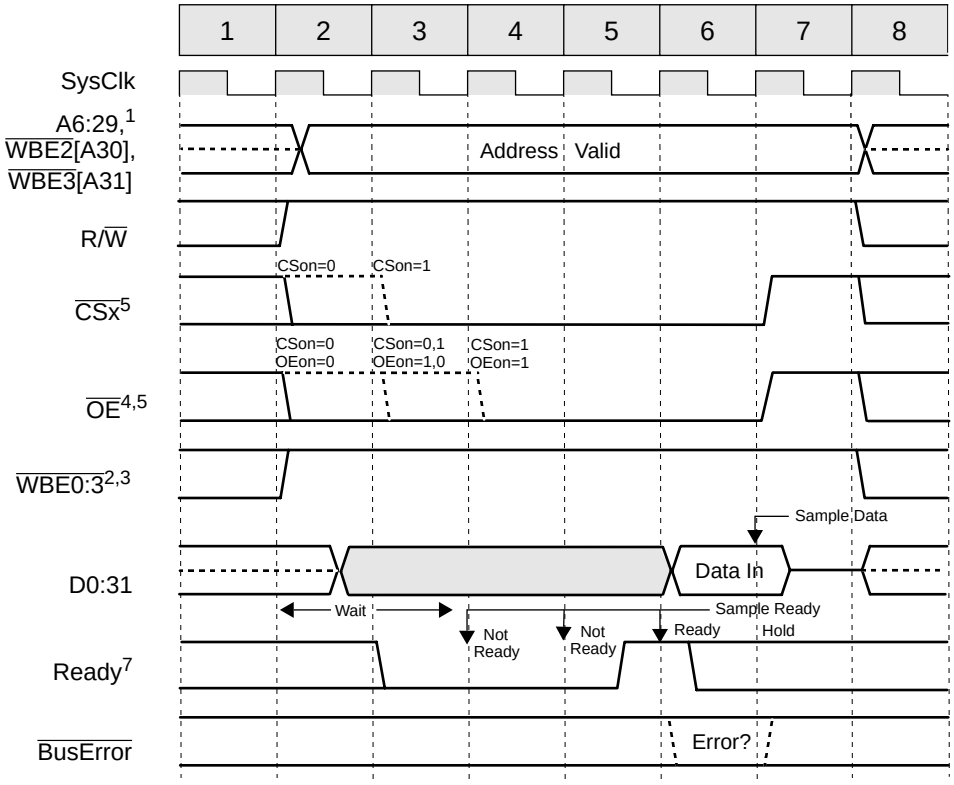
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	0	xx	0	00 0011	0 or 1	0 or 1	0 or 1	0 or 1	001

Notes:

1. $\overline{WBE2:3}$ are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 20 for $\overline{WBE}$ signal definitions based on bus width.
3. $\overline{WBE}$ signals can be read/write byte enables based on the setting of IOCR[BEM]. See waveform and note 3 on page 35.
4. When in Byte Enable Mode IOCR[BEM] = 1, the $\overline{BLast}$ signal appears on the multiplexed $\overline{OE}$[XSize1][$\overline{BLast}$] output, as described in Table 4 on page 8.
5. Wait must be programmed to a value ≥ (CSon + WEon + WEoff) and ≥ (CSon + OEon + WEoff).
   If Wait > (CSon + WEon) and > (CSon + OEon), then all signals retain the values shown in cycle 4 until the Wait time expires.
6. If Hold is programmed > 001, all signals retain the values shown in cycle 6 until the Hold timer expires.

SRAM, ROM, or I/O Read Request, Wait Extended with Ready



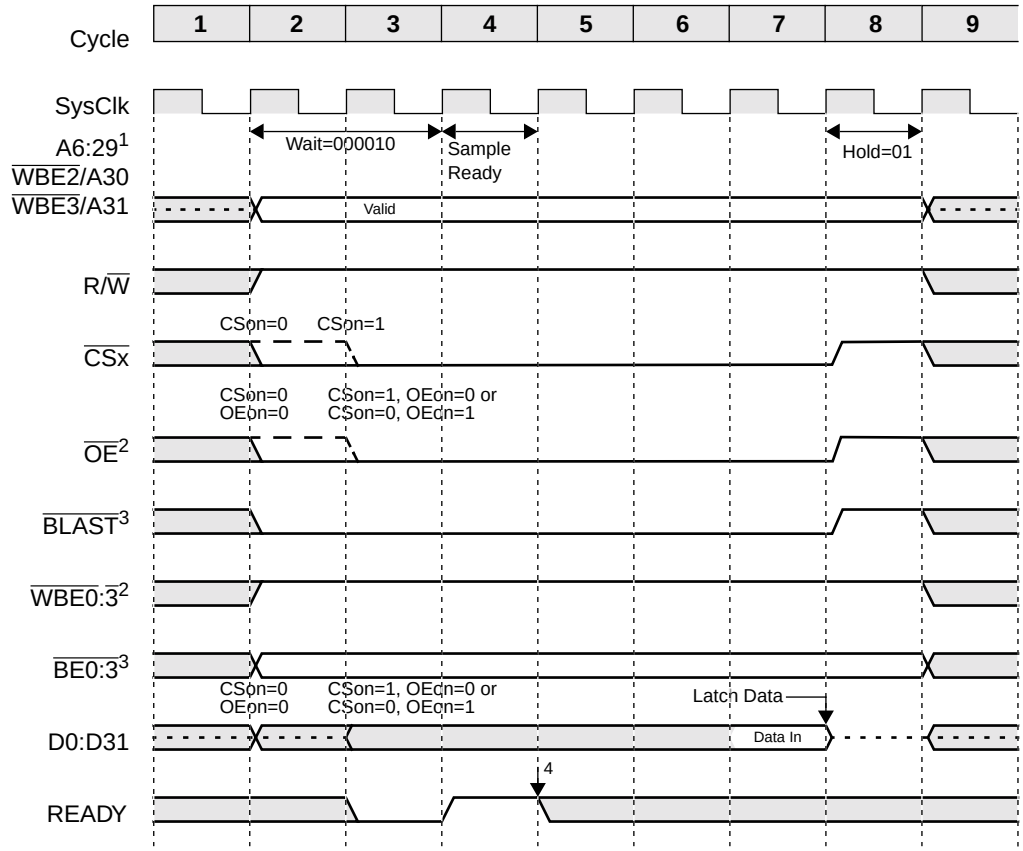
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	0	xx	1	00 0010	0 or 1	0 or 1	0 or 1	x	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 20 on page 34 for WBE signal definitions based on bus width.
3. WBE signals can be read/write byte enables based on the setting of IOCR[BEM]. See waveform and note 3 on page 35.
4. When in Byte Enable Mode IOCR[BEM] = 1, the BLast signal appears on the multiplexed OE[XSize1][BLast] output, as described in Table 4 on page 8.
5. Wait must be programmed to a value ≥ (CSon + OEon). If Wait > (CSon + OEon), then all signals will retain the values shown in cycle 4 until the Wait timer expires.
6. If Hold is programmed > 001, all output signals retain the values shown in cycle 7 until the Hold timer expires.
7. If Wait = 00 0000, the Ready input is ignored and single-cycle transfers occur. If Wait > 00 0000, Ready is sampled starting after the Wait cycles have expired.
8. IOCR[SOR] = 0.

SRAM Read Extended with Ready (Asynchronous Ready Mode)



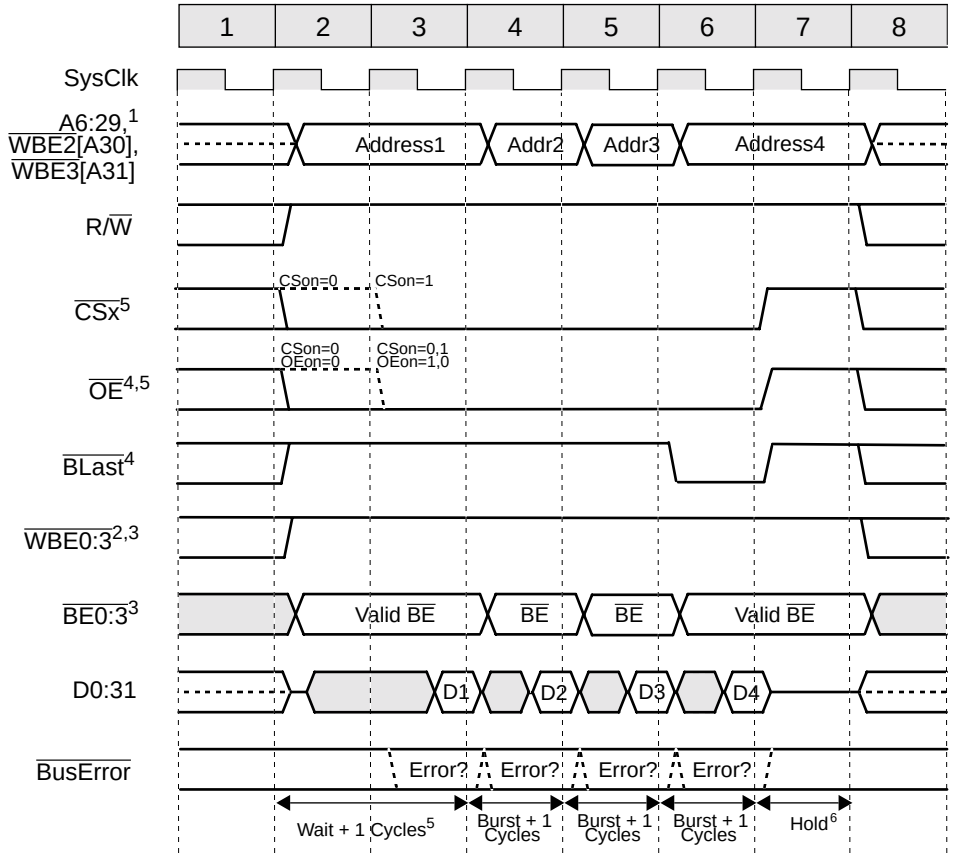
Bank Register Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
x	o	xx	1	000010	0 or 1	0 or 1	x	0	001

Notes:

1. WBE2:3 are address bits A30:31 if the bus width is programmed as byte or halfword.
2. Not Byte Enable Mode (IOCR[BEM] = 0). WBE0:3/BE0:3 are write byte enables and OE/BLAST is OE.
3. Byte Enable Mode (IOCR[BEM] = 1). WBE0:3/BE0:3 are byte enables and OE/BLAST is BLAST
4. Arrows indicate when READY is sampled.
5. IOCR[ARE] is set.

SRAM, ROM or I/O Burst Read with Wait and Hold



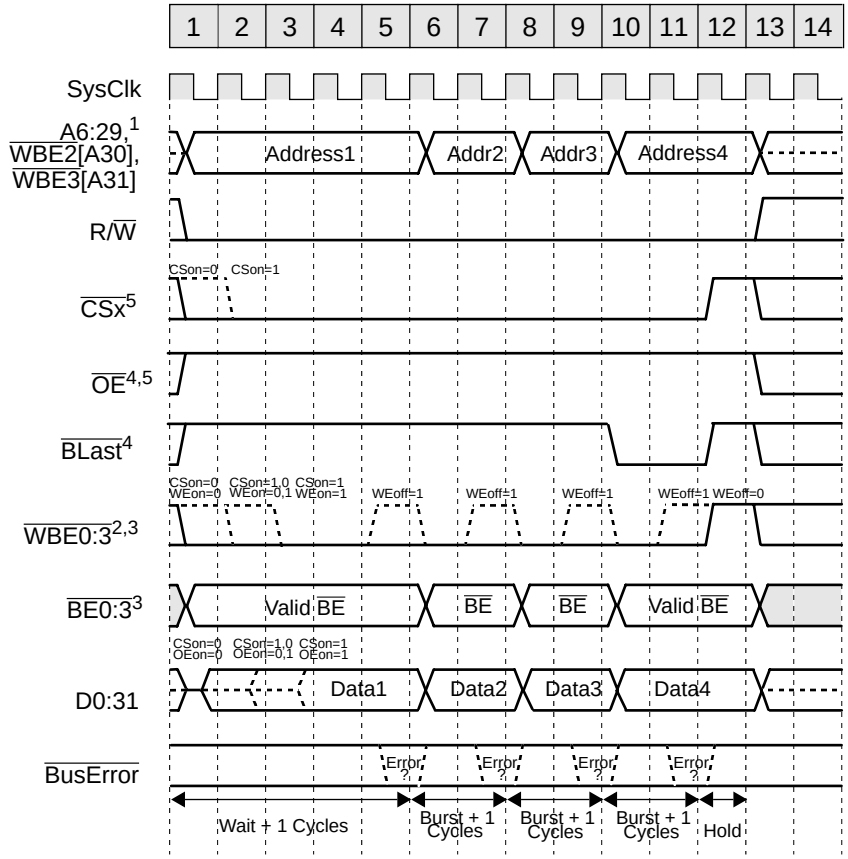
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	Burst Wait	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:21	Bits 22:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	1	xx	0	0001	00	0 or 1	0 or 1	x	x	001

Notes:

1. $\overline{WBE2:3}$ are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 20 on page 34 for $\overline{WBE}$ signal definitions based on bus width.
3. $\overline{WBE}$ signals can be read/write byte enables based on the setting of IOCR[BEM].
4. When in Byte Enable Mode (IOCR[BEM] = 1), the $\overline{BLast}$ signal appears on the multiplexed $\overline{OE}$[XSize1][$\overline{BLast}$] output, as described in Table 4 on page 8.
5. Wait must be programmed to a value ≥ (CSon + OEon). If Wait > (CSon + OEon), then all signals will retain the values shown in cycle 3 until the Wait timer expires.
6. If Hold is programmed > 001, all output signals retain the values shown in cycle 7 until the Hold timer expires.
7. Data parity is only checked when IOCR[RDM] = 11 and BRHx[PCE] is set.

SRAM, ROM or I/O Burst Write with Wait, Burst Wait, and Hold



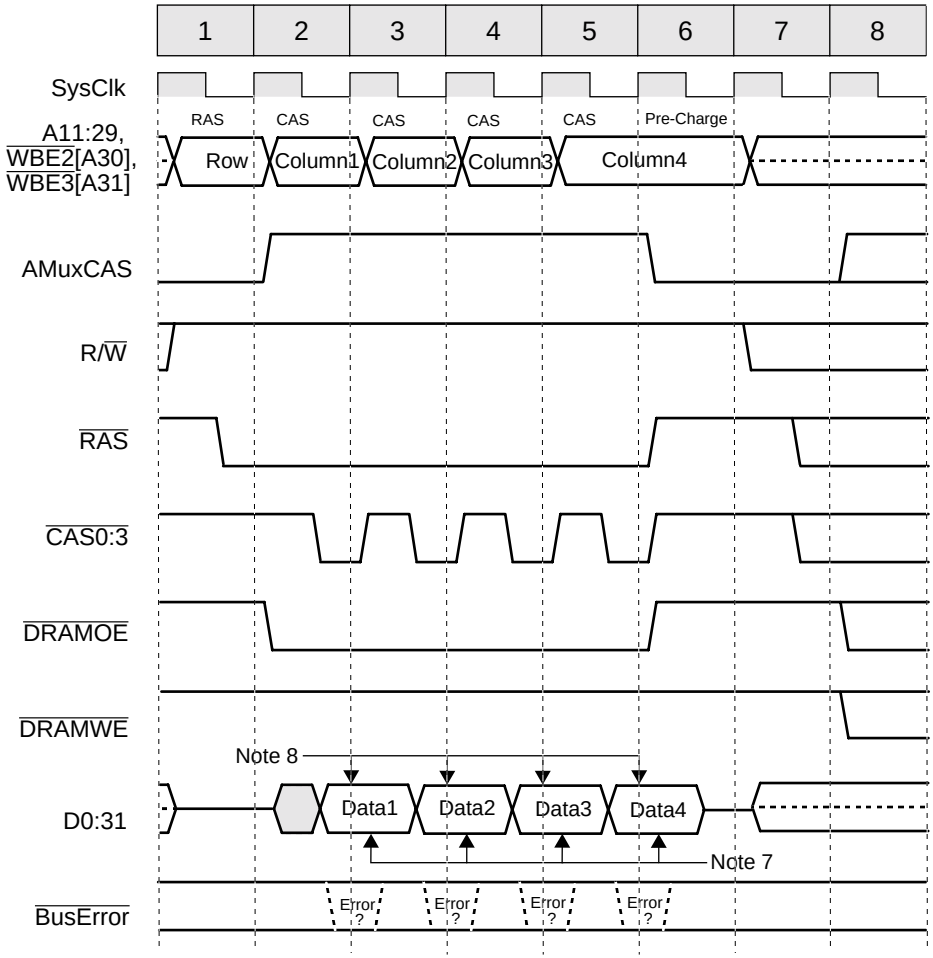
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	Burst Wait	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:21	Bits 22:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	1	xx	0	0100	01	0 or 1	0 or 1	0 or 1	0 or 1	001

Notes:

1. $\overline{\text{WBE2:3}}$ are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 20 on page 34 for $\overline{\text{WBE}}$ signal definitions based on bus width.
3. $\overline{\text{WBE}}$ signals can be read/write byte enables based on the setting of a control bit in the IOCR.
4. When in Byte Enable Mode (IOCR bit 20 = 0), the $\overline{\text{BLast}}$ signal appears on the multiplexed $\overline{\text{OE}}$[XSize1][$\overline{\text{BLast}}$] output, as described in Table 4 on page 8.
5. Wait must be programmed to a value ≥ (CSon + WEon + WEoff) and ≥ (CSon + OEon + WEoff).
   If Wait > (CSon + WEon) and > (CSon + OEon), then all signals retain the values shown in cycle 3 until the Wait timer expires.
6. If Hold is programmed > 001, all output signals retain the values shown in cycle 12 until the Hold timer expires.
7. Data parity is only generated when IOCR[RDM] = 11.

DRAM 2-1-1-1 Page Mode Read



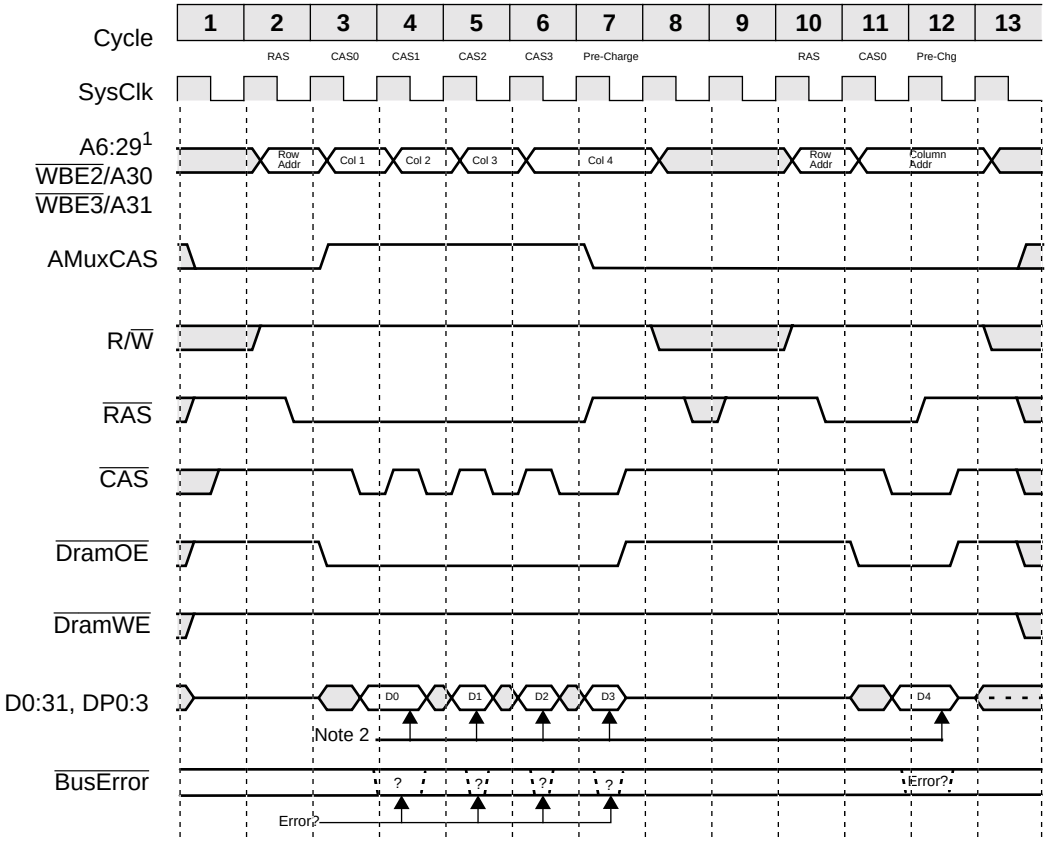
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	xx	x	0	0	1	00	00	0	x	xxxx

Notes:

1. For burst access, the addresses represented by Columns 1 to 4 does not necessarily indicate that they are in incremental address order. Typically, burst access is target word first.
2. If internal mux mode is used, address bits A11:29 represent address bits described in Table 21 on page 34.
3. During internal mux mode access, A6:10 retain their unmultiplexed values.
4. If external mux mode is used, A11:29 are unaffected and do not change between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ cycles.
5. If bus width is programmed as byte or half-word, $\overline{\text{WBE2:3}}$ represent address bits A30:31 regardless of mux mode.
6. $\overline{\text{WBE0:1}}$ are always ones during DRAM transfers.
7. Data is latched on the rising edge of SysClk when IOCR[DRC] = 0 (default setting).
8. Data is latched later (on the rising edge of $\overline{\text{CAS}}$) if IOCR[DRC] = 1.

EDO DRAM 2-1-1-1 Burst Read Followed by Single Transfer Read



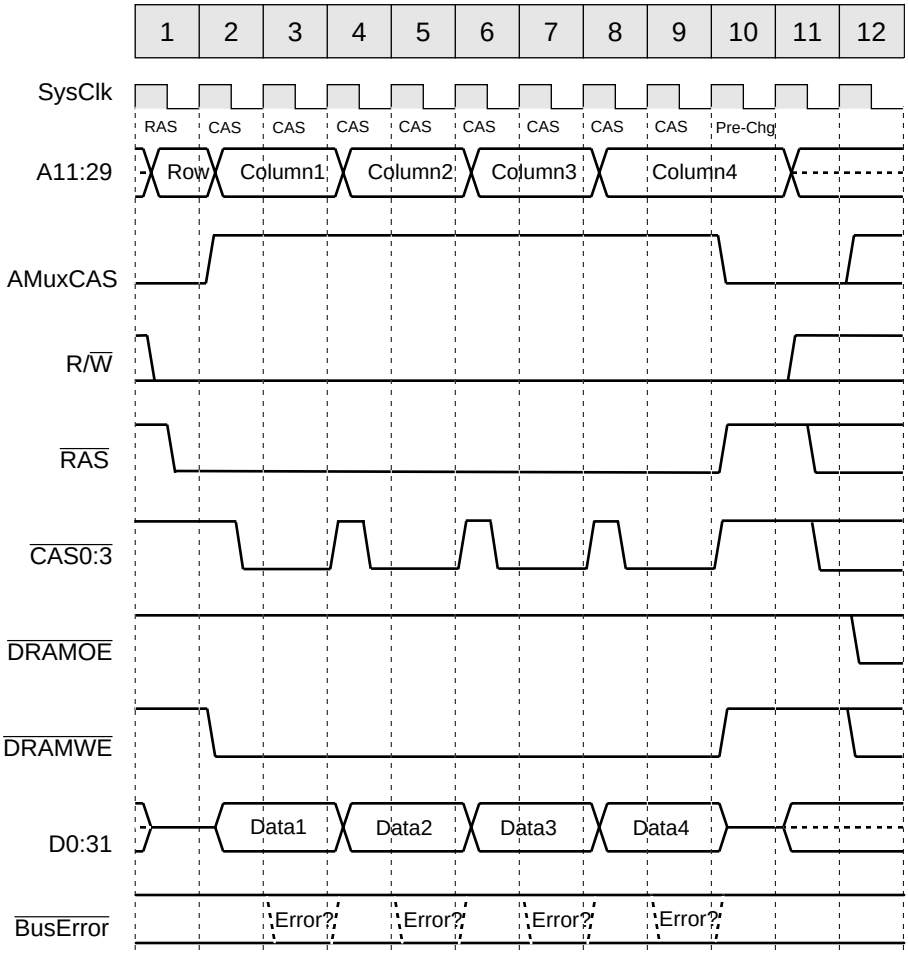
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
x	0	10	0	0	0	1	00	00	0	1	xxxx

Notes:

1. IOCR[EDO] is set and IOCR[DRC] is cleared.
2. Data is latched with respect to the fall of the internal system clock (duty-cycle corrected).
3. Data parity, if enabled, matches the timing of data bus transfers.

DRAM 3-2-2-2 Page Mode Write



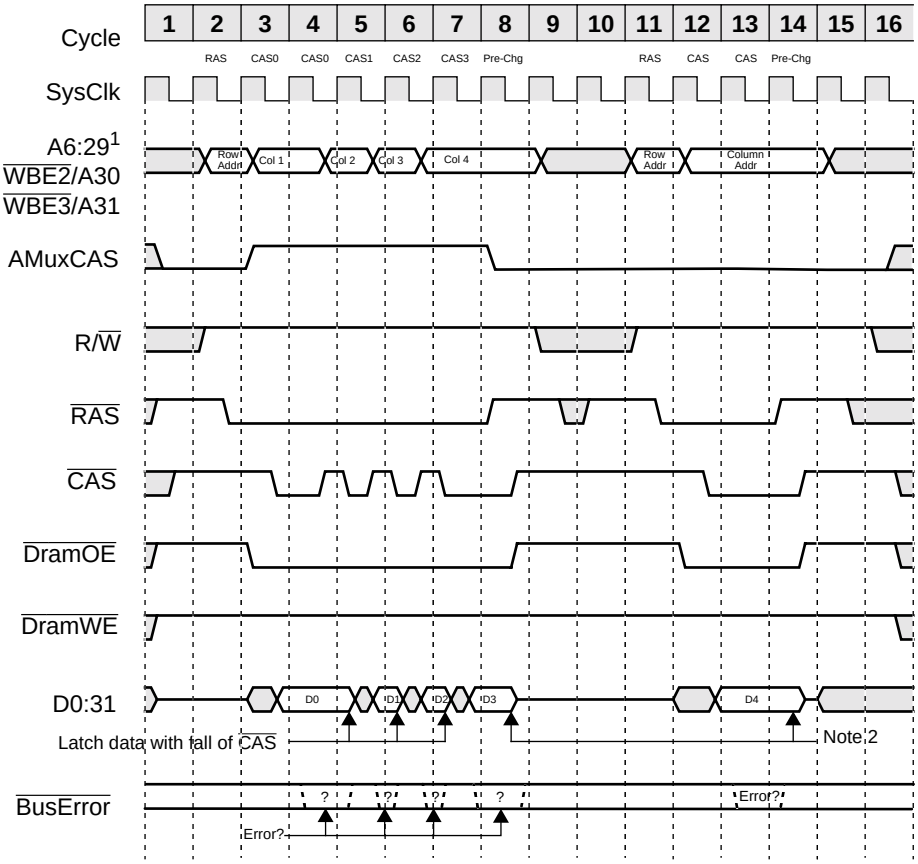
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	xx	x	0	0	1	01	01	0	x	xxxx

Notes:

1. For burst access, the addresses represented by Columns 1 to 4 do not necessarily indicate that they are in incremental address order. Typically, burst access is target word first.
2. If internal mux mode is used, address bits A11:29 represent address bits described in Table 21 on page 34.
3. During internal mux mode access, A6:10 retain their unmultiplexed values.
4. If external mux mode is used, A11:29 are unaffected and do not change between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ cycles.
5. If bus width is programmed as byte or half-word, $\overline{\text{WBE2:3}}$ represent address bits A30:31 regardless of mux mode.
6. $\overline{\text{WBE0:1}}$ are always ones during DRAM transfers.
7. DRAM read on $\overline{\text{CAS}}$, IOCR[DRC], and EDO DRAM, IOCR[EDO], modes do not affect writes.

EDO DRAM 3-1-1-1 Burst Read Followed by Single Transfer Read



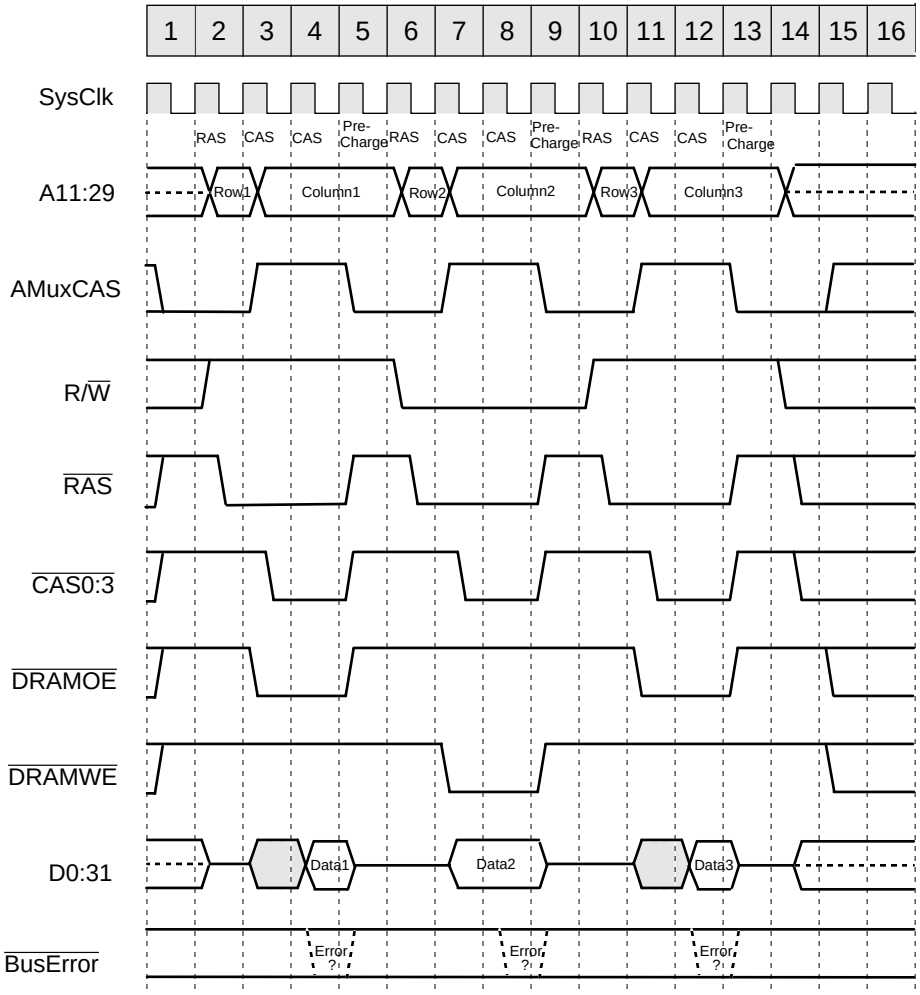
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
x	0/1	10	0	0	0	1	01	00	0	x	xxxx

Notes:

1. IOCR[EDO] is set and IOCR[DRC] is cleared.
2. Data is latched with respect to the fall of the internal system clock (duty-cycle corrected).
3. Data parity, if enabled, matches the timing of data bus transfers.

DRAM Read-Write-Read, One Wait



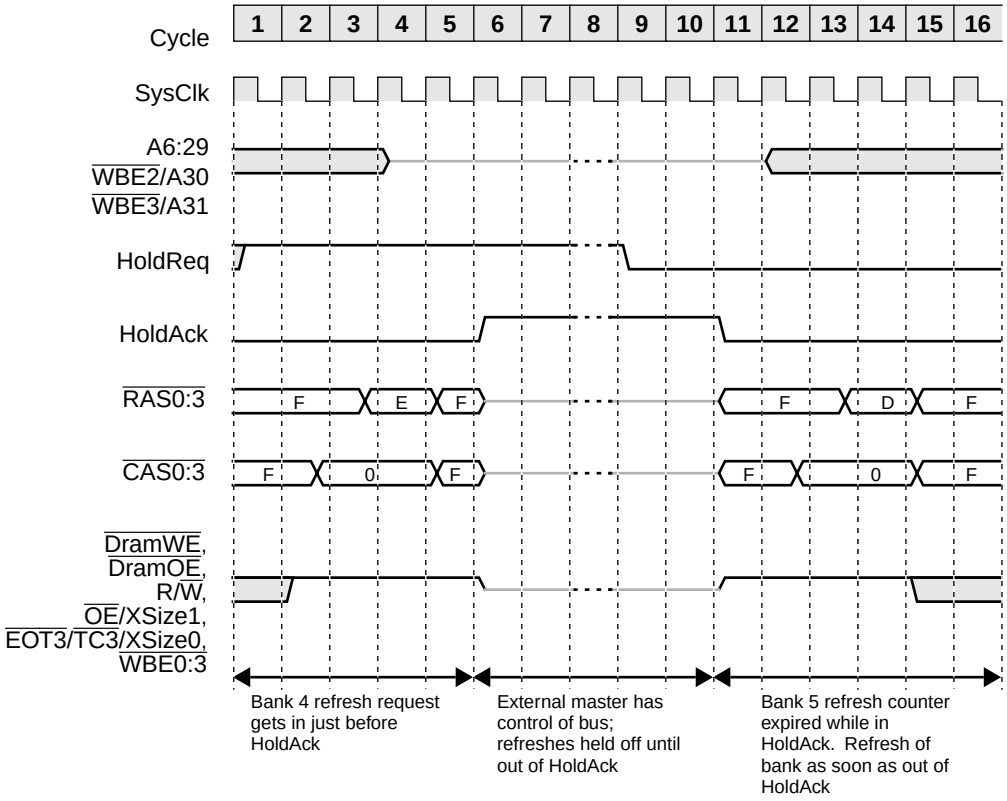
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	xx	x	0	0	0	01	xx	0	x	xxxx

Notes:

1. If internal mux mode is used, address bits A11:29 represent address bits described in Table 21 on page 34.
2. During internal mux mode access, A6:10 retain their unmultiplexed values.
3. If external mux mode is used, A11:29 are unaffected and do not change between $\overline{CAS}$ and $\overline{RAS}$ cycles.
4. If bus width is programmed as byte or half-word, $\overline{WBE2:3}$ represent address bits A30:31 regardless of mux mode.
5. $\overline{WBE0:1}$ are always ones during DRAM transfers.

DRAM Three-state - Refresh request before and after HoldAck

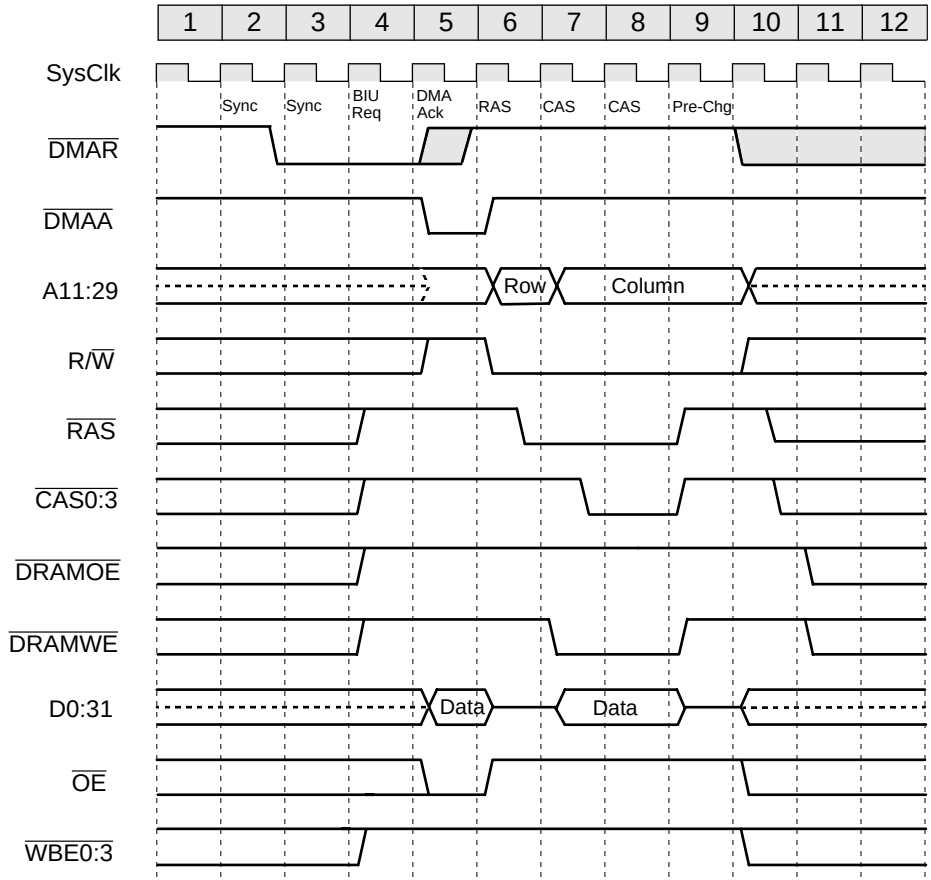


Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
x	x	10	0	x	0	x	x	x	x	0	xxxx

Note:
1. IOCR[EDT] is set.

DMA Buffered Single Transfer from Peripheral to 3-Cycle DRAM



Bank Register Bit Settings

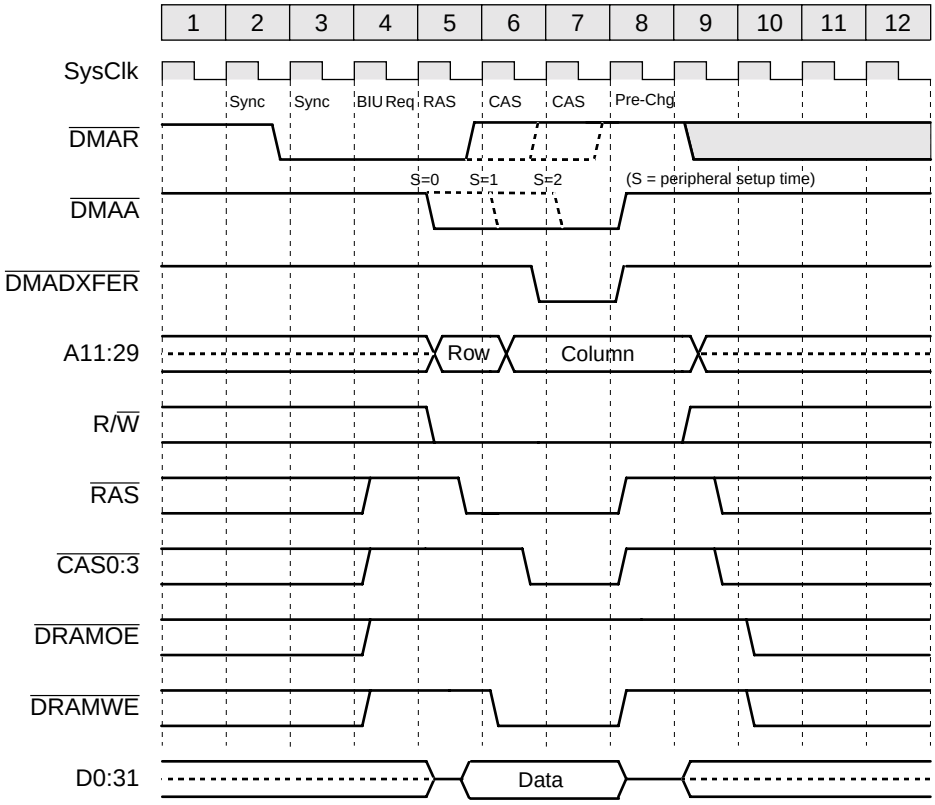
SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	0	0	0	0	01	xx	0	x	xxxx

DMA Control Register Bit Settings

Transfer Direction	Transfer Width	Transfer Mode	PeripheralSetup	Peripheral Wait	Peripheral Hold
Bit 2	Bits 4:5	Bits 9:10	Bits 11:12	Bits 13:18	Bits 19-21
1	10	00	00	00 0000	000

Notes:
1. $\overline{\text{DMAR}}$ must be inactive inactive at the start of cycle 9 to guarantee a single transfer.
2. This waveform assumes that the internal address mux is used.
3. $\overline{\text{CAS0}}$ is used for byte accesses, $\overline{\text{CAS0:1}}$ for halfwords, and $\overline{\text{CAS0:3}}$ for fullwords.

DMA Fly-By Single Transfer, Write to 3-Cycle DRAM



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	0	0	0	0	01	xx	0	x	xxxx

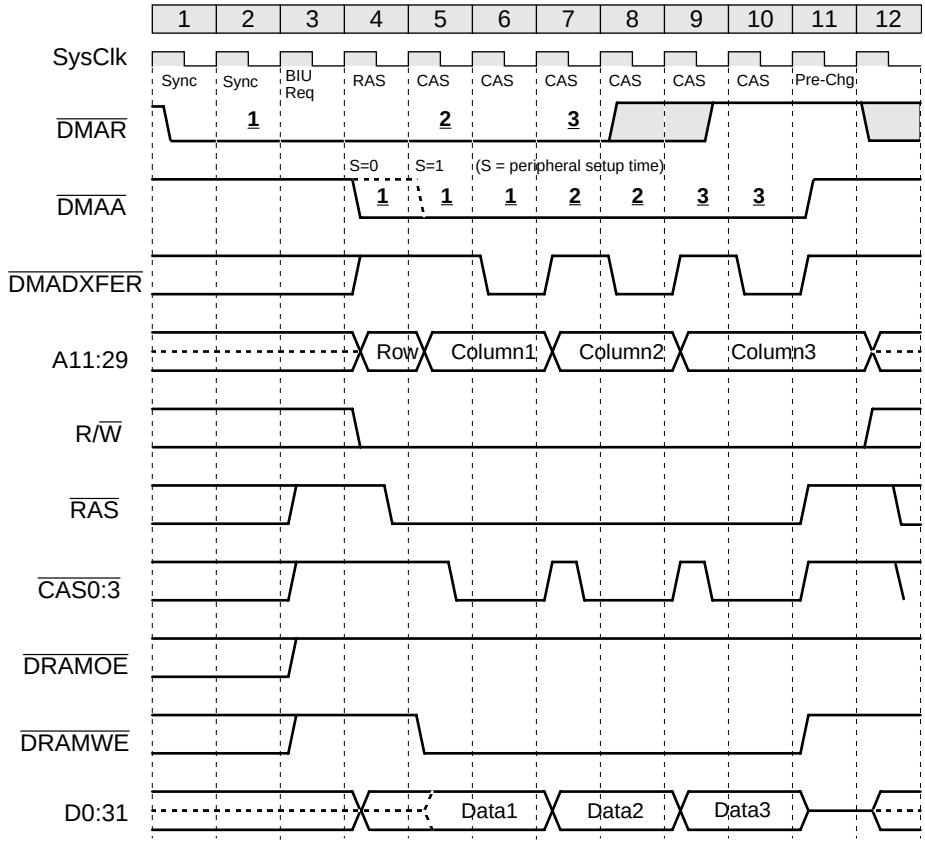
DMA Control Register Bit Settings

Transfer Direction	Transfer Width	Transfer Mode	PeripheralSetup	Peripheral Wait	Peripheral Hold
Bit 2	Bits 4:5	Bits 9:10	Bits 11:12	Bits 13:18	Bits 19-21
1	10	01	Note 3	xx xxxx	xxx

Notes:

1. $\overline{\text{DMAR}}$ must be inactive in cycle 7 (last $\overline{\text{DMAA}}$ cycle) to guarantee a single transfer.
2. Peripheral data bus width must match DRAM bus width.
3. See diagram for settings.
4. This waveform assumes that the internal address mux is used.
5. $\overline{\text{CAS0}}$ is used for byte accesses, $\overline{\text{CAS0:1}}$ for halfwords, and $\overline{\text{CAS0:3}}$ for fullwords.

DMA Fly-By Continuous Burst to 3-Cycle DRAM



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	0	0	0	1	01	01	0	x	xxxx

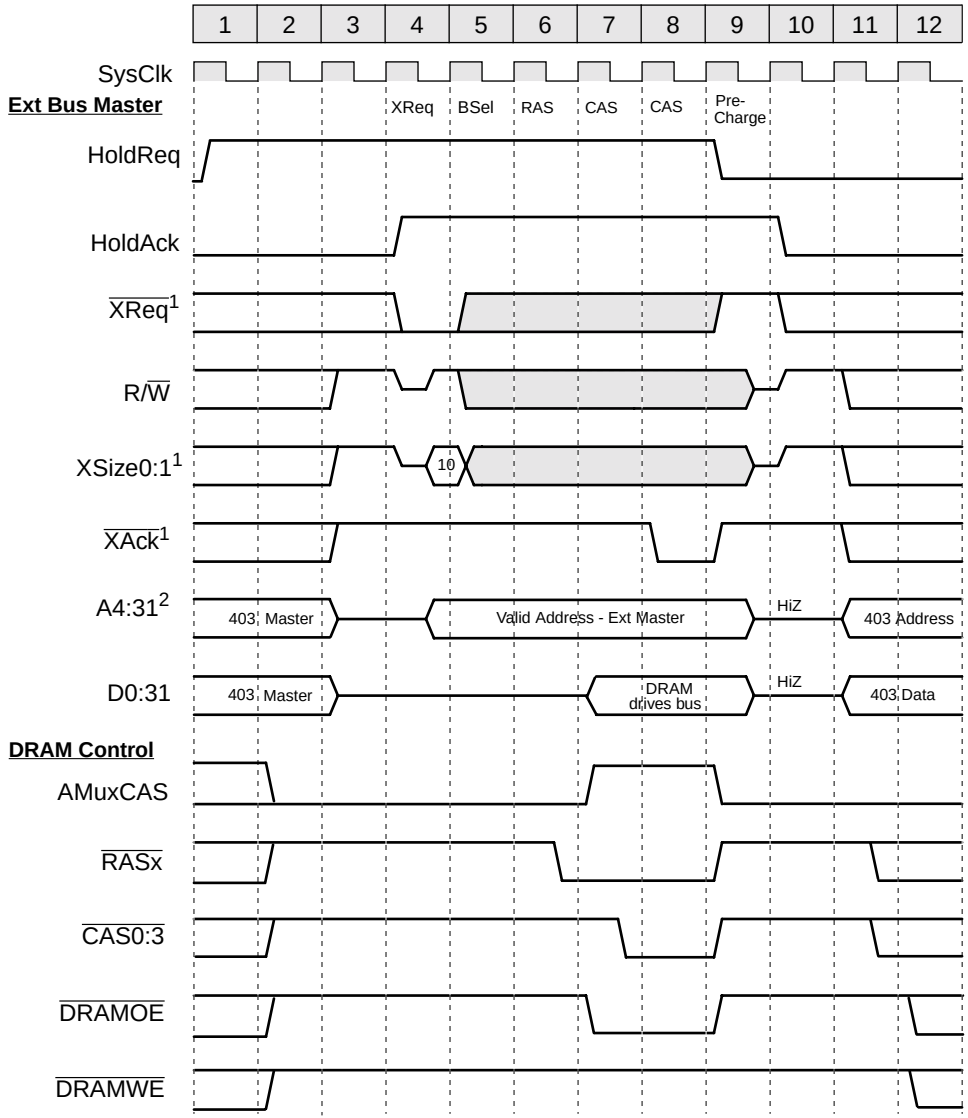
DMA Control Register Bit Settings

Transfer Direction	Transfer Width	Transfer Mode	Peripheral Setup	Peripheral Wait	Peripheral Hold	Burst Mode
Bit 2	Bits 4:5	Bits 9:10	Bits 11:12	Bits 13:18	Bits 19-21	Bit 25
1	10	01	Note 3	xx xxxx	xxx	1

Notes:

1. $\overline{\text{DMAR}}$ must be inactive at the end of cycle 10 (last $\overline{\text{DMAA}}$ cycle) to guarantee three transfers.
2. Peripheral data bus width must match DRAM bus width.
3. See diagram for settings.
4. This waveform assumes that the internal address mux is used.
5. $\overline{\text{CAS0}}$ is used for byte accesses, $\overline{\text{CAS0:1}}$ for halfwords, and $\overline{\text{CAS0:3}}$ for fullwords.
6. Numbers (**1**,**2**,**3**,...) in the $\overline{\text{DMAR}}$ signal represent when $\overline{\text{DMAR}}$ is sampled and accepted. Numbers (**1**,**2**,**3**,...) in the $\overline{\text{DMAA}}$ signal represent the transfers associated with the accepted $\overline{\text{DMAR}}$.

External Master Nonburst DRAM Read with HoldReq/HoldAck



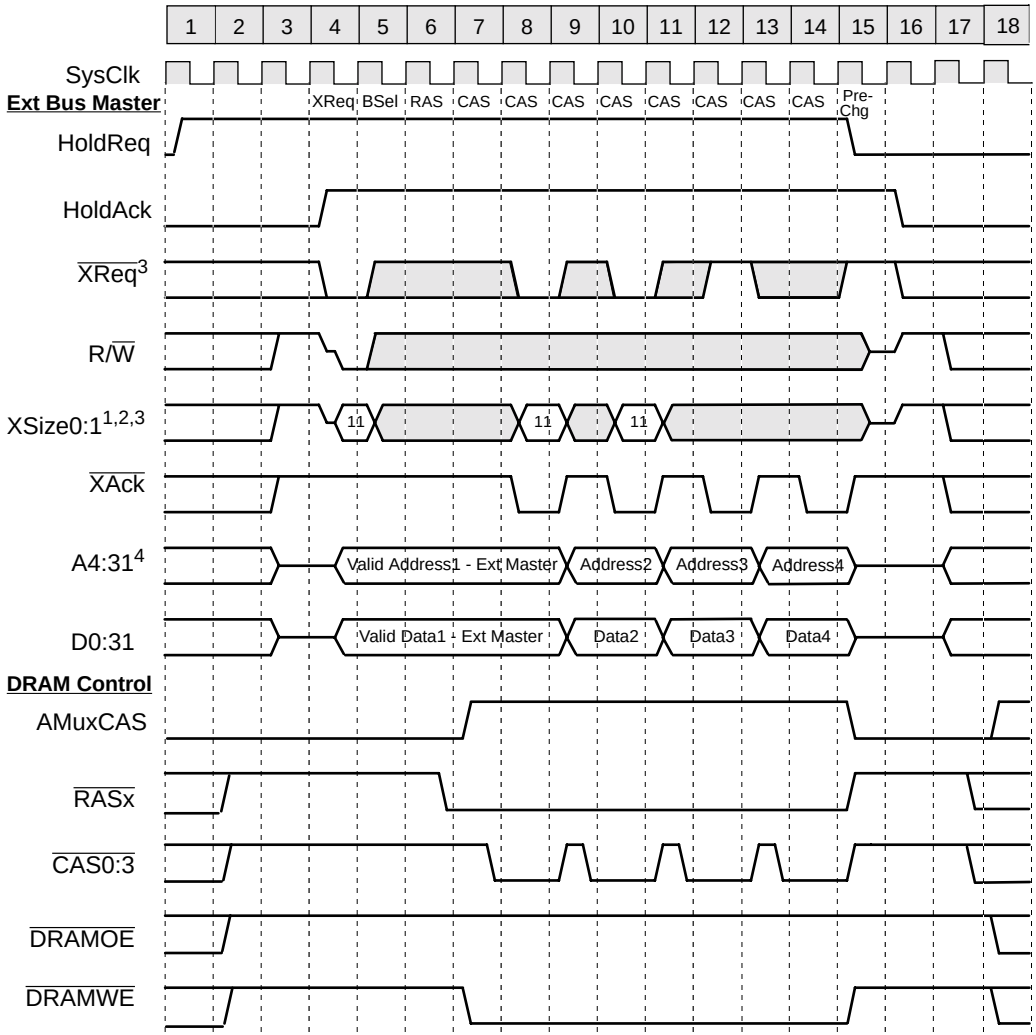
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	1	0	0	0	01	xx	0	x	xxxx

Notes:

1. $\overline{\text{XReq}}$, XSize0, XSize1, and $\overline{\text{XAck}}$ are multiplexed with $\overline{\text{DMAR3}}$, $\overline{\text{EOT3}}$/$\overline{\text{TC3}}$, $\overline{\text{OE}}$, and $\overline{\text{DMAA3}}$, respectively.
2. A4, A5, A30, and A31 are multiplexed with $\overline{\text{WBE0}}$, $\overline{\text{WBE1}}$, $\overline{\text{WBE2}}$, and $\overline{\text{WBE3}}$, respectively.

External Master DRAM Burst Write, 3-2-2-2 Page Mode



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	1	0	0	1	01	01	0	x	xxxx

Notes:

1. $\overline{\text{XReq}}$, XSize0, XSize1, and $\overline{\text{XAck}}$ are multiplexed with $\overline{\text{DMAR3}}$, $\overline{\text{EOT3}}$/$\overline{\text{TC3}}$, $\overline{\text{OE}}$, and $\overline{\text{DMAA3}}$, respectively.
2. XSize0:1 = 11 indicates a burst transfer at the width of the DRAM device.
3. The burst is terminated in cycle 12 by deasserting the $\overline{\text{XReq}}$ input signal. A burst may also be terminated by deasserting either XSize0 or XSize1.
4. A4, A5, A30, and A31 are multiplexed with $\overline{\text{WBE0}}$, $\overline{\text{WBE1}}$, $\overline{\text{WBE2}}$, and $\overline{\text{WBE3}}$, respectively.

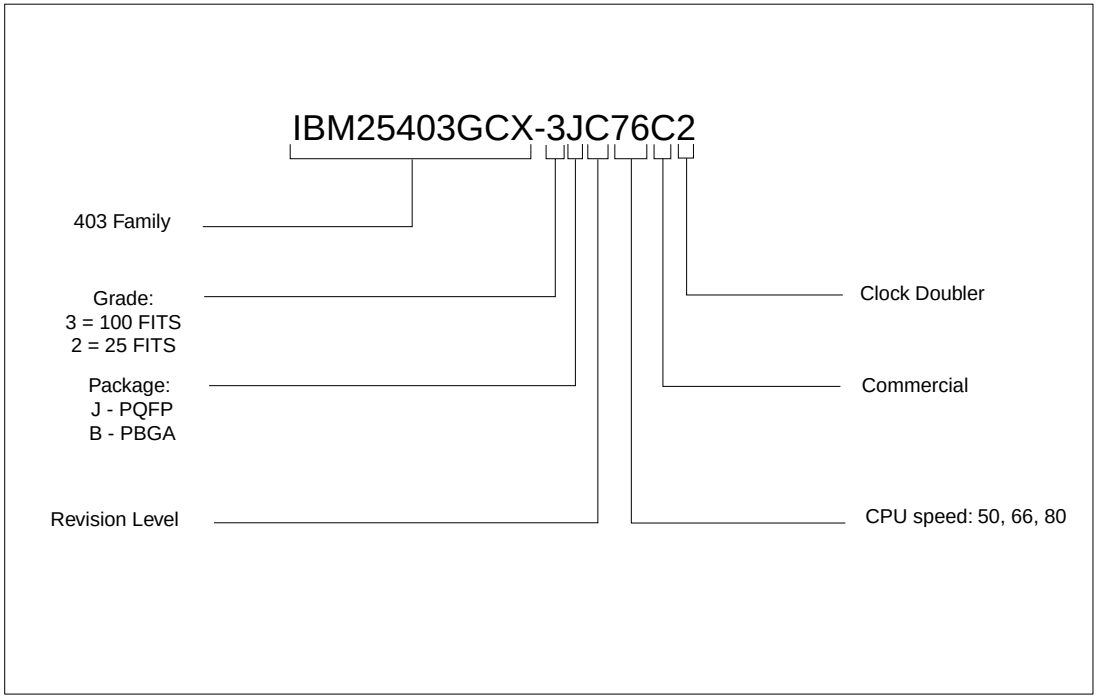
Ordering Information

This section provides the part numbering nomenclature for the 403GCX. For availability, contact your local IBM sales office.

Table 22. PPC403GCX Part Number

IBM Part Number	OEMLS Part Number	Processor Bus Frequency	Package	Revision Level
06K6173	IBM25403GCX-3JC76C2	76 MHz	PQFP	C

IBM Part Number Key for 403GCX



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