REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15								

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
15 MAY 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, FAST, CMOS, OCTAL TRANSPARENT LATCHES, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88651

SHEET 1 OF 15

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1257-2

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88651	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT533	Octal transparent latches
02	54FCT533A	Octal transparent latches

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +6.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK})	-20 mA
DC output diode current (I_{OK})	-50 mA
DC output current	±100 mA
Maximum power dissipation (P_D) 2/	500 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Case operating temperature (T_C)	-55°C to +125°C

1/ All voltages referenced to GND.
2/ Must withstand the added P_D due to short circuit test, e.g.: I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, V_{CC} = 5.0 V dc ±10% unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OH} = -300 µA	1, 2, 3	All	4.3		V
			I_{OH} = -12 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OL} = 300 µA	1, 2, 3	All		0.2	V
			I_{OL} = 32 mA	1, 2, 3	All		0.5	V
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1	All		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		1, 2, 3	All		-5.0	µA
High impedence output current	I_{OZH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		10	µA
	I_{OZL}	V_{CC} = 5.5 V, V_{IN} = GND		1, 2, 3	All		-10	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/	V_{OUT} = GND	1, 2, 3	All	-60		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \leq 0.2$ V or $V_{IN} \geq 5.3$ V, V_{CC} = 5.5 V, f_I = 0.0 MHz		1, 2, 3	All		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V 2/		1, 2, 3	All		2.0	mA
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $\overline{OE}$ = GND, $V_{IN} \geq 5.3$ V or $V_{IN} \leq 0.2$ V, Outputs open, One bit toggling: 50% duty cycle, LE = V_{CC}		3/	All		0.4	mA/MHz

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Total power supply current 4/	I_{CC}	$V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V, V_{CC} = 5.5 V, f_I = 10 MHz, Outputs open, One bit toggling: 50% duty cycle, $\overline{OE}$ = GND, LE = V_{CC}	1, 2, 3	All		5.5	mA
		V_{IN} = 3.4 V or V_{IN} = GND, V_{CC} = 5.5 V, f_I = 10 MHz, Outputs open, One bit toggling: 50% duty cycle, $\overline{OE}$ = GND, LE = V_{CC}				6.0	mA
Functional tests		See 4.3.1d	7, 8	All			
Input capacitance	C_{IN}	See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	See 4.3.1c	4	All		12	pF
Propagation delay, Dn to $\overline{On}$	t_{PLH1}, t_{PHL1}	V_{CC} = 5.0 V ±10%, C_L = 50 pF, R_L = 500Ω, See figure 4 5/	9, 10, 11	01	1.5	12.0	ns
				02	1.5	5.6	
Propagation delay, LE to $\overline{On}$	t_{PLH2}, t_{PHL2}		9, 10, 11	01	2.0	14.0	ns
				02	2.0	9.8	
Output enable time, $\overline{OE}$ to $\overline{On}$	t_{PZH}, t_{PZL}		9, 10, 11	01	1.5	12.5	ns
				02	1.5	7.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 5.0 V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output disable time, $\overline{OE}$ to $\overline{On}$	t_{PHZ}, t_{PLZ}	V_{CC} = 5.0 V ±10%, C_L = 50 pF, R_L = 500Ω, See figure 4 5/	9, 10, 11	01	1.5	8.5	ns
				02	1.5	6.5	
Setup time, Dn to LE (high or low)	t_S	V_{CC} = 5.0 V ±10%, C_L = 50 pF, R_L = 500Ω, See figure 4	9, 10, 11	01	2.0		ns
				02	2.0		
Hold time, Dn to LE (high or low)	t_h		9, 10, 11	01	3.0		ns
				02	1.5		
LE pulse width (high or low)	t_{PW}		9, 10, 11	01	6.0		ns
				02	6.0		

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed one second.

2/ TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + (I_{CCD}(f_I \times N_I + f_{CP}/2))$

where: D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
f_I = Input frequency in MHz
N_I = Number of inputs at f_I
f_{CP} = Clock frequency in MHz

5/ The minimum limits are guaranteed, if not tested, to the limits specified in table I.

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Device types	01 and 02
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	$\overline{O}_0$
3	D_0
4	D_1
5	$\overline{O}_1$
6	$\overline{O}_2$
7	D_2
8	D_3
9	$\overline{O}_3$
10	GND
11	LE
12	$\overline{O}_4$
13	D_4
14	D_5
15	$\overline{O}_5$
16	$\overline{O}_6$
17	D_6
18	D_7
19	$\overline{O}_7$
20	V_{CC}

FIGURE 1. Terminal connections.

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Device types 01 and 02			
Inputs		Outputs	
Dn	LE	$\overline{OE}$	$\overline{On}$
H	H	L	L
L	H	L	H
X	X	H	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance state

FIGURE 2. Truth table.

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Device types 01 and 02

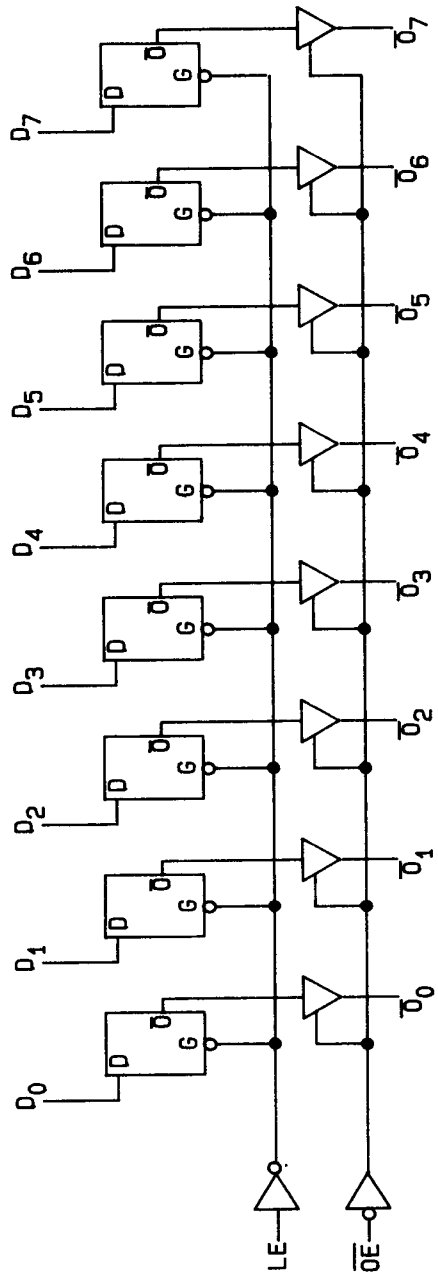
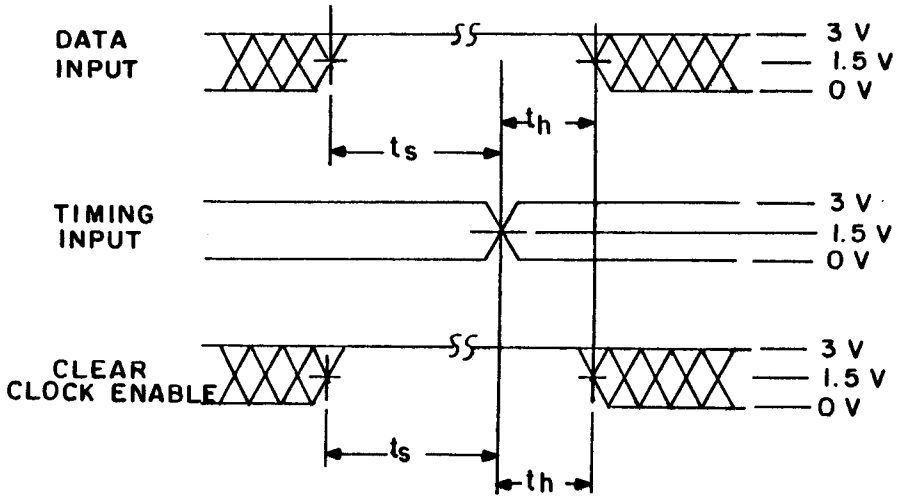
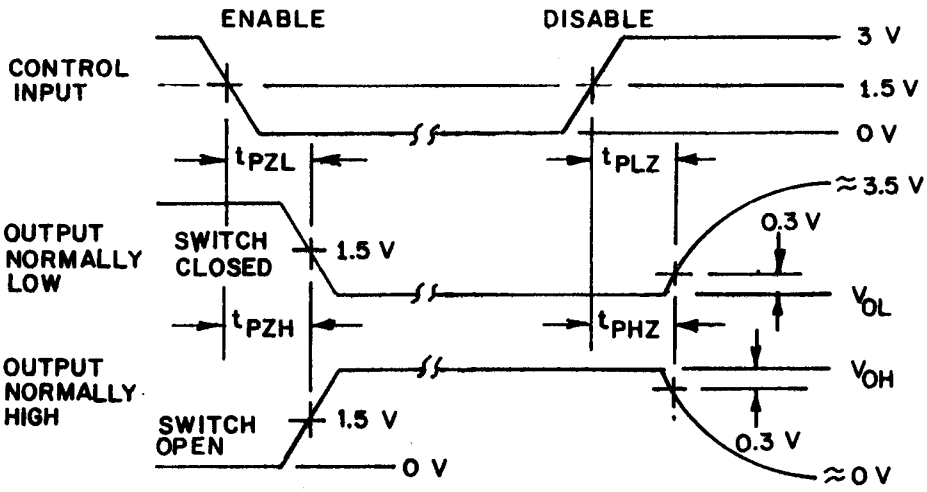


FIGURE 3. Logic diagram.



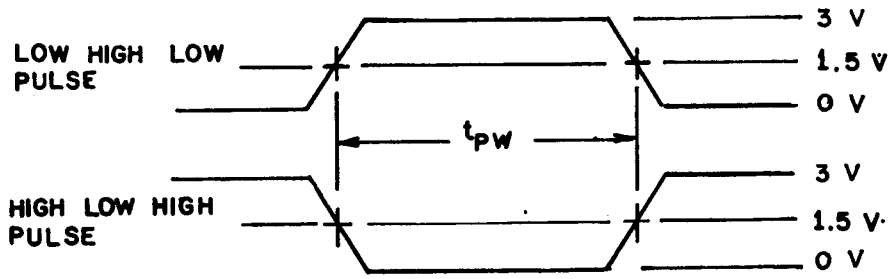
ENABLE AND DISABLE TIMES



NOTES:
1. Diagram shown for input control enable - low and input control disable - high.
2. Pulse generator for all pulses: $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

FIGURE 4. Switching waveforms and test circuit.

PULSE WIDTH



PROPAGATION DELAY

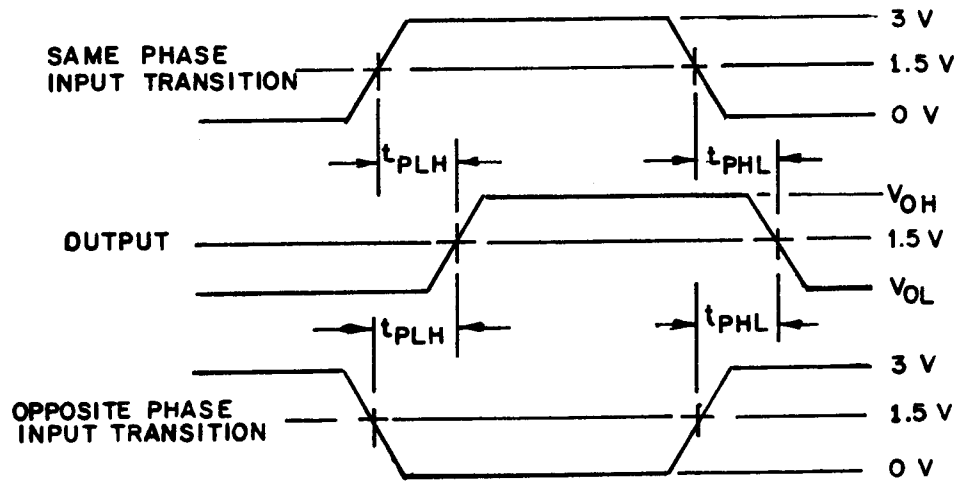
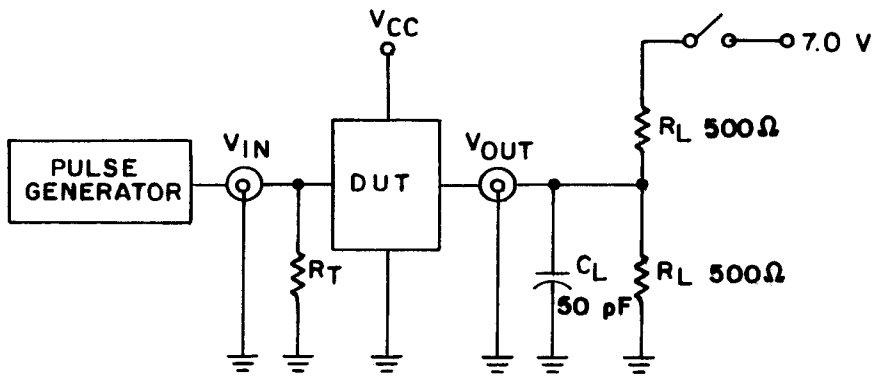


FIGURE 4. Switching waveforms and test circuit - Continued.



Switch position

Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
All other	Open

Definitions:
R_L = Load resistor see ac characteristics for value.
C_L = Load capacitance includes jig and probe capacitance:
See ac characteristics for value.
R_T = Termination should be equal to Z_{OUT} of pulse generators.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8865101RX	61772 75569	IDT54FCT533DB P54PCT533DMB
5962-8865101SX	61772	IDT54FCT533EB
5962-88651012X	61772 75569	IDT54FCT533LB P54PCT533LMB
5962-8865102RX	61772 75569	IDT54FCT533ADB P54PCT533ADMB
5962-8865102SX	61772	IDT54FCT533AEB
5962-88651022X	61772 75569	IDT54FCT533ALB P54PCT533ALMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology 3236 Scott Boulevard Santa Clara, CA 95052
75569	Performance Semiconductor Corporation 610 E. Weddle Drive Sunnyvale, CA 94089