REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET	22																							
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
17 SEPTEMBER 1990

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, MEMORY, CMOS
PARALLEL 512 X 9 FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89863

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E012

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89863	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.6	512 X 9 FIFO	80 ns
02	See 6.6	512 X 9 FIFO	65 ns
03	See 6.6	512 X 9 FIFO	50 ns
04	See 6.6	512 X 9 FIFO	40 ns
05	See 6.6	512 X 9 FIFO	30 ns
06	See 6.6	512 X 9 FIFO	25 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	D-15 (28-lead, 1.485" x .310" x .230"), dual-in-line package
Z	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
U	F-11 (28-lead, .740" x .380" x .090"), flat package

1.3 Absolute maximum ratings.

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation 1/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-M-38510, appendix C
Junction temperature (T_J) 2/	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
2/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMDs).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All		0.4	V
Input high voltage	V_{IH} 2/		1, 2, 3	All	2.2		V
Input low voltage	V_{IL} 2/		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	+10	uA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	+10	uA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA f = $1/t_{RC}$ $\overline{W}$, $\overline{R}$, D_0 - D_8 pins are toggling between 0 V and 3 V $\overline{FF}$, $\overline{XO/HF}$ = 0 mA Q_0 - Q_8 = 0 mA $\overline{MR}$, $\overline{FL/RT}$ = 3.0 V	1, 2, 3	01,02 03 04,05 06		115 130 140 147	mA
Standby current	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA All inputs = V_{IH} $\overline{FF}$, $\overline{XO/HF}$ = 0 mA Q_0 - Q_8 = 0 mA	1, 2, 3	All		30	mA
Power down current	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA All inputs = V_{CC} -0.2 V $\overline{FF}$, $\overline{XO/HF}$ = 0 mA Q_0 - Q_8 = 0 mA	1, 2, 3	All		25	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input capacitance	C_{IN} 3/	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Output capacitance	C_{OUT} 3/	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Functional tests		See 4.3.1d	7,8	All			
Read cycle time	t_{RC}	See figure 3	9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	35		
Access time	t_A		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		25	
Read recovery time	t_{RR}		9, 10, 11	01	20		ns
				02,03	15		
				04,05,06	10		
Read pulse width	t_{PR}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Read low to low Z	t_{LZR} 3/ 4/		9, 10, 11	All	3		ns
Read high to data valid	t_{DVR}		9, 10, 11	All	3		ns
Read high to high Z	t_{HZR} 3/ 4/		9, 10, 11	01,02,03		30	ns
				04		25	
				05		20	
				06		18	
Write cycle time	t_{WC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write pulse width	t_{PW}	See figure 3	9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Write high to low $\overline{Z}$	t_{HWZ} 3/ 4/		9, 10, 11	All	10		ns
Write recovery time	t_{WR}		9, 10, 11	01	20		ns
				02,03	15		
				04,05,06	10		
Data setup time	t_{SD}		9, 10, 11	01	40		ns
				02,03	30		
				04	20		
				05	18		
				06	15		
Data hold time	t_{HD}		9, 10, 11	01,02	10		ns
				03	5		
				04,05,06	0		
Master reset cycle time	t_{MRSC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	35		
Master reset pulse width	t_{PMR}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Master reset recovery time	t_{RMR}		9, 10, 11	01	20		ns
				02,03	15		
				04,05,06	10		
Read high to master reset high	t_{RPW} 3/		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write high to master reset high	t_{WPW} 3/	See figure 3	9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Retransmit cycle time	t_{RTC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	35		
Retransmit pulse width	t_{PRT}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Retransmit recovery time	t_{RTR}		9, 10, 11	01	20		ns
				02,03	15		
				04,05,06	10		
Master reset to empty flag low	t_{EFL}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Master reset to half-full flag high	t_{HFH}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Master reset to full flag high	t_{FFH}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Read low to empty flag low	t_{REF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Read high to full flag high	t_{RFF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write high to empty flag high	t_{WEF}	See figure 3	9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Write low to full flag low	t_{WFF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Write low to half-full flag low	t_{WHF}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Read high to half-full flag high	t_{RHF}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Effective read from write high	t_{RAE} 3/		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Effective read pulse width after empty flag high	t_{RPE}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Effective write from read high	t_{WAF} 3/		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Effective write pulse width after full flag high	t_{WPF}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Expansion out low delay from clock	t_{XOL}	See figure 3	9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		25	
Expansion out high delay from clock	t_{XOH}		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		25	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, and the output load on figure 4.
2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510), shall be subjected to and pass the Internal Moisture Content Test, (see method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

Device types	All	
Case outlines	U, X, Y	Z
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D_8	$\overline{W}$
3	D_3	D_8
4	D_2	D_3
5	D_1	D_2
6	D_0	D_1
7	$\overline{XI}$	D_0
8	$\overline{FF}$	$\overline{XI}$
9	Q_0	$\overline{FF}$
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	$\overline{R}$	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	$\overline{R}$
19	Q_7	Q_4
20	$\overline{XO}/\overline{HF}$	Q_5
21	$\overline{EF}$	Q_6
22	$\overline{MR}$	Q_7
23	FL/$\overline{RT}$	$\overline{XO}/\overline{HF}$
24	D_7	$\overline{EF}$
25	D_6	$\overline{MR}$
26	D_5	FL/$\overline{RT}$
27	D_4	NC
28	V_{CC}	D_7
29	-	D_6
30	-	D_5
31	-	D_4
32	-	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{MR}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment 1/	Increment 1/	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load truth table
Depth expansion/compound expansion mode

Mode	Inputs			Internal status		Outputs	
	$\overline{MR}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	1/	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{1}$/	Location zero	Location zero	0	1
Read/Write	1	X	$\overline{1}$/	X	X	X	X

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

Note: $\overline{MR}$ = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit $\overline{EF}$ = Empty flag output, $\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output

FIGURE 2. Truth tables.

Asynchronous read and write timing diagram

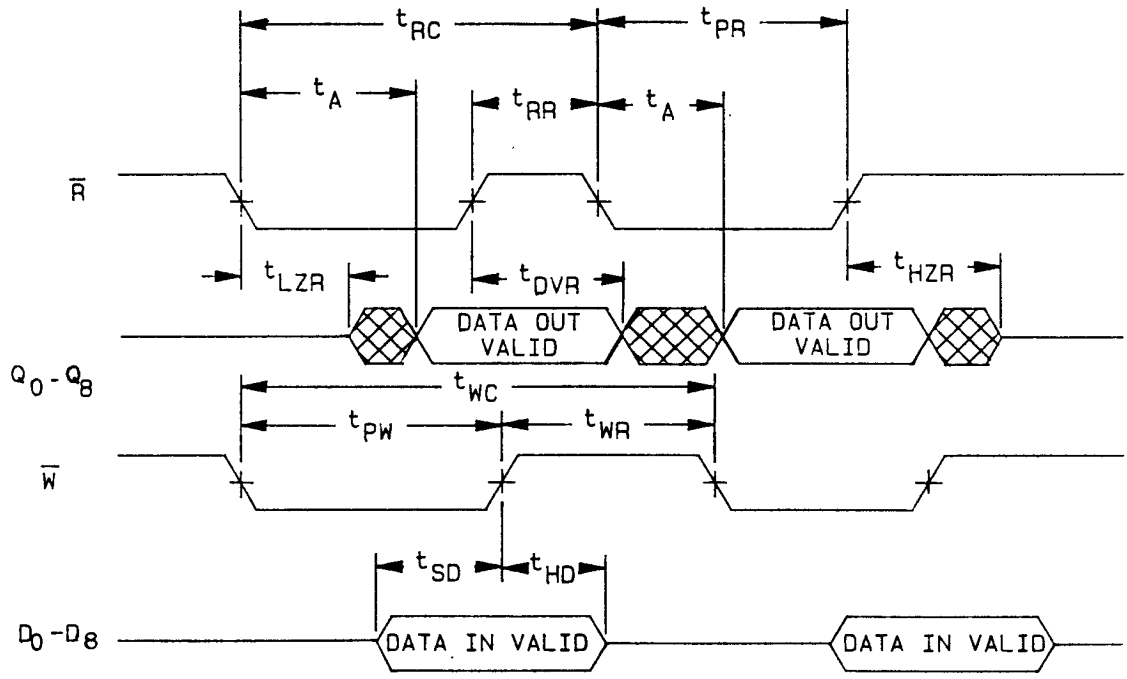
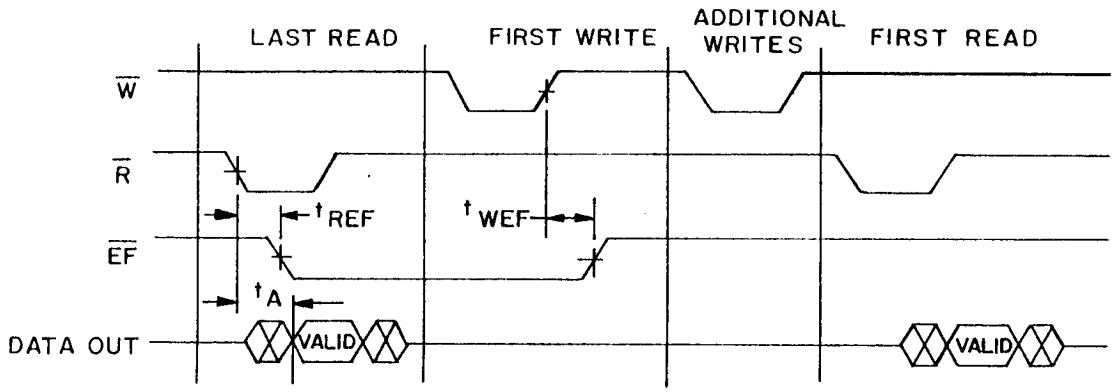
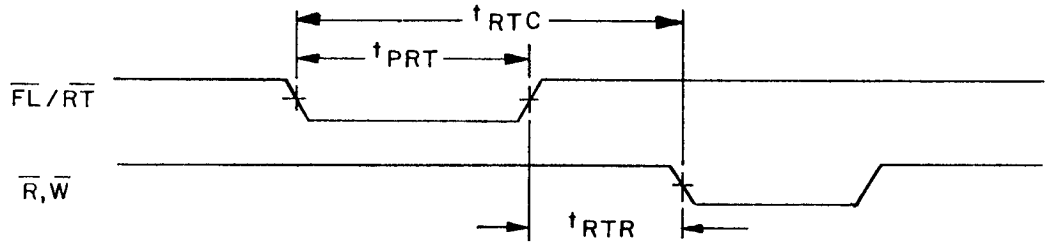


FIGURE 3. Timing waveforms.

Last read to first write empty flag timing diagram



Retransmit timing diagram

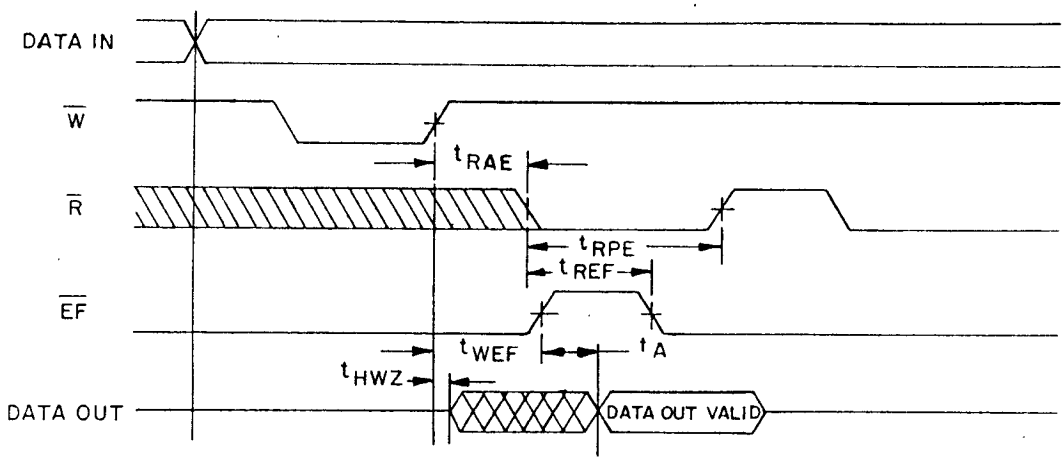


NOTES:

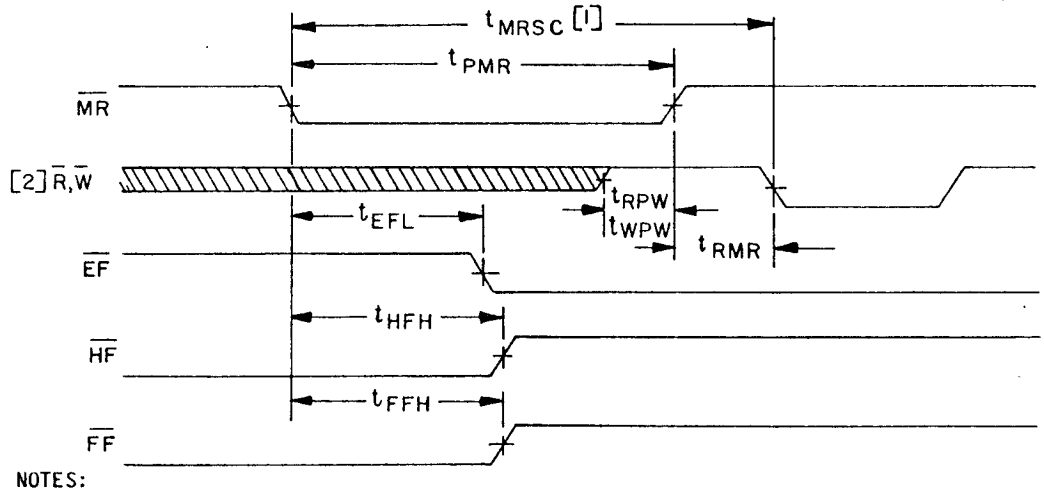
1. $t_{RTC} = t_{PRT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointer, but flags will be valid at t_{RTC}.

FIGURE 3. Timing waveforms - Continued.

Empty flag and read bubble-through mode timing diagram.



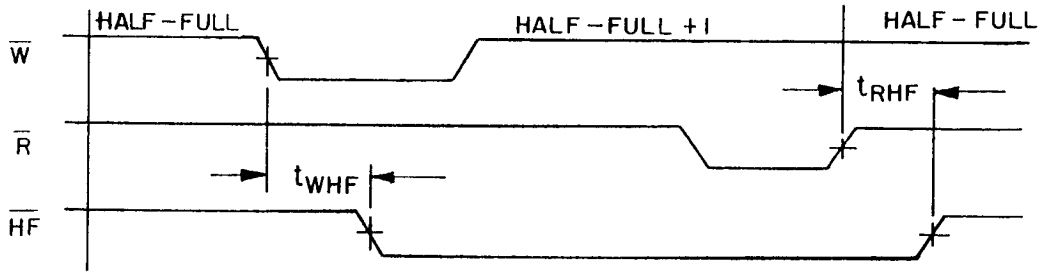
Master reset timing diagram.



NOTES:
1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.

FIGURE 3. Timing waveforms - Continued.

Half-full flag timing diagram



Last write to first read full flag timing diagram

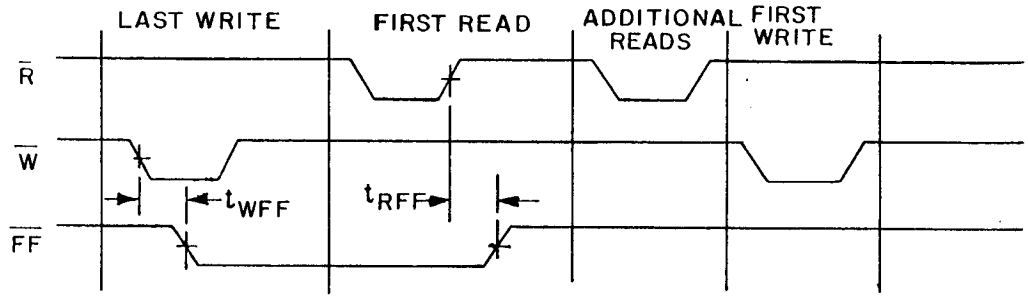


FIGURE 3. Timing waveforms - Continued.

Full flag and write bubble-through mode timing diagram

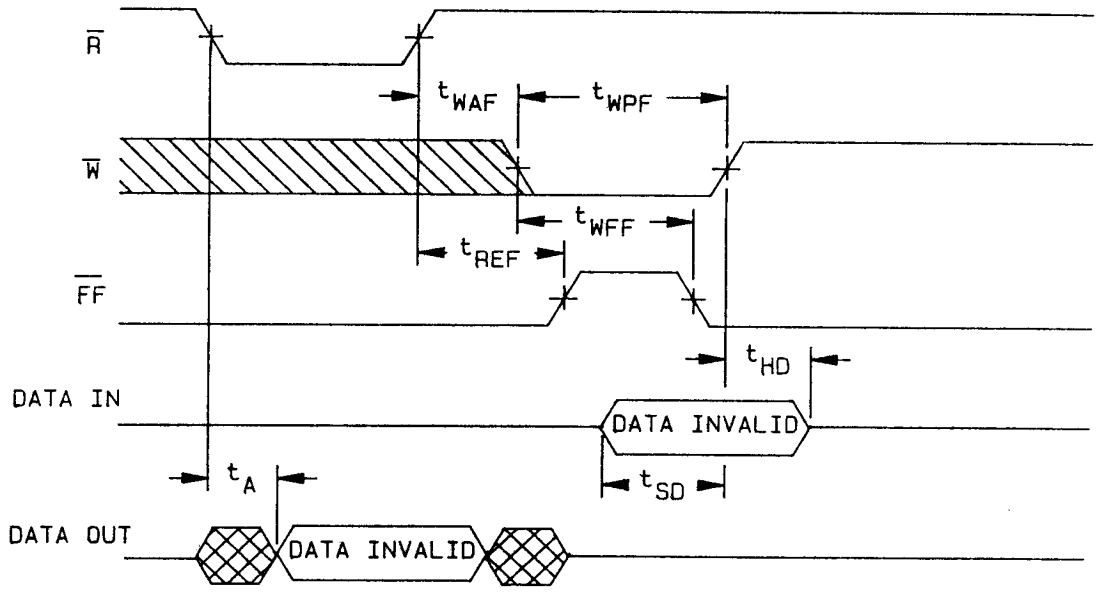
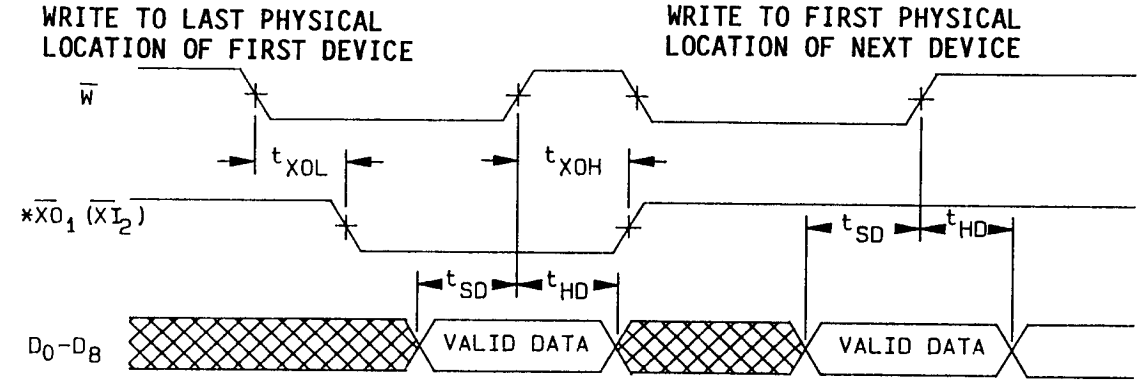
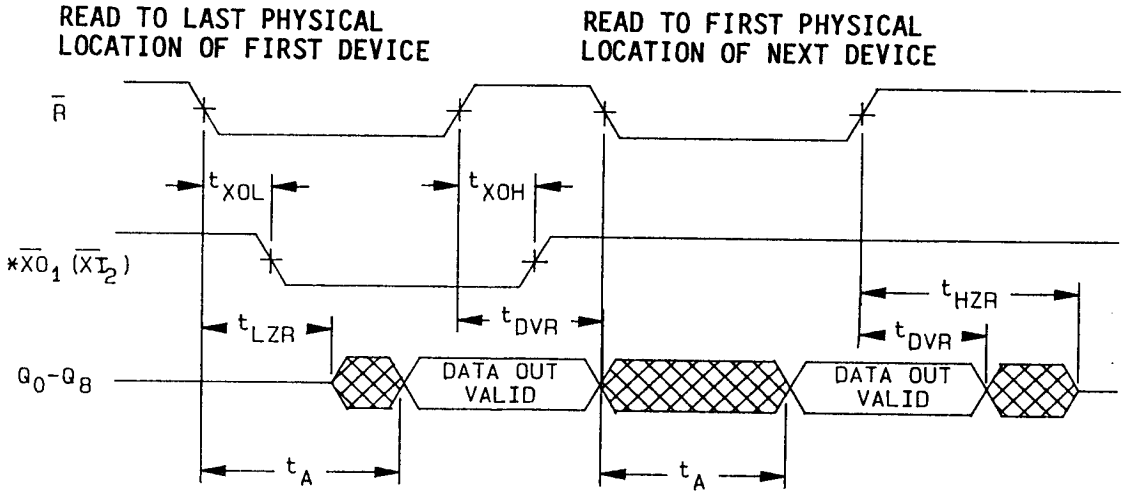


FIGURE 3. Timing waveforms - Continued.

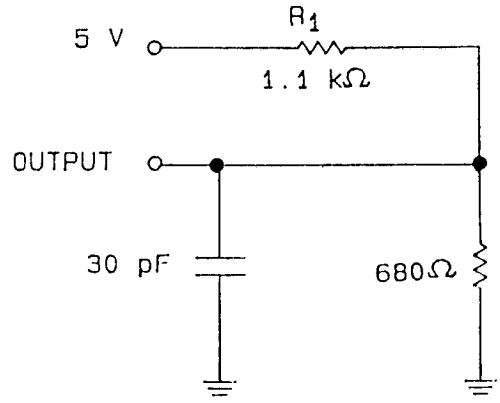
Expansion timing diagram





*Expansion out of device type first (XO_1) is connected to expansion in of device type next ($\overline{XI}_2$).

FIGURE 3. Timing waveforms - Continued.



Circuit A
Output load

*Including scope and jig (minimum values)

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuit and test conditions.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A,8B 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, 8***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroup 1 and 7.
** For subgroup 4, see 4.3.1c.
*** For subgroups 7 and 8, see 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMDs. All proposed changes to existing SMDs will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

Military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8986301UX	61772	IDT7201SA80XEB
5962-8986301XX	61772	IDT7201SA80DB
5962-8986301YX	61772	IDT7201SA80TCB
5962-8986301ZX	61772	IDT7201SA80LB
5962-8986302UX	65786 61772	CY7C421-65KMB IDT7201SA65XEB
5962-8986302XX	65786 61772	CY7C420-65DMB IDT7201SA65DB
5962-8986302YX	65786 61772	CY7C421-65DMB IDT7201SA65TCB
5962-8986302ZX	65786 61772	CY7C421-65LMB IDT7201SA65LB
5962-8986303UX	65786 61772	CY7C421-50KMB IDT7201SA50XEB
5962-8986303XX	65786 61772	CY7C420-50DMB IDT7201SA50DB
5962-8986303YX	65786 61772	CY7C421-50DMB IDT7201SA50TCB
5962-8986303ZX	65786 61772	CY7C421-50LMB IDT7201SA50LB
5962-8986304UX	65786 61772	CY7C421-40KMB IDT7201SA40XEB
5962-8986304XX	65786 61772	CY7C420-40DMB IDT7201SA40DB

Military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8986304YX	65786 61772	CY7C421-40DMB IDT7201SA40TCB
5962-8986304ZX	65786 61772	CY7C421-40LMB IDT7201SA40LB
5962-8986305UX	65786 61772	CY7C421-30KMB IDT7201SA30XEB
5962-8986305XX	65786 61772	CY7C420-30DMB IDT7201SA30DB
5962-8986305YX	65786 61772	CY7C421-30DMB IDT7201SA30TCB
5962-8986305ZX	65786 61772	CY7C421-30LMB IDT7201SA30LB
5962-8986306UX	65786	CY7C421-25KMB
5962-8986306XX	65786	CY7C420-25DMB
5962-8986306YX	65786	CY7C421-25DMB
5962-8986306ZX	65786	CY7C421-25LMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134
61772	Integrated Device Technology, Incorporated 1556 Moffett Boulevard Salinas, CA 93905 Point of contact: 3236 Scott Boulevard Santa Clara, CA 95054