REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																		*	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-08-31

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, CMOS, 512 X 18 PARALLEL FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92101
A	67268	

SHEET 1 OF 33

DESC FORM 193
JUL 91

5962-E644-92

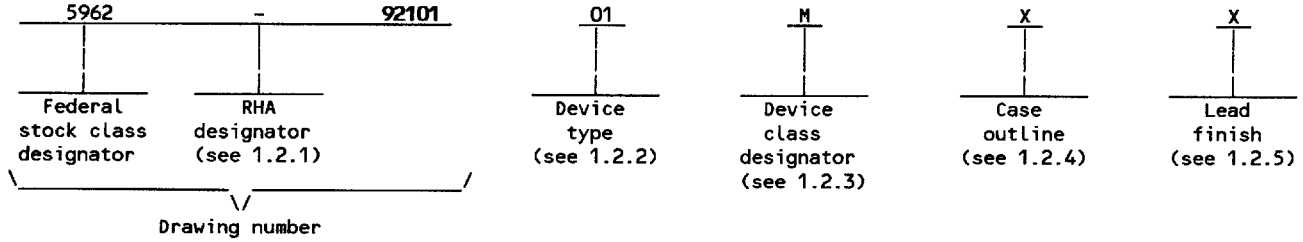
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0005362 058

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Clock cycle time (min)
01		512 x 18 CMOS parallel FIFO	50 ns
02		512 x 18 CMOS parallel FIFO	35 ns
03		512 x 18 CMOS parallel FIFO	25 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-PM	68 2/	Grid array
Y	See figure 1	68	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

2/ 68 = actual number of pins used, not maximum listed in MIL-STD-1835.

1.3 Absolute maximum ratings. 3/

Terminal voltage with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 4/	1.25 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	20 °C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (GND)	0 V
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum 5/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ Must withstand the added P_D due to short circuit test e.g., I_{OS}.

5/ -1.5 V undershoots are allowed for 10 ns once per cycle.

6/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Values will be added when they become available.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Input leakage current	I_{LI}	$0.4\ V \le V_{IN} \le V_{CC}$	1,2,3	All	-10	+10	µA
Output leakage current	I_{LO}	$\overline{OE} \ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$	1,2,3	All	-10	+10	µA
Output high voltage	V_{OH}	I_{OH} = -2 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 8 mA	1,2,3	All		0.4	V
Active power supply current	I_{CC1}	f = 20 MHz, outputs open	1,2,3	All		250	mA
Average standby current	I_{CC2}	All inputs = V_{CC} - 0.2 V, except RCLK and WCLK which are free-running, f = 20 MHz, outputs open	1,2,3	All		85	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.4.1e	4	All		10	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz, with output deselected ($\overline{OE}$ = high), T_A = +25°C, see 4.4.1e	4	All		10	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
Clock cycle frequency	fs	C_L = 30 pF, input pulse levels = GND to 3.0 V; input rise/fall times = 3 ns; input timing reference levels = 1.5 V; output timing reference levels =1.5 V; see figure 4 and 5	9,10,11	01		20	MHz
				02		28.6	
				03		40	
Data access time	t_A		9,10,11	01	3	25	ns
				02	3	20	
				03	3	15	
Clock cycle time	t_{CLK}		9,10,11	01	50		ns
				02	35		
				03	25		
Clock high time	t_{CLKH}		9,10,11	01	20		ns
				02	14		
				03	10		
Clock low time	t_{CLKL}		9,10,11	01	20		ns
				02	14		
				03	10		
Data setup time	t_{DS}		9,10,11	01	10		ns
				02	7		
				03	6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Data hold time	t_{DH}	C_L = 30 pF, input pulse levels = GND to 3.0 V; input rise/fall times = 3 ns; Input timing reference levels = 1.5 V; output timing reference levels = 1.5 V; see figure 4 and 5	9,10,11	01,02	2		ns
				03	1		
Enable setup time	t_{ENS}		9,10,11	01	10		ns
				02	7		
				03	6		
Enable hold time	t_{ENH}		9,10,11	01,02	2		ns
				03	1		
Reset pulse width 1/	t_{RS}		9,10,11	01	50		ns
				02	35		
				03	25		
Reset setup time	t_{RSS}		9,10,11	01	30		ns
				02	20		
				03	15		
Reset recovery time	t_{RSR}		9,10,11	01	30		ns
				02	20		
				03	15		
Reset to flag and output time	t_{RSF}		9,10,11	01		50	ns
				02		45	
				03		40	
Output enable to output in low Z 2/	t_{OLZ}		9,10,11	All	0		ns
Output enable to output valid	t_{OE}		9,10,11	01		20	ns
				02		15	
				03		12	
Output enable to output in high Z 2/	t_{OHZ}		9,10,11	01	1	20	ns
				02	1	15	
				03	1	12	
First read latency time	t_{FRL}		9,10,11	All		3/	ns

See footnotes at end of table.

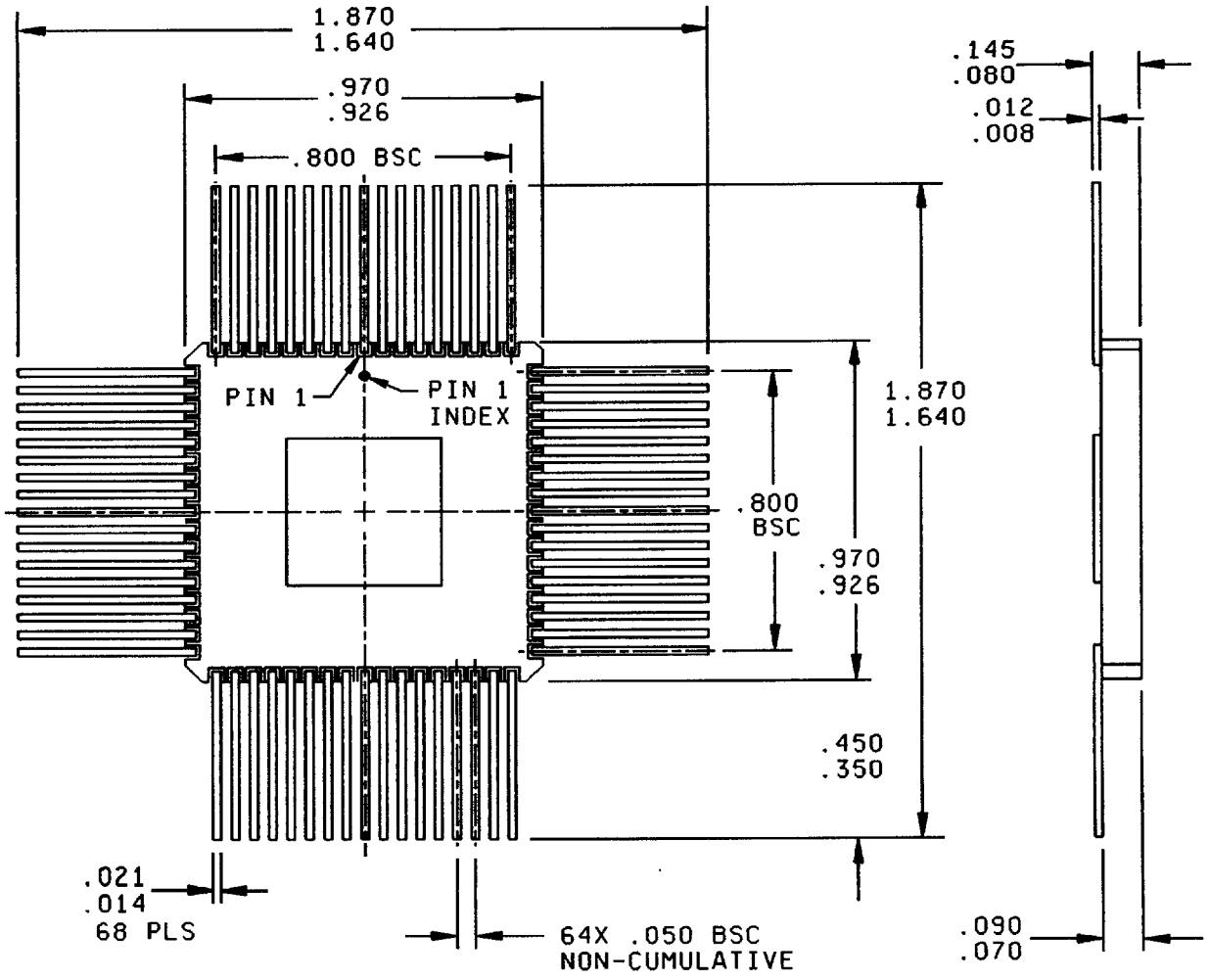
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Write clock to full flag	t_{WFF}	C_L = 30 pF, input pulse levels = GND to 3.0 V; input rise/fall times = 3 ns; Input timing reference levels = 1.5 V; output timing reference levels = 1.5 V; see figure 4 and 5	9,10,11	01		30	ns
				02		20	
				03		15	
Read clock to empty flag	t_{REF}		9,10,11	01		30	ns
				02		20	
				03		15	
Clock to programmable almost-empty flag	t_{PAE}		9,10,11	01,02		40	ns
				03		35	
Clock to programmable almost-full flag	t_{PAF}		9,10,11	01,02		40	ns
				03		35	
Clock to half-full flag	t_{HF}		9,10,11	01,02		40	ns
				03		35	
Clock to expansion out	t_{XO}		9,10,11	01		30	ns
				02		20	
				03		15	
Expansion in pulse width	t_{XI}		9,10,11	01	20		ns
				02	14		
				03	10		
Expansion in setup time	t_{XIS}		9,10,11	01	20		ns
				02	15		
				03	10		
Skew time between read clock and write clock for full flag	t_{SKEW1}		9,10,11	01	20		ns
				02	18		
				03	16		
Skew time between read clock and write clock for empty flag	t_{SKEW2}		9,10,11	01	20		ns
				02	18		
				03	16		

1/ Pulse widths less than the minimum values specified are not allowed.

2/ If not tested, shall be guaranteed to the limits specified in table I.

3/ When $t_{SKEW2} \ge$ the minimum limit, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW2} <$ the minimum limit, t_{FRL} (maximum) = either $2t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The latency timing applies only at the empty boundary (EF = LOW).



Inch	mm	Inch	mm
008	.20	.350	8.89
.012	.30	.450	11.43
.014	.36	.800	20.32
.021	.53	.926	23.52
.050	1.27	.970	24.64
.080	2.03	1.640	41.66
.090	2.29	1.870	47.50
.145	3.68		

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for information only.

FIGURE 1. Case outline.

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		REVISION LEVEL	SHEET 9

Case outline X

Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	V_{CC}	F10	$\overline{FF}$
A3	Q14	F11	$\overline{WXO/HF}$
A4	GND	G1	$\overline{REN}$
A5	Q11	G2	$\overline{LD}$
A6	Q10	G10	$\overline{PAF}$
A7	GND	G11	$\overline{RXI}$
A8	Q7	H1	GND
A9	Q6	H2	RCLK
A10	GND	H10	$\overline{WXI}$
B1	GND	H11	V_{CC}
B2	Q15	J1	D16
B3	Q13	J2	D17
B4	Q12	J10	WCLK
B5	V_{CC}	J11	$\overline{WEN}$
B6	Q9	K1	D15
B7	Q8	K2	D14
B8	V_{CC}	K3	D12
B9	Q5	K4	D10
B10	Q4	K5	V_{CC}
B11	V_{CC}	K6	GND
C1	Q17	K7	D6
C2	Q16	K8	D4
C10	Q2	K9	D2
C11	Q3	K10	$\overline{PAE}$
D1	$\overline{EF}$	K11	$\overline{FL}$
D2	V_{CC}	L2	D13
D10	Q1	L3	D11
D11	GND	L4	D9
E1	V_{CC}	L5	D8
E2	GND	L6	D7
E10	$\overline{RXO}$	L7	D5
E11	Q0	L8	D3
F1	$\overline{OE}$	L9	D1
F2	$\overline{RS}$	L10	D0

FIGURE 2. Terminal connections.

Case outline Y

Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Q15	35	$\overline{PAE}$
2	GND	36	$\overline{FL}$
3	Q16	37	$\overline{WCLK}$
4	Q17	38	$\overline{WEN}$
5	V_{CC}	39	$\overline{WXI}$
6	$\overline{EF}$	40	V_{CC}
7	GND	41	$\overline{PAF}$
8	V_{CC}	42	$\overline{RXI}$
9	$\overline{RS}$	43	$\overline{FF}$
10	$\overline{OE}$	44	$\overline{WXO/FF}$
11	$\overline{LD}$	45	$\overline{RXO}$
12	$\overline{REN}$	46	Q0
13	RCLK	47	Q1
14	GND	48	GND
15	D17	49	Q2
16	D16	50	Q3
17	D15	51	V_{CC}
18	D14	52	Q4
19	D13	53	GND
20	D12	54	Q5
21	D11	55	Q6
22	D10	56	V_{CC}
23	D9	57	Q7
24	V_{CC}	58	Q8
25	D8	59	GND
26	GND	60	Q9
27	D7	61	Q10
28	D6	62	V_{CC}
29	D5	63	Q11
30	D4	64	Q12
31	D3	65	GND
32	D2	66	Q13
33	D1	67	Q14
34	D0	68	V_{CC}

FIGURE 2. Terminal connections - Continued.

No. of words in FIFO 1/ 2/	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	H	H	H	L	L
1 to n	H	H	H	L	H
(n+1) to 256	H	H	H	H	H
257 to (512-(m+1))	H	H	L	H	H
(512-m) to 511	H	L	L	H	H
512	L	L	L	H	H

1/ n = empty offset (default values = 63).

2/ m = full offset (default values = 63).

FIGURE 3. Truth table.

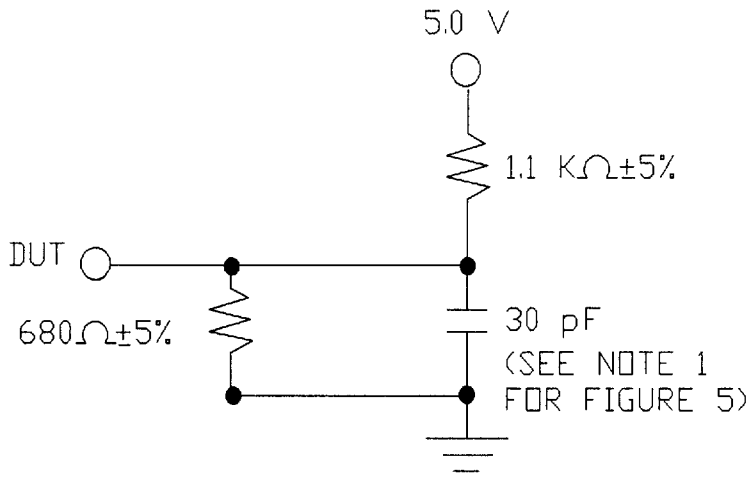


FIGURE 4. Output load circuit.

RESET TIMING (SEE NOTE 2)

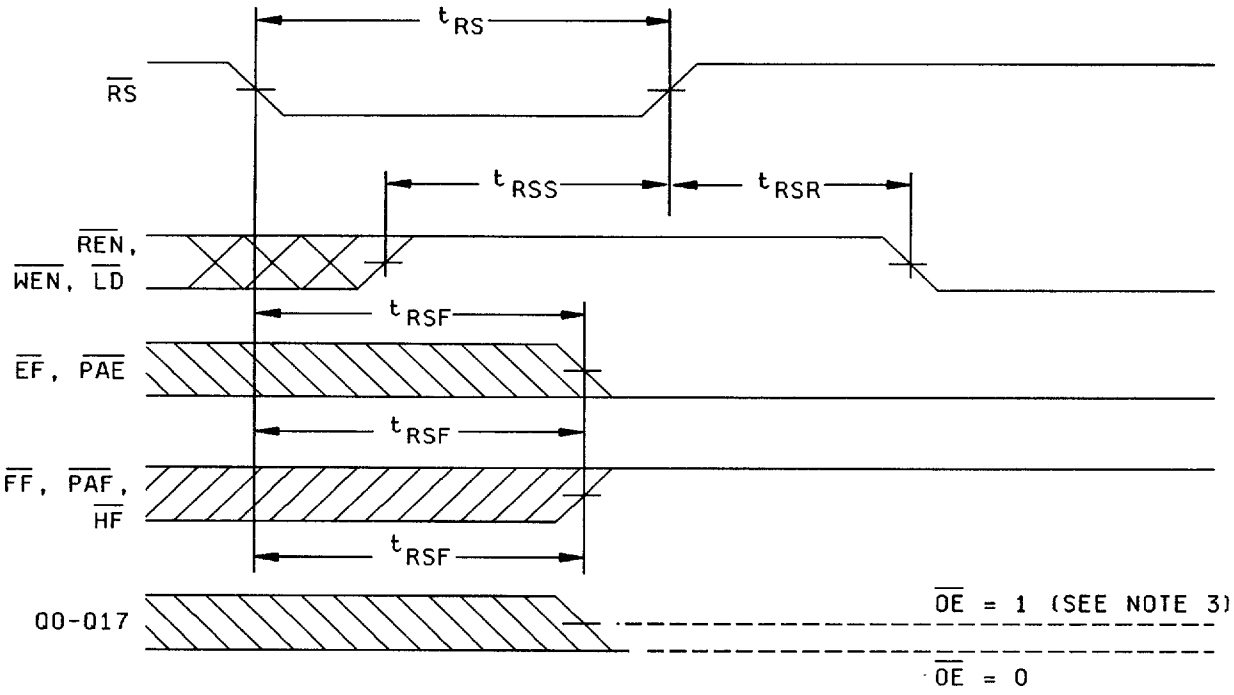


FIGURE 5. Timing waveforms.

WRITE CYCLE TIMING

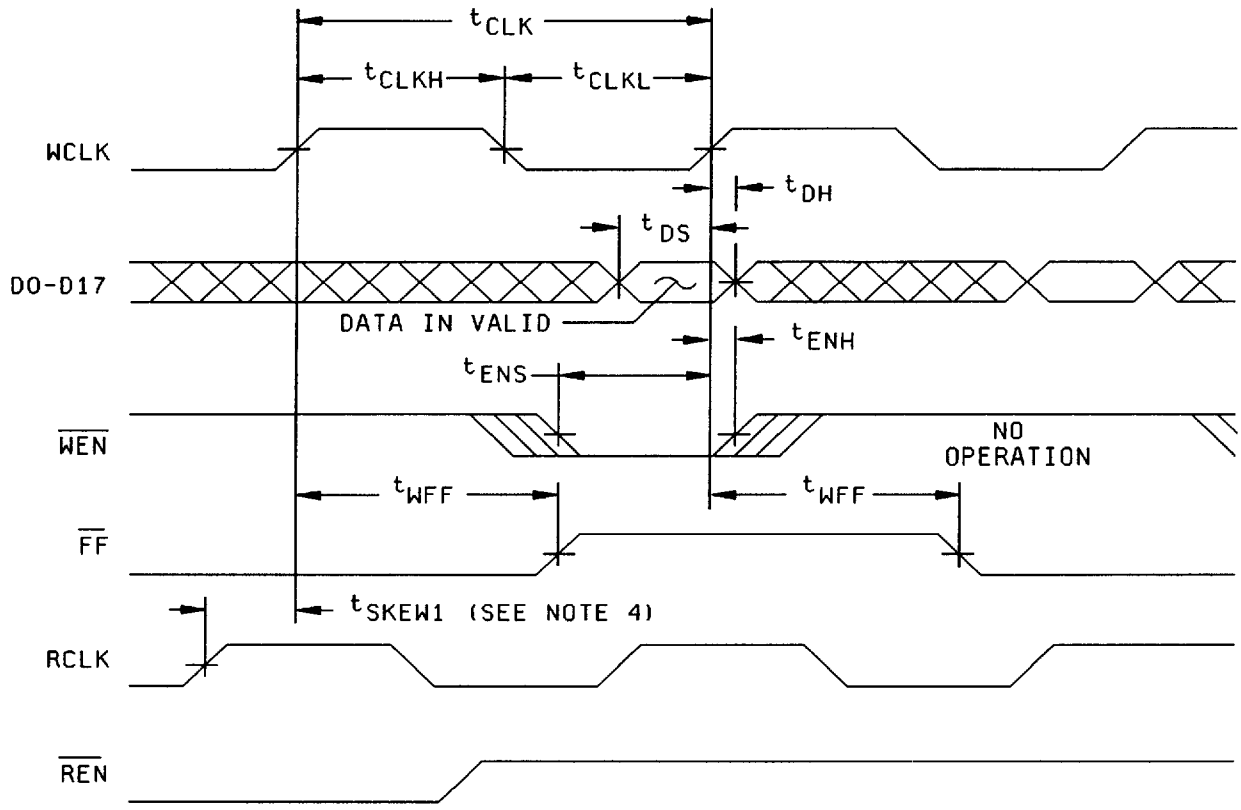


FIGURE 5. Timing waveforms - Continued.

READ CYCLE TIMING

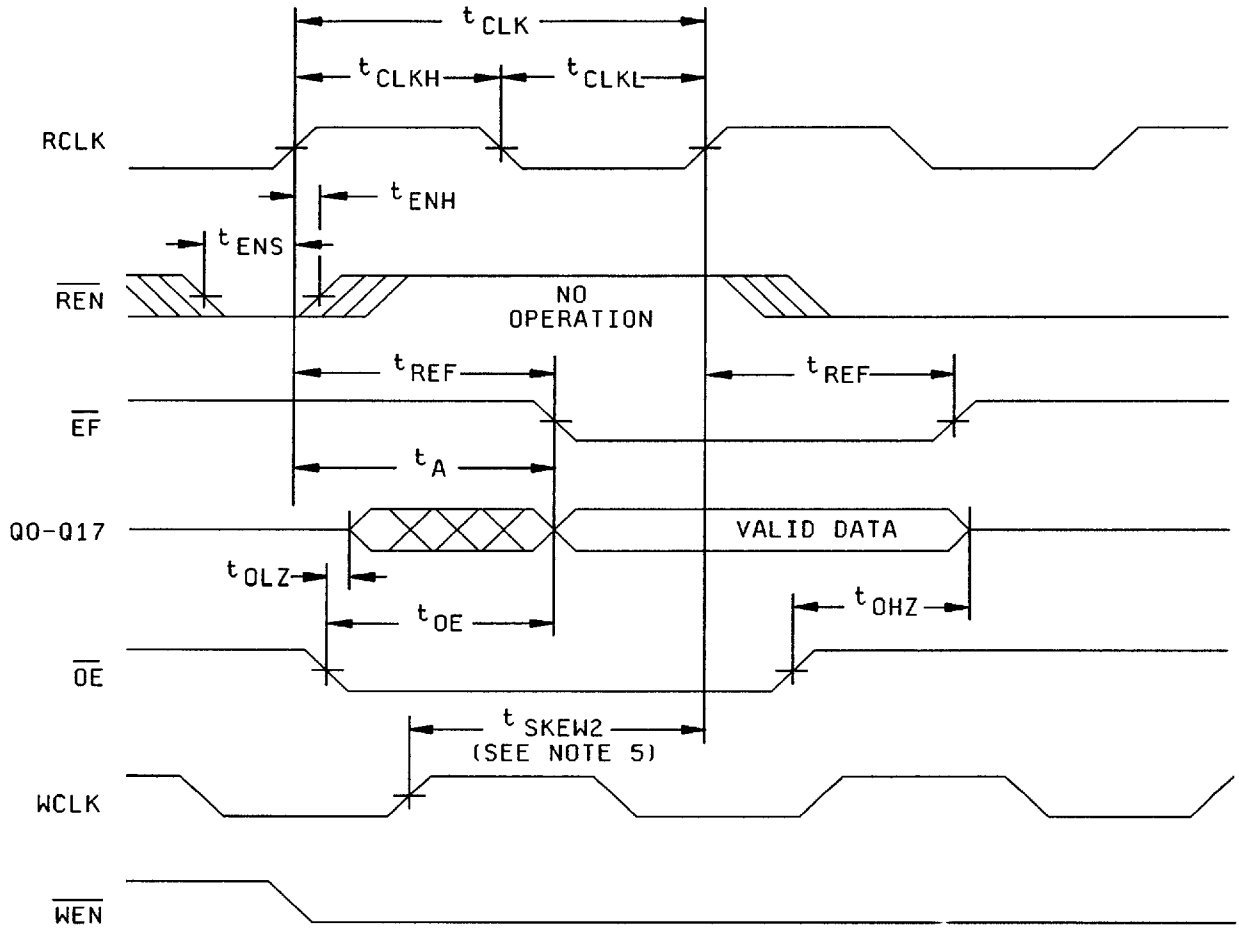


FIGURE 5. Timing waveforms - Continued.

FIRST DATA WORD LATENCY AFTER RESET WITH
SIMULTANEOUS READ AND WRITE

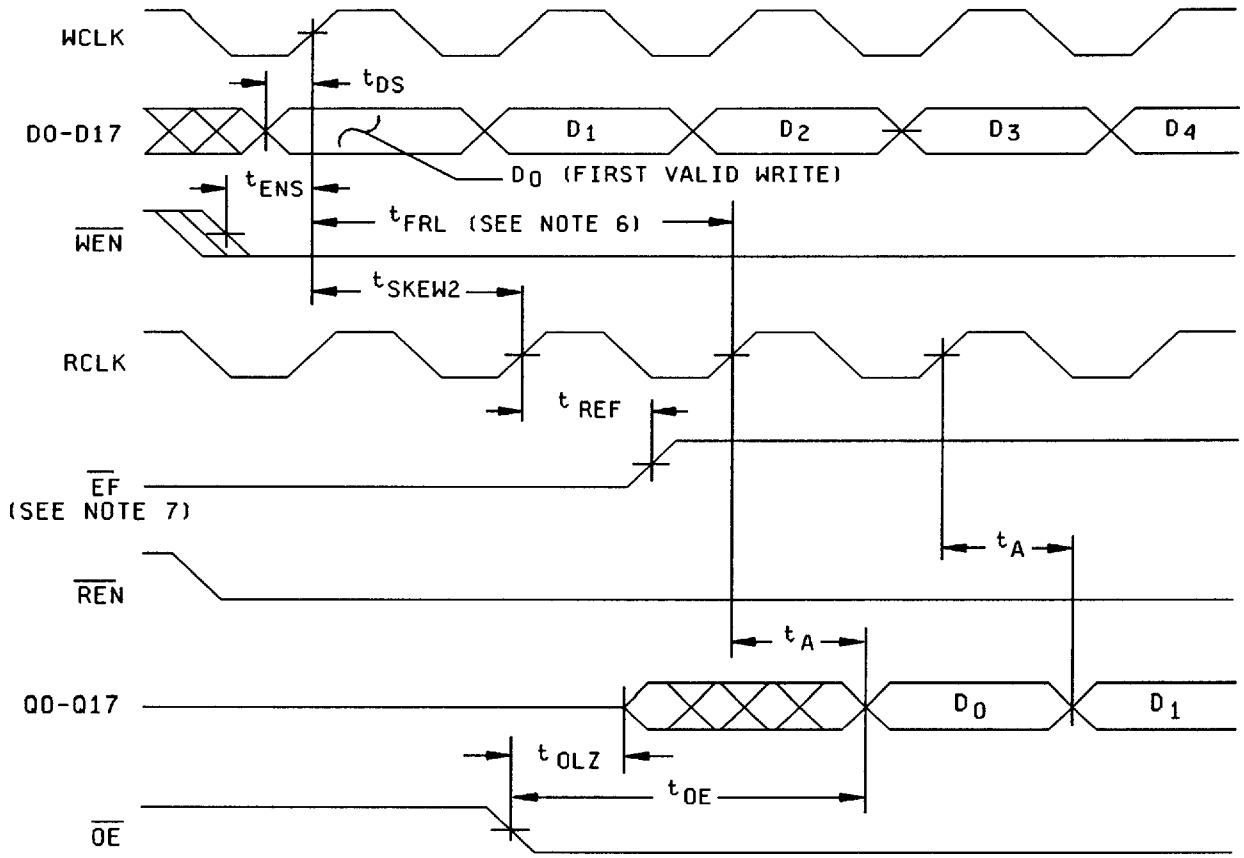


FIGURE 5. Timing waveforms - Continued.

FULL FLAG TIMING

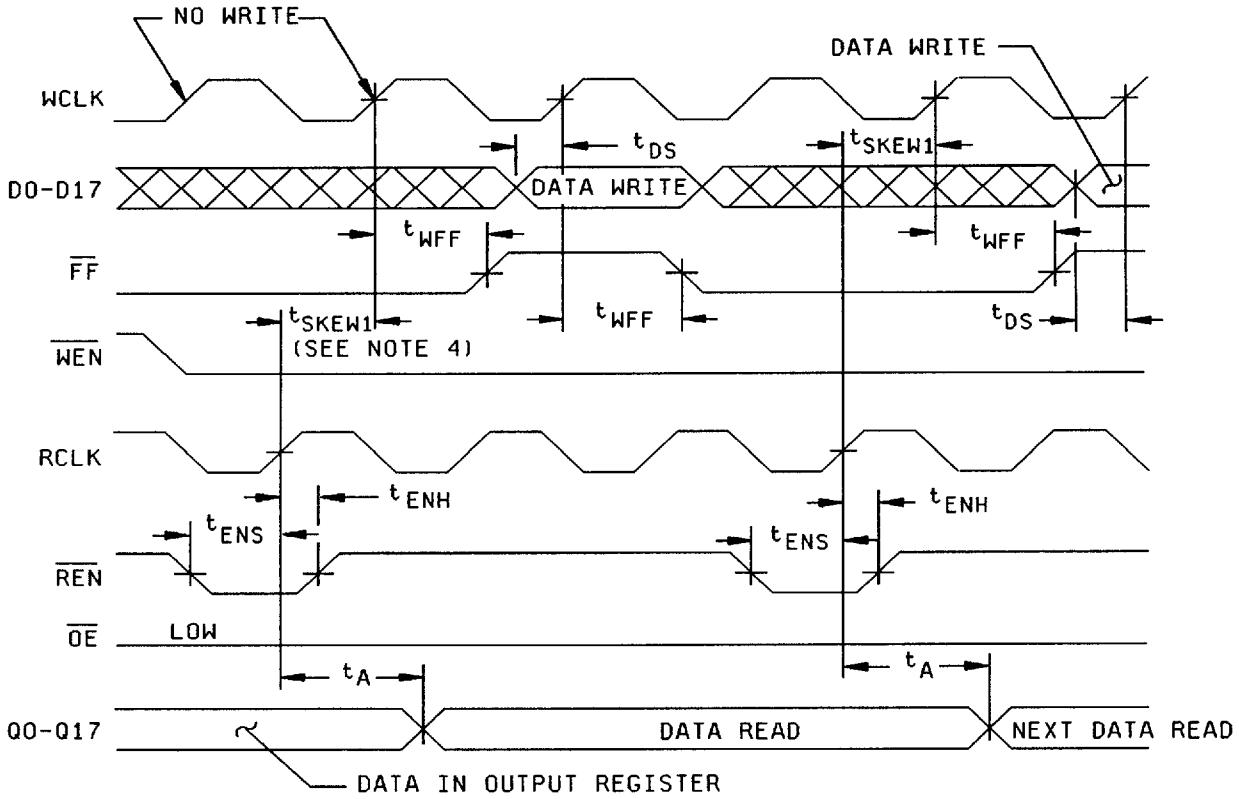


FIGURE 5. Timing waveforms - Continued.

EMPTY FLAG TIMING

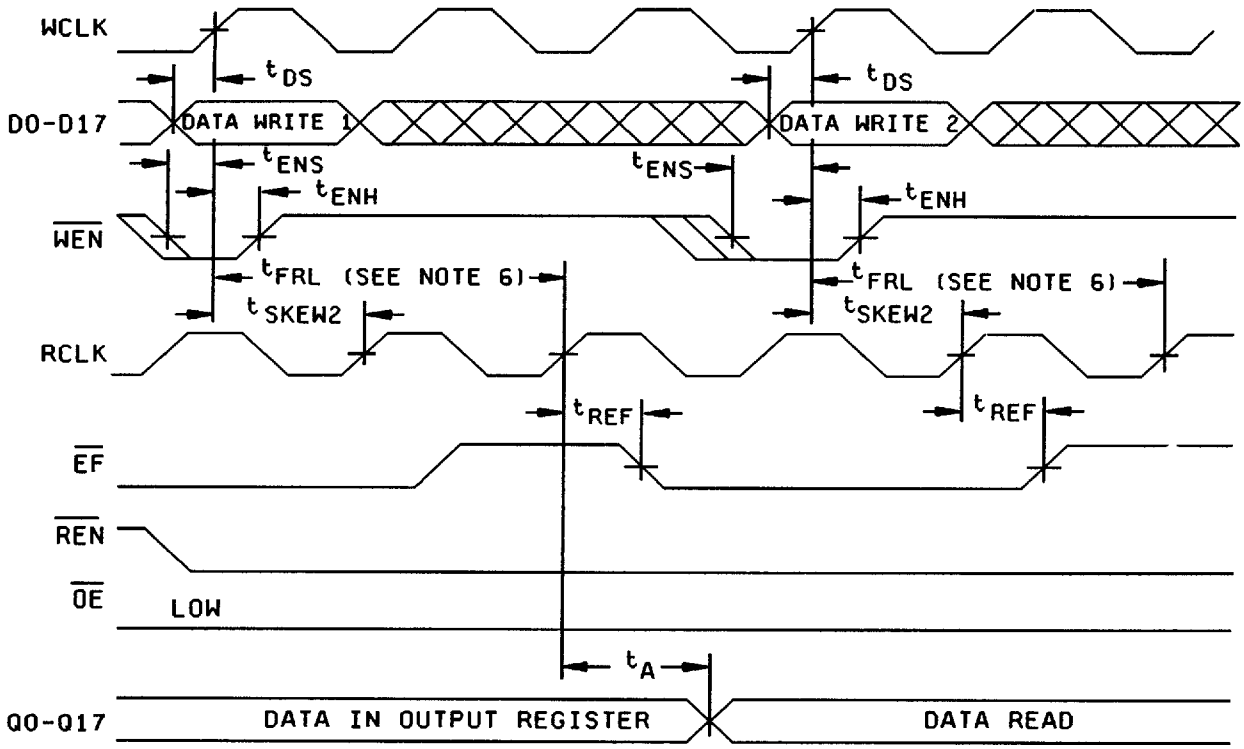


FIGURE 5. Timing waveforms - Continued.

WRITE PROGRAMMABLE REGISTERS

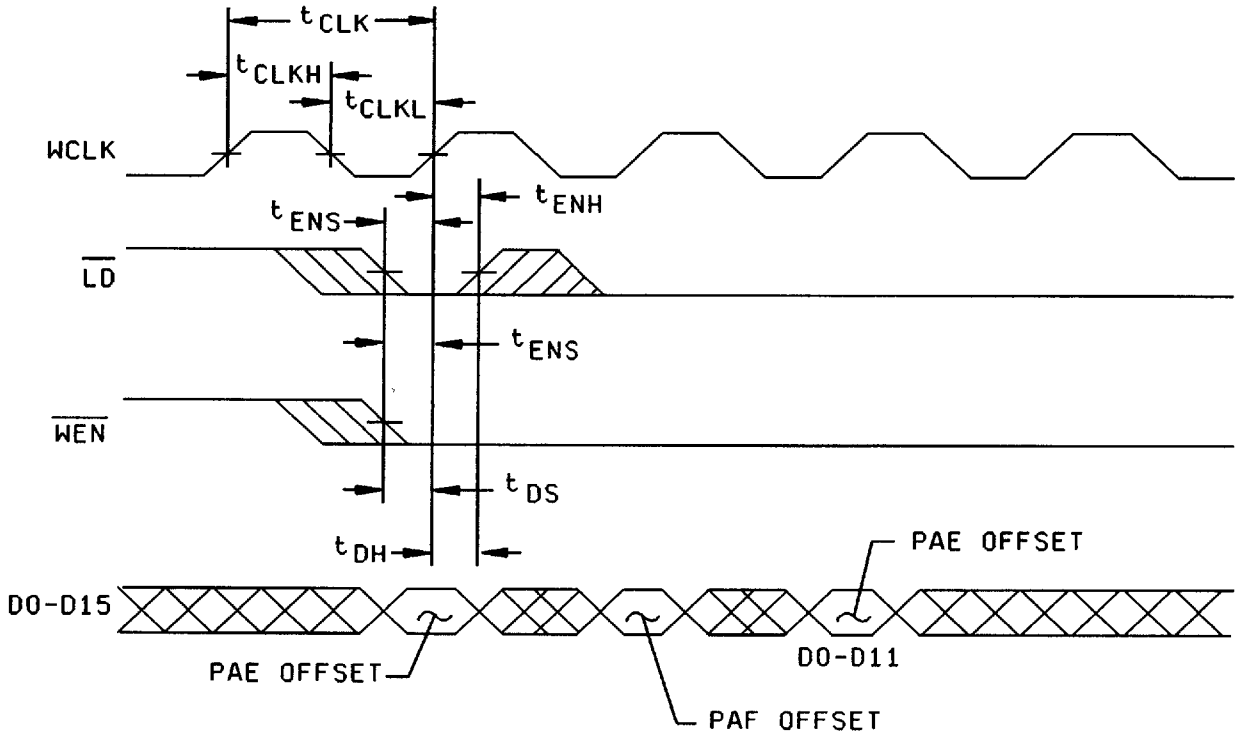


FIGURE 5. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92101
		REVISION LEVEL	SHEET 19

DESC FORM 193A
JUL 91

9004708 0005380 073

READ PROGRAMMABLE REGISTERS

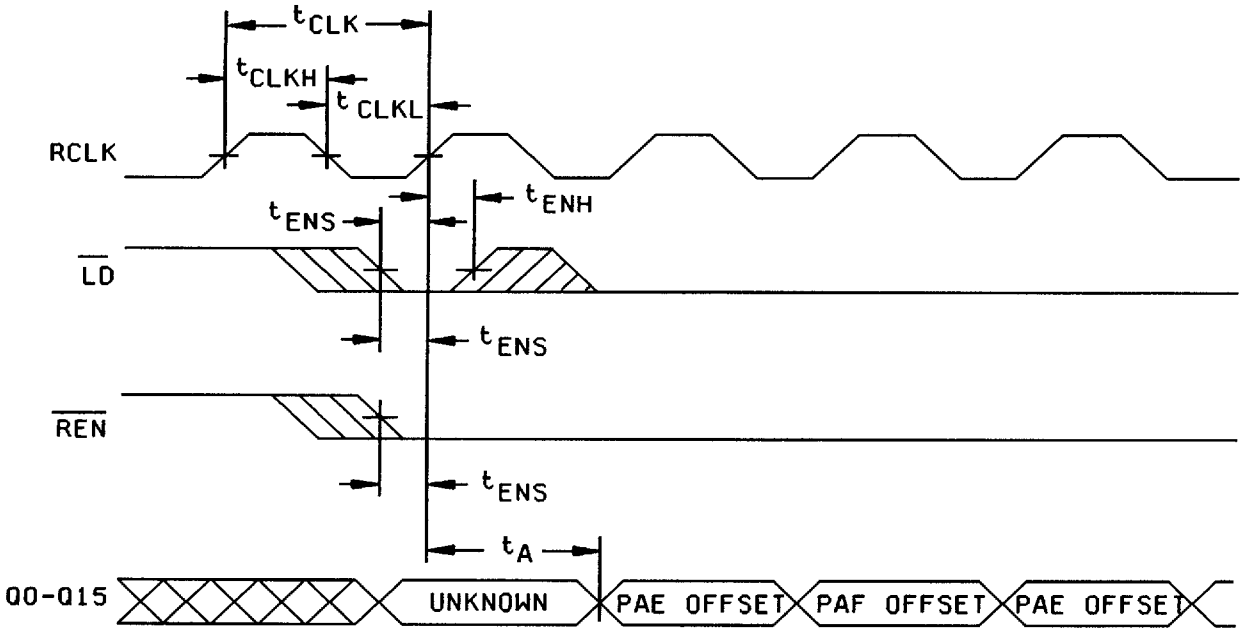


FIGURE 5. Timing waveforms - Continued.

PROGRAMMABLE ALMOST-EMPTY FLAG TIMING

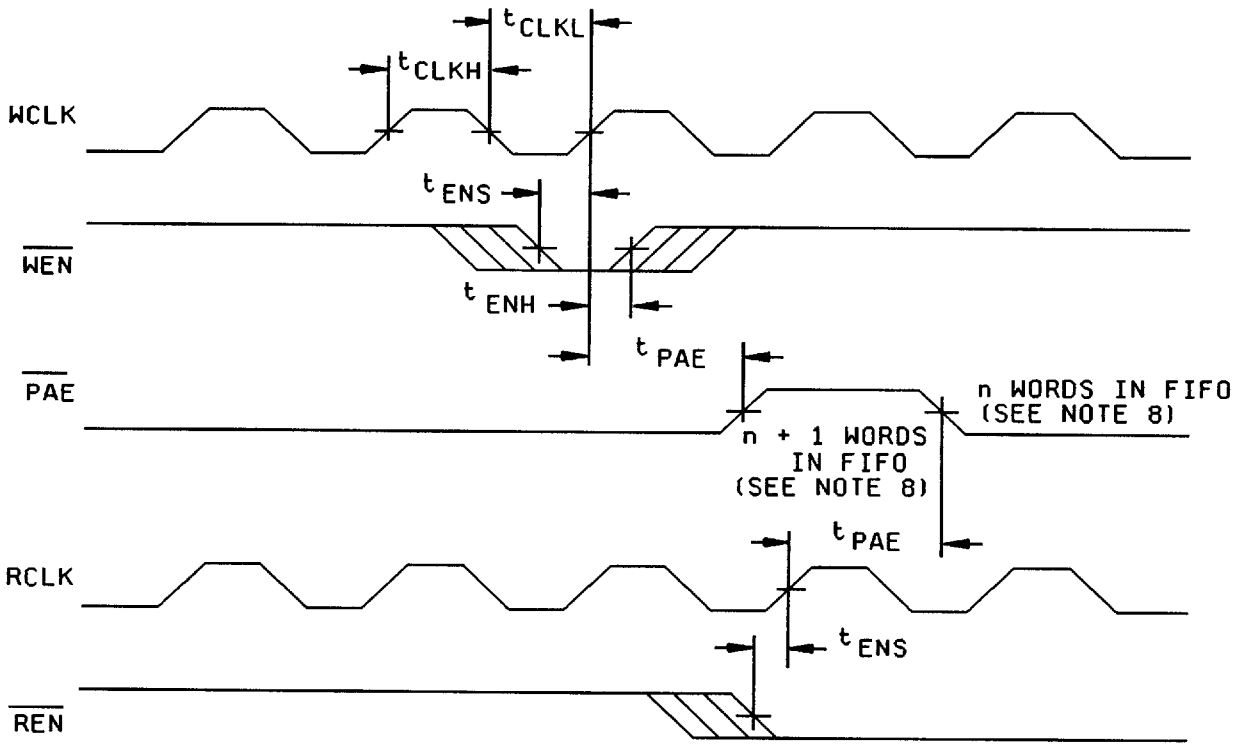


FIGURE 5. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92101
		REVISION LEVEL	SHEET 21

PROGRAMMABLE ALMOST-FULL FLAG TIMING

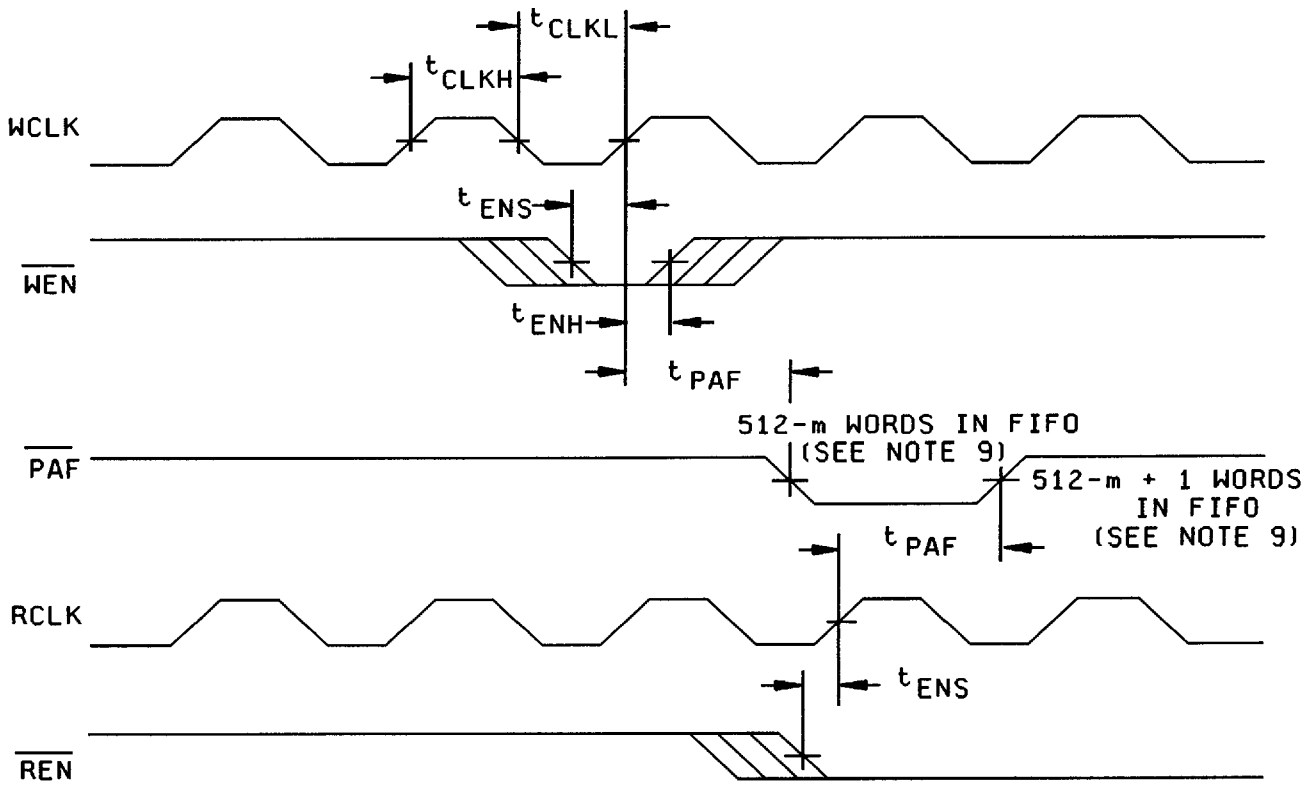


FIGURE 5. Timing waveforms - Continued.

HALF FULL FLAG TIMING

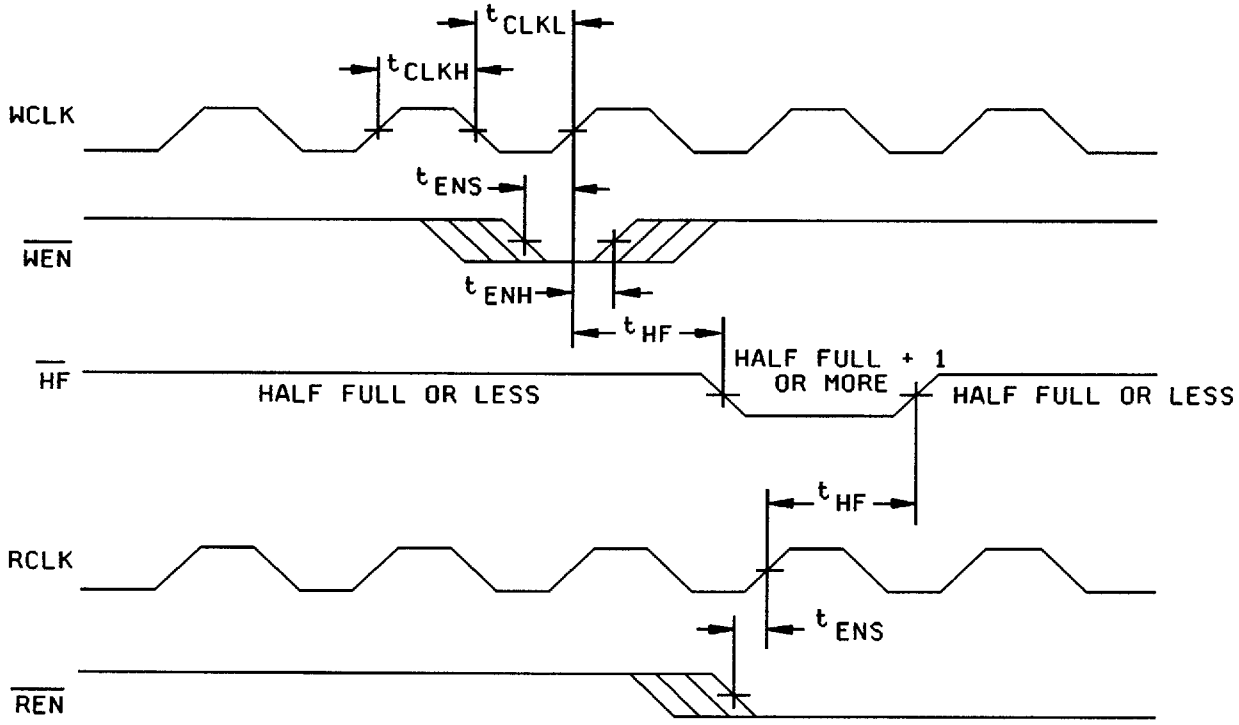
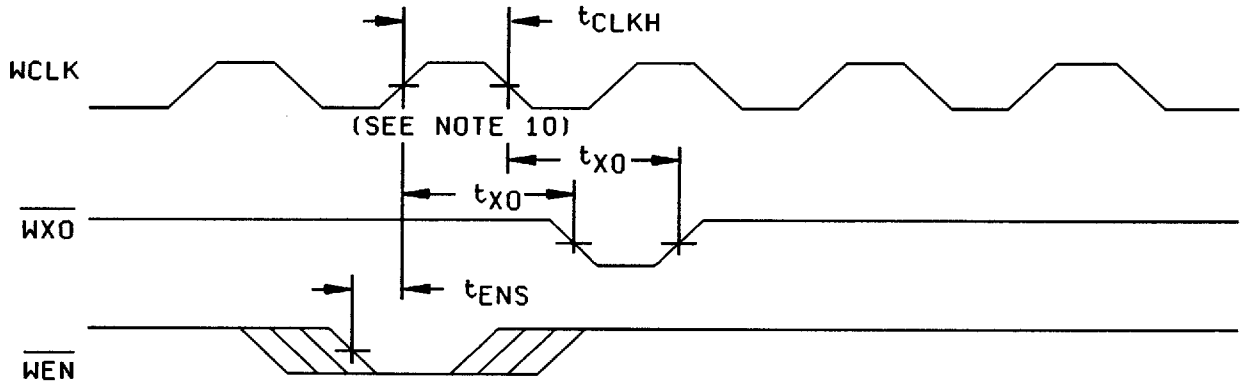


FIGURE 5. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92101
		REVISION LEVEL	SHEET 23

WRITE EXPANSION OUT TIMING



READ EXPANSION OUT TIMING

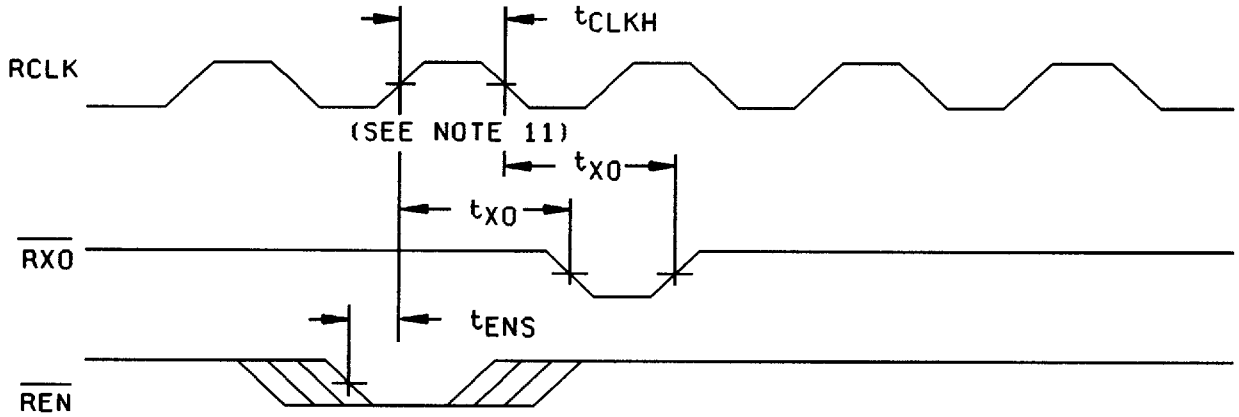
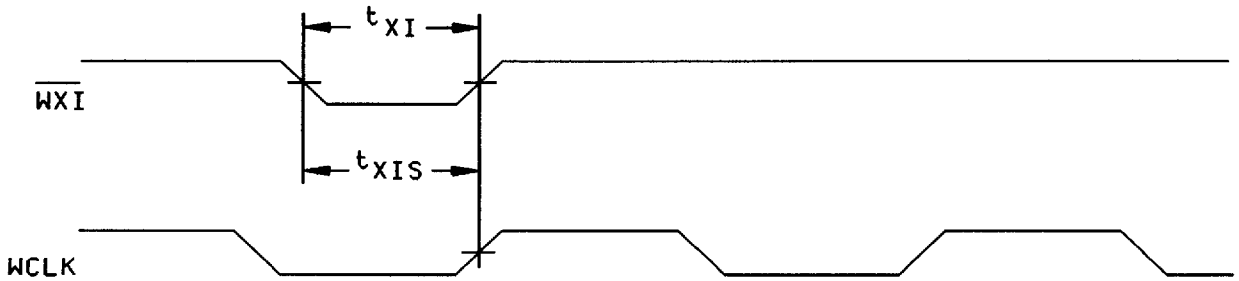


FIGURE 5. Timing waveforms - Continued.

WRITE EXPANSION IN TIMING



READ EXPANSION IN TIMING

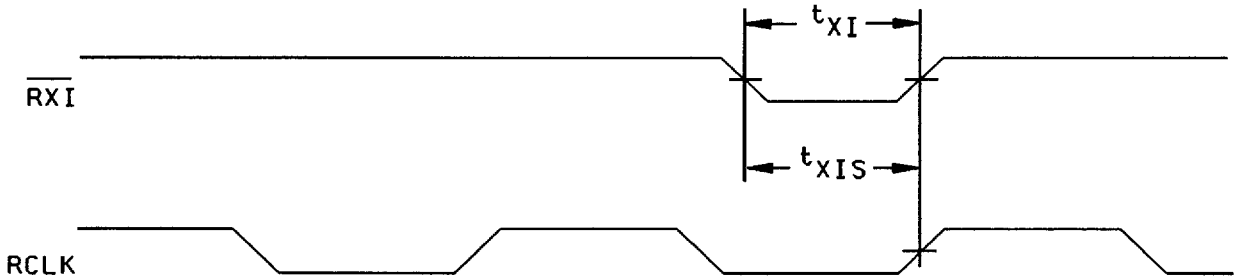


FIGURE 5. Timing waveforms. - Continued.

NOTES:

1. C_L = load capacitance and includes jig and probe capacitance.
2. The clocks (RCLK, WCLK) can be free-running during reset.
3. After reset, the outputs will be low if $\overline{OE}$ = low and three-state if $\overline{OE}$ = high.
4. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.
5. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.
6. When $t_{SKEW2} \geq$ the minimum limit specified in table I, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW2} <$ the minimum limit, t_{FRL} (maximum) = either $2t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The latency timing applies only at the empty boundary ($\overline{EF}$ = LOW).
7. The first word is always available one cycle after $\overline{EF}$ goes high.
8. PAE is offset = n. Number of data words written into FIFO already = n.
9. PAF offset = m. Number of data words written into FIFO already = 512 - m + 1.
10. Write to last physical location.
11. Read from last physical location.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC2} standby	±10% of specified value in table I
I_{LI}, I_{LO}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.1 Group A inspection - continued.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38535, MIL-STD-1331, and as follows:

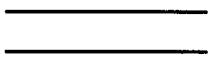
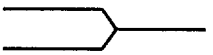
Symbol	Name	I/O	Description
D0-D17	Data Inputs	I	Data inputs for an 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is low, data is written into the FIFO on a low-to-high transition of WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is low, data is written into the FIFO on every low-to-high transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is low.
RCLK	Read Clock	I	When $\overline{REN}$ is low, data is read from the FIFO on a low-to-high transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is low, data is read from the FIFO on every low-to-high transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is low, the data output bus is active. If $\overline{OE}$ is high, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is low, data on the inputs D0-D11 is written to the offset and depth registers on the low-to-high transition of the WCLK, when $\overline{WEN}$ is low. When $\overline{LD}$ is low, data on the outputs Q0-Q11 is read from the offset and depth registers on the low-to-high transition of the RCLK, when $\overline{REN}$ is low.
$\overline{FL}$	First load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to high for all other devices in the daisy chain.

6.5 Abbreviations, symbols, and definitions - continued.

Symbol	Name	I/O	Description
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is low, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is high, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is low, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 63 from empty.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is low, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 63 from full.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is low, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is high, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO/HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q0-Q17	Data Outputs	O	Data outputs for an 18-bit bus.
V_{CC}	Power	-	Eight +5 volt power supply pins.
GND	Ground	-	Eight ground pins.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.