REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						
REV STATUS OF SHEETS			REV																
			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
95-02-07

REVISION LEVEL

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS ELECTRICALLY ERASABLE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

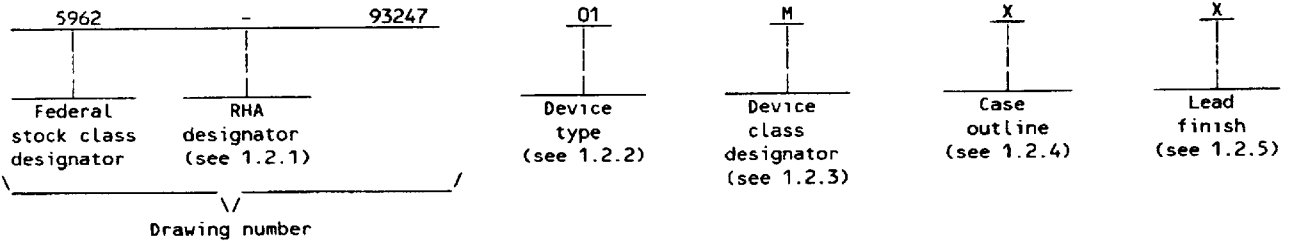| SIZE A	CAGE CODE 67268	5962-93247
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1. SCOPE

1.1 <u>Scope</u>. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 <u>PIN</u>. The PIN shall be as shown in the following example:

```
   5962          -      93247          01           M            X            X
     |           |        |             |           |            |            |
     |           |        |             |           |            |            |
 Federal       RHA                   Device      Device        Case         Lead
stock class  designator             type        class        outline      finish
designator   (see 1.2.1)          (see 1.2.2)  designator   (see 1.2.4)  (see 1.2.5)
                                                (see 1.2.3)
  _____/ _____/
                   \/
            Drawing number
```

1.2.1 <u>RHA designator</u>. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7256E	256 macrocell EEPLD	20 ns
02	7256E	256 macrocell EEPLD	15 ns

1.2.3 <u>Device class designator</u>. The device class designator shall be a single letter identifying the product assurance level (see 6.6 herein) as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals		Package style
X	CMGA7-P192	192	1/	pin grid array
Y	see figure 1	208	2/	quad-flat package

1.2.5 <u>Lead finish</u>. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/   192 = actual number of pins used, not maximum listed in MIL-STD-1835.
2/   208 = actual number of pins used, not maximum listed in MIL-STD-1835.

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1.3 <u>Absolute maximum ratings.</u> <u>3/</u>

Supply voltage range with respect to ground (V_{CC})	-2.0 V dc to +7.0 V dc <u>4/</u>
Programming supply voltage range with respect to ground (V_{PP}) . . .	-2.0 V dc to +13.0 V dc <u>4/</u>
DC input voltage range with respect to ground (V_{IN})	-2.0 V dc to +7.0 V dc <u>4/</u>
DC V_{CC} or GND current (I_{MAX})	800 mA
DC output current, per pin I_{OUT}	±25 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Case Y	12°C/W <u>5/</u>
Maximum power dissipation (P_D) <u>5/</u>	4.0 W
Temperature range under bias	-65°C to +135°C
Junction temperature under bias (T_J)	+175°C
Endurance	100 erase/write cycles (minimum)
Data retention	10 years (minimum)

1.4 <u>Recommended operating conditions.</u>

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	0 V dc to V_{CC}
Output voltage range (V_{OUT})	0 V dc to V_{CC}
Input rise time (t_r)	40 ns maximum
Input fall time (t_f)	40 ns maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 <u>Digital logic testing for device classes Q and V.</u>

Fault coverage measurement of manufacturing
   logic tests (MIL-STD-883, test method 5012) . . . . XX percent <u>6/</u>

2. APPLICABLE DOCUMENTS

2.1   <u>Government specification, standards, bulletin, and handbook</u>. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

   SPECIFICATION

      MILITARY

         MIL-I-38535   -   Integrated Circuits, Manufacturing, General Specification for.

   STANDARD

      MILITARY

         MIL-STD-883   -   Test Methods and Procedures for Microelectronics.
         MIL-STD-973   -   Configuration Management.
         MIL-STD-1835 -   Microcircuit Case Outlines.

   BULLETIN

      MILITARY

         MIL-BUL-103- List of Standard Microcircuit Drawings (SMD's).

<u>3/</u>   Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
<u>4/</u>   When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
<u>5/</u>   Minimum DC input is -0.3 V. During transistions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
<u>6/</u>   Must withstand the added P_D due to short circuit test, e.g., I_{SC}.
<u>7/</u>   Values will be added when they become available.

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HANDBOOK

MILITARY

MIL-HDBK-780- Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88   -   Standard Guide for the Measurement of Single Event Phenomena from
Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17   -   A Standardized Test Procedure for the Characterization of
Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified in figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in screening (see 4.2 herein) or quality conformance inspection, groups A, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic cells shall be programmed or at least 25 percent of the total logic cells shall be programmed for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Processing of EEPLDs All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Conditions of the supplied devices. Devices will be supplied in erased state. No provision will be made for supplying written devices.

3.12.2 Writing of EEPLDS. When specified, devices shall be written in accordance with the procedures and characteristics specified in 4.6.

3 12.3 Clearing of EEPLDs. When specified, devices shall be cleared in accordance with the procedures and characteristics specified in 4 7.

3.12.4 Verification of state of EEPLDs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request. Endurance capability shall be guaranteed at 25°C only.

3.14 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

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4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 <u>Screening</u>. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 <u>Additional criteria for device class M</u>.

   a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

   b. Prior to burn-in, the devices shall be programmed (see 4.6 herein) with a checkboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.

   c. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

     (1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D); for circuit see 4.2.1c herein.

   d. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 <u>Additional criteria for device classes Q and V</u>.

   a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

   b. Interim and final electrical test parameters shall be as specified in table IIA herein.

   c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

   d. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 <u>Conformance inspection</u>. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

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TABLE 1. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OH} = -4.0 mA, V_{IL} = -0.8 V	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V I_{OL} = 8.0 mA, V_{IL} = 0.8 V	1,2,3	All		0.45	V
Input high voltage	V_{IH}		1,2,3	All	2.0	V_{CC} +0.3	V
Input low voltage	V_{IL}		1,2,3	All	-0.3	0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V V_{IN} = 5.5 V and GND	1,2,3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V V_{OUT} = 5.5 V and GND	1,2,3	All	-40	40	µA
Output short circuit current 1/ 2/	I_{SC}	V_{OUT} = 0.5 V, V_{CC} = 5.5 V	1,2,3	All	-100	-225	mA
Power supply current (active, low power mode) 3/ 4/	I_{CC1}	V_{IN} = V_{CC} to GND, V_{CC} = 5.5 V, I_{OUT} = 0 mA f = 1 MHZ	1,2,3	All		400	mA
Power supply current (standby, low power mode) 3/ 4/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = GND	1,2,3	All		300	mA
Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0.0 V, T_A = +25°C, f = 1 MHz	4	All			
OE1n		See 4.4.1f				20	pF
All other inputs						15	
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0.0 V T_A = +25°C, f = 1 MHz See 4.4.1f	4	All		15	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Functional tests		See 4.4.1c	7,8A,8B	All			

EXTERNAL TIMING

Test	Symbol	Conditions	Group A subgroups	Device type	Min	Max	Unit
Input to nonregistered output	t_{PD1}	See figures 4 circuit A and 5 5/	9,10,11	01		20	ns
				02		15	
I/O input to non-registered output	t_{PD2}		9,10,11	01		20	ns
				02		15	
Global clock setup time 2/	t_{FSU}		9,10,11	01	5		ns
				02	3		
Global clock setup time for fast input 2/	t_{FH}		9,10,11	01	2		ns
				02	1		
Global clock setup time	t_{SU}		9,10,11	01	12		ns
				02	11		
Global clock hold time	t_H		9,10,11	All	0		ns
Global clock to output delay	t_{CO1}		9,10,11	01		12	ns
				02		9.0	
Global clock high time 2/ 4/	t_{CH}		9,10,11	01	6.0		ns
				02	5.0		
Array clock to output delay	t_{ACO1}		9,10,11	01		20	ns
				02		15	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V −55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Array clock high time 2/ 4/	t_{ACH}	See figures 4 circuit A and 5 5/	9,10,11	01	8.0		ns
				02	6.0		
Global clock low time 2/ 4/	t_{CL}		9,10,11	01	6.0		ns
				02	5.0		
Array clock setup time	t_{ASU}		9,10,11	01	6.0		ns
				02	5.0		
Array clock hold time	t_{AH}		9,10,11	01	6.0		ns
				02	5.0		
Array clock low time 2/ 4/	t_{ACL}		9,10,11	01	8.0		ns
				02	6.0		
Minimum global clock period 2/ 3/ 4/	t_{CNT}		9,10,11	01		16	ns
				02		13	
Maximum internal global clock frequency 2/ 3/ 4/	f_{CNT}		9,10,11	01	62.5		MHz
				02	76.9		
Minimum array clock period 2/ 3/ 4/	t_{ACNT}		9,10,11	01		16	ns
				02		13	
Maximum internal array clock frequency 2/ 3/ 4/	f_{ACNT}		9,10,11	01	62.5		MHz
				02	76.9		
Maximum clock frequency 2/ 4/ 6/	f_{MAX}		9,10,11	01	83.3		MHz
				02	100		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
INTERNAL TIMING							
Input pad and buffer delay	t_{IN}	See figures 4 circuit A and 5 5/ 7/	9,10,11	All		3.0	ns
I/O input pad and buffer delay	t_{IO}		9,10,11	All		3.0	ns
Shared expander delay	t_{SEXP}		9,10,11	01		9.0	ns
				02		8.0	
Parallel expander delay	t_{PEXP}		9,10,11	All		2.0	ns
Logic array delay	t_{LAD}		9,10,11	01		8.0	ns
				02		5.0	
Logic control array delay	t_{LAC}		9,10,11	01		8.0	ns
				02		5.0	
Output buffer and pad delay	t_{OD}		9,10,11	01		5.0	ns
				02		4.0	
Output buffer enable delay	t_{ZX}		9,10,11	01		10	ns
				02		7	
Output buffer disable delay	t_{XZ}	See figures 4 circuit B and 5 5/ 7/	9,10,11	01		10	ns
				02		7	
Register setup time	t_{SU}	See figures 4 circuit A and 5 5/ 7/	9,10,11	01	4.0		ns
				02	5.0		
Global control delay	t_{GLOB}		9,10,11	01		3.0	ns
				02		1.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Register hold time	t_H	See figures 4 circuit A and 5 5/ 7/	9,10,11	All	5.0		ns
Register delay	t_{RD}		9,10,11	All		1.0	ns
Combinatorial delay	t_{COMB}		9,10,11	All		1.0	ns
Array clock delay	t_{IC}		9,10,11	01		8.0	ns
				02		5.0	
Register enable time	t_{EN}		9,10,11	01		8.0	ns
				02		5.0	
Register preset time	t_{PRE}		9,10,11	All		4.0	ns
Register clear time	t_{CLR}		9,10,11	All		4.0	ns
Program interconnect array delay	t_{PIA}		9,10,11	01		3.0	ns
				02		2.0	
Low power adder 8/	t_{LPA}		9,10,11	01		15	ns
				02		13	
Slew rate adder 9/	t_{SRA}		9,10,11	All		4	ns

1/ Not more than one output at a time should be shorted. Short circuit test duration should not exceed 1.0 second.
2/ Tested initially and after any design or process changes that affect the parameter, and therefore shall be guranteed to the limits specified in table I.
3/ Specified with a device programmed as a 16-bit loadable, enabled, up/down counter in each LAB.
4/ Values are guaranteed by design and may not be tested directly.
5/ AC tests are specified with input rise and fall times (10 percent to 90 percent) at 3.0 ns, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, and the output load of figure 3, circuit A.
6/ f_{MAX} represents the highest frequency for pipelined data.
7/ Internal timing parameters are not directly measurable and therefore are guaranteed by testing external timing parameters.
8/ The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low power mode.
9/ The t_{SRA} parameter must be added to the t_{OD} and t_{ZX} parameters for outputs set to slow slew rate.

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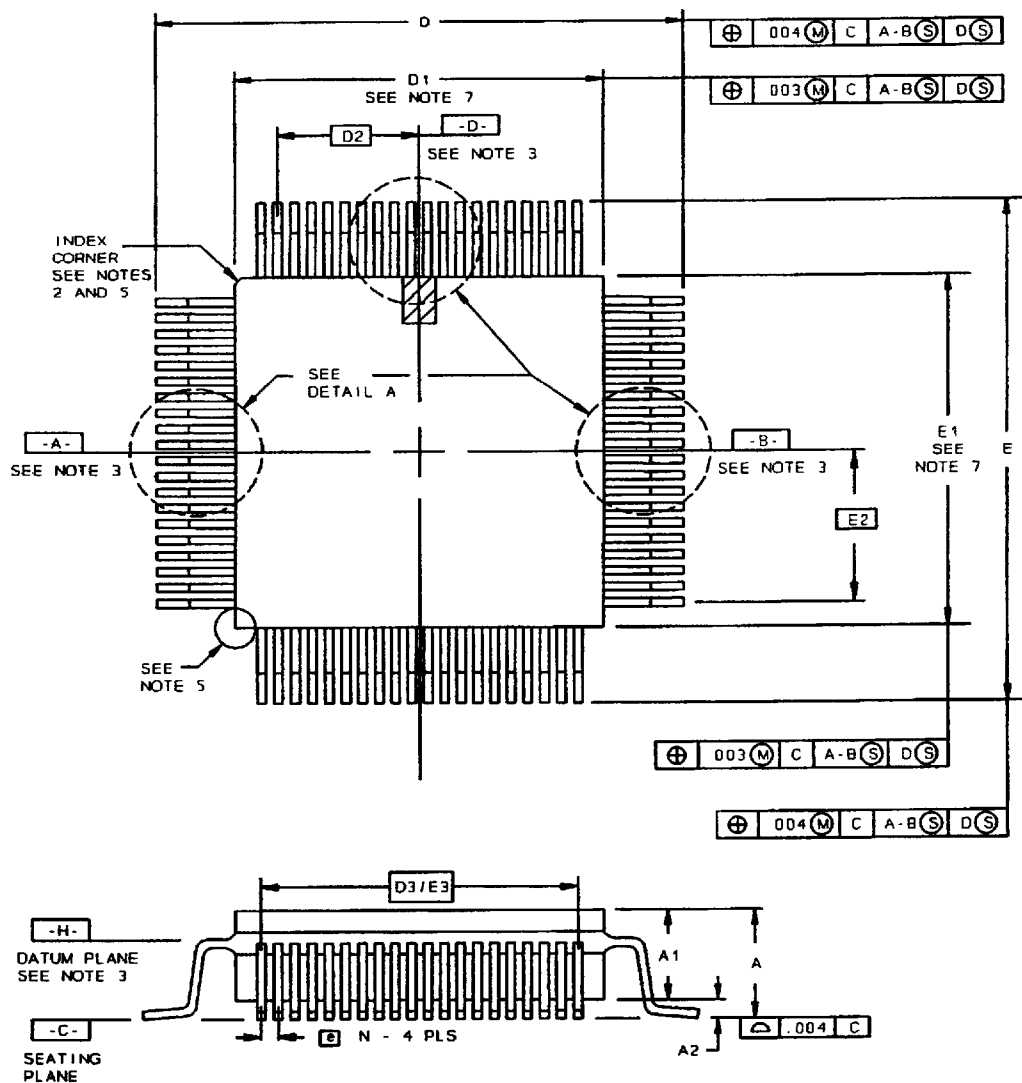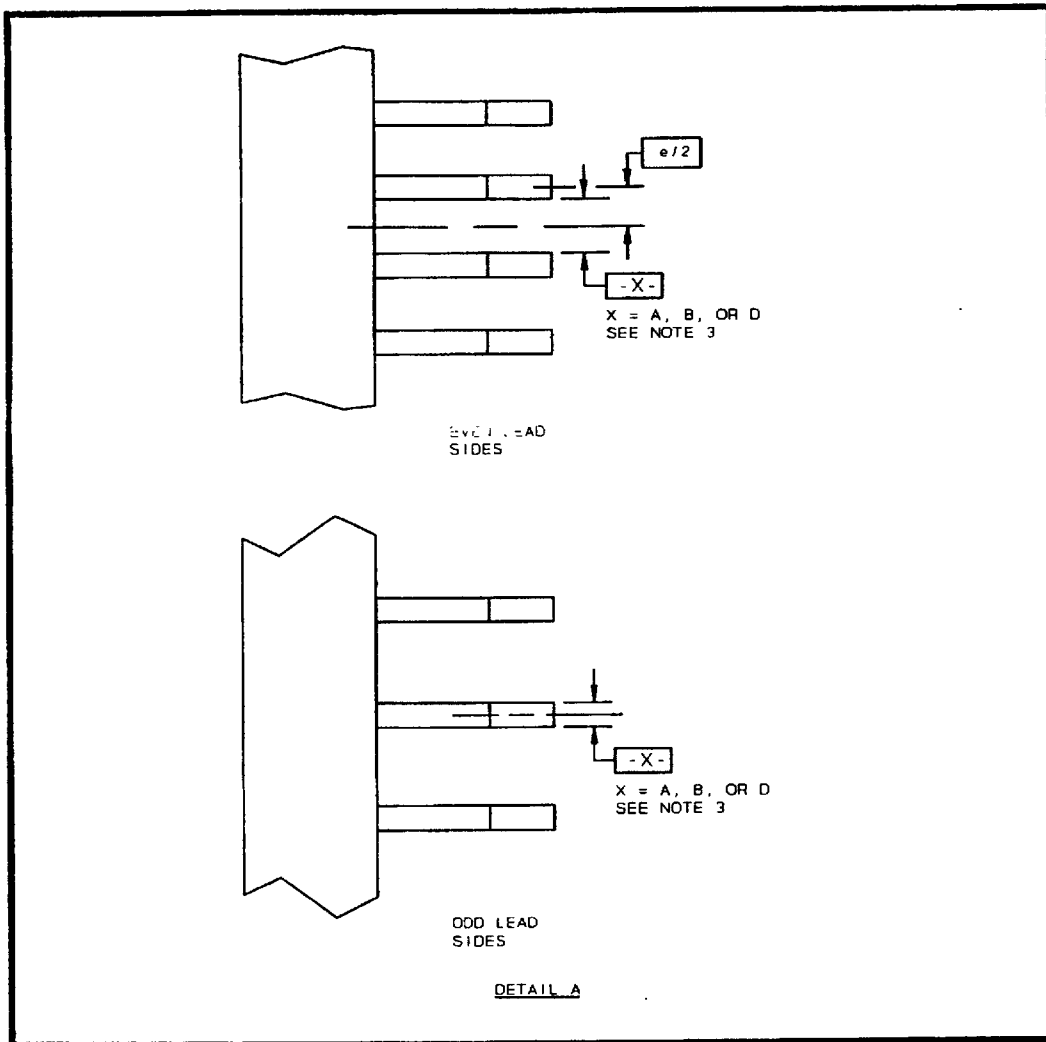
FIGURE 1. Case outline Y.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93247
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EVEN LEAD
SIDES

X = A, B, OR D
SEE NOTE 3

ODD LEAD
SIDES

DETAIL A

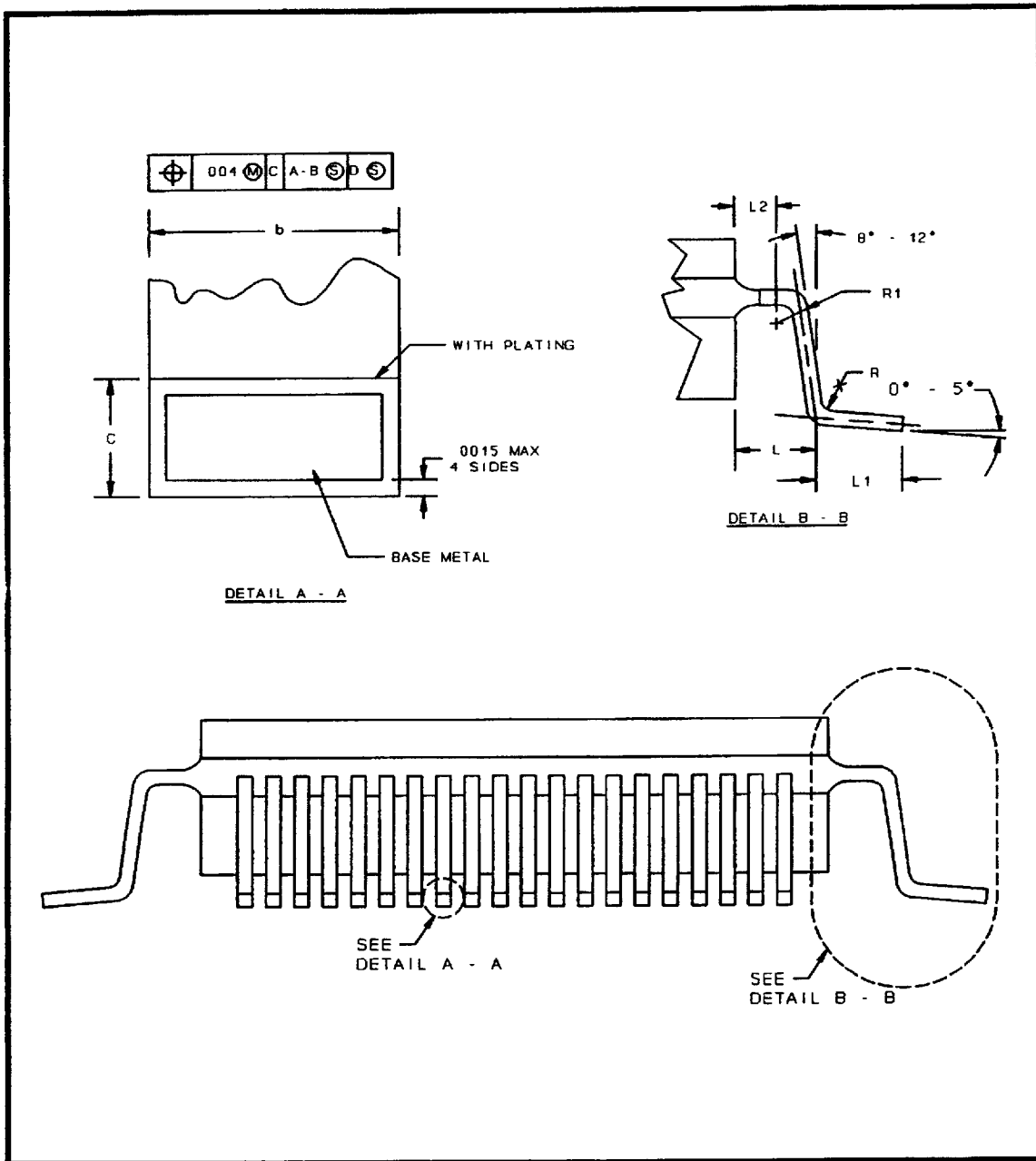FIGURE 1. Case outline Y - continued.

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FIGURE 1. Case outline Y – continued.

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Symbol	208 pin CQFP		Notes
	Min	Max	
A	2.16	4.83	1,2
A1	1.91	3.81	
A2	0.20	1.02	
b	0.20	0.56	
c	0.19	0.28	
D/E	30.4	30.8	
D1/E1	26.9	27.5	2,3
D2/E2	12.75 BSC		
D3/E3	25.5 BSC		
e	0.50 BSC		
L	1.20 REF		
L1	0.30	---	
L2	0.82 REF		
R	0.20	---	
R1	N/A		
ND/NE	52		4
N	208		4,5

1. Controlling dimensions are in milimeters.

2. Dimension "A" controls the overall package height. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).

3. Chip carriers shall be constructed of a minimum of two ceramic layers.

4. This dimension allows for package edge anomalies caused by material protrusion, such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.

5. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of lengths "D" and "E" respectively.

6. A terminal 1 identification mark shall be located on the first side clockwise from the index corner, within the shaded area shown. Terminal numbers shall increase in a counterclockwise direction when viewed as shown. If the identification mark is not exactly adjacent to terminal 1, terminal 1 is located as follows:

    a. If the number of terminals on a side is odd, terminal 1 is the center terminal.
    b. If the number of terminals on a side is even, terminal 1 is the terminal which is adjacent to the centerline of the terminal array in the direction closest to the index corner.

7. When the number of terminals per side is even, datums A, B, and D are located at the terminal array centers. When the number of terminals per side is odd, datums A, B, and D are located at the centers of the center terminals. The measurement point for establishing these datums is the package/lead interface at datum plane H.

8. Corner shape (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.

9. The leads on this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc.) are not shown on the drawing; however, when microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead protection shall be in place.

10. The quad leaded chip carrier drawings in this figure show a "gullwing" lead configuration. An optional lead configuration can be specified for unformed (straight) leads, see figure 1 and table V concerning how to designate an option. When either option is selected and straight leads are subsequently formed by the microcircuit device user, the resultant lead configuration shall conform to the "gullwing" lead dimensions and coplanarity requirements specified in this figure.

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Case outline X

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	PI/O		C1	OI/O		E16	CI/O
A2	PI/O		C2	OI/O		E17	CI/O
A3	PI/O		C3	OI/O		F1	KI/O
A4	PI/O		C4	PI/O		F2	OI/O
A5	LI/O		C5	VCC		F3	KI/O
A6	LI/O		C6	LI/O		F15	GI/O
A7	LI/O		C7	GND		F16	CI/O
A8	LI/O		C8	LI/O		F17	GI/O
A9	LI/O		C9	HI/O		G1	KI/O
A10	HI/O		C10	HI/O		G2	KI/O
A11	HI/O		C11	VCC		G3	KI/O
A12	HI/O		C12	HI/O		G4	VCC
A13	HI/O		C13	GND		G14	GND
A14	DI/O		C14	DI/O		G15	GI/O
A15	DI/O		C15	CI/O		G16	GI/O
A16	DI/O		C16	CI/O		G17	GI/O
A17	DI/O		C17	CI/O		H1	KI/O
B1	OI/O		D1	OI/O		H2	KI/O
B2	PI/O		D2	OI/O		H3	KI/O
B3	PI/O		D3	OI/O		H4	GND
B4	PI/O		D4	GNDO		H14	VCC
B5	PI/O		D7	VCC		H15	GI/O
B6	PI/O		D8	GND		H16	GI/O
B7	LI/O		D9	HI/O		H17	GI/O
B8	LI/O		D10	GND		J1	KI/O
B9	LI/O		D11	VCC		J2	JI/O
B10	HI/O		D14	VCC		J3	JI/O
B11	HI/O		D15	CI/O		J4	JI/O
B12	DI/O		D16	CI/O		J14	FI/O
B13	DI/O		D17	CI/O		J15	FI/O
B14	DI/O		E1	OI/O		J16	FI/O
B15	DI/O		E2	KI/O		J17	GI/O
B16	DI/O		E3	OI/O			
B17	DI/O		E15	CI/O			

NC = NO CONNECT

FIGURE 2. Terminal connections.

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Case outline X

Device type	All		Device type	All			Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol			Terminal number	Terminal symbol
K1	JI/O		R1	NI/O			U8	II/O
K2	JI/O		R2	MI/O			U9	II/O
K3	JI/O		R3	MI/O			U10	EI/O
K4	VCC		R4	GND			U11	EI/O
K14	GND		R5	VCC			U12	EI/O
K15	FI/O		R6	II/O			U13	AI/O
K16	FI/O		R7	II/O			U14	AI/O
K17	FI/O		R8	II/O			U15	AI/O
L1	JI/O		R9	GCLRK			U16	AI/O
L2	JI/O		R10	EI/O			U17	AI/O
L3	JI/O		R11	GND				
L4	GND		R12	EI/O				
L14	VCC		R13	EI/O				
L15	FI/O		R14	VCC				
L16	FI/O		R15	AI/O				
L17	FI/O		R16	AI/O				
M1	JI/O		R17	BI/O				
M2	NI/O		T1	NI/O				
M3	NI/O		T2	NI/O				
M15	BI/O		T3	MI/O				
M16	BI/O		T4	MI/O				
M17	FI/O		T5	MI/O				
N1	NI/O		T6	II/O				
N2	NI/O		T7	II/O				
N3	NI/O		T8	II/O				
N15	BI/O		T9	II/O				
N16	BI/O		T10	EI/O				
N17	BI/O		T11	EI/O				
P1	NI/O		T12	EI/O				
P2	NI/O		T13	EI/O				
P3	VCC		T14	AI/O				
P4	MI/O		T15	AI/O				
P7	VCC		T16	BI/O				
P8	GND		T17	BI/O				
P9	GCCKI		U1	MI/O				
P10	GND		U2	MI/O				
P11	VCC		U3	MI/O				
P14	AI/O		U4	MI/O				
P15	GND		U5	MI/O				
P16	BI/O		U6	II/O				
P17	BI/O		U7	II/O				

NC = NO CONNECT

FIGURE 2. Terminal connections – Continued.

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Case outline Y

Device type	ALL		Device type	ALL			Device type	ALL			Device type	ALL
Terminal number	Terminal symbol		Terminal number	Terminal symbol			Terminal number	Terminal symbol			Terminal number	Terminal symbol
1	NC		53	NC			105	NC			157	NC
2	NC		54	NC			106	NC			158	NC
3	MI/O		55	PI/O			107	VCCio			159	AI/O
4	MI/O		56	PI/O			108	CI/O			160	AI/O
5	VCCio		57	PI/O			109	CI/O			161	AI/O
6	NI/O		58	PI/O			110	CI/O			162	AI/O
7	NI/O		59	PI/O			111	CI/O			163	AI/O
8	NI/O		60	PI/O			112	CI/O			164	AI/O
9	NI/O		61	PI/O			113	CI/O			165	VCCio
10	NI/O		62	PI/O			114	CI/O			166	AI/O
11	NI/O		63	VCCio			115	CI/O			167	AI/O
12	NI/O		64	PI/O			116	GND			168	EI/O
13	NI/O		65	PI/O			117	CI/O			169	EI/O
14	GND		66	LI/O			118	CI/O			170	EI/O
15	NI/O		67	LI/O			119	GI/O			171	EI/O
16	NI/O		68	LI/O			120	GI/O			172	EI/O
17	JI/O		69	LI/O			121	GI/O			173	EI/O
18	JI/O		70	LI/O			122	GI/O			174	GND
19	JI/O		71	LI/O			123	GI/O			175	EI/O
20	JI/O		72	GND			124	GI/O			176	EI/O
21	JI/O		73	LI/O			125	VCCio			177	EI/O
22	JI/O		74	VCCint			126	GI/O			178	EI/O
23	VCCio		75	GND			127	GI/O			179	VCCint
24	JI/O		76	LI/O			128	GI/O			180	GND
25	JI/O		77	LI/O			129	GI/O			181	OE2/GCLK2
26	JI/O		78	LI/O			130	FI/O			182	GCLRn
27	JI/O		79	HI/O			131	FI/O			183	OE1
28	KI/O		80	HI/O			132	FI/O			184	GCLK1
29	KI/O		81	HI/O			133	FI/O			185	GND
30	KI/O		82	GND			134	GND			186	VCCint
31	KI/O		83	VCCint			135	FI/O			187	II/O
32	GND		84	HI/O			136	FI/O			188	II/O
33	KI/O		85	VCCio			137	FI/O			189	II/O
34	KI/O		86	HI/O			138	FI/O			190	II/O
35	KI/O		87	HI/O			139	FI/O			191	VCCio
36	KI/O		88	HI/O			140	FI/O			192	II/O
37	KI/O		89	HI/O			141	BI/O			193	II/O
38	KI/O		90	HI/O			142	BI/O			194	II/O
39	OI/O		91	HI/O			143	VCCio			195	II/O
40	OI/O		92	DI/O			144	BI/O			196	II/O
41	VCCio		93	DI/O			145	BI/O			197	II/O
42	OI/O		94	GND			146	BI/O			198	MI/O
43	OI/O		95	DI/O			147	BI/O			199	MI/O
44	OI/O		96	DI/O			148	BI/O			200	GND
45	OI/O		97	DI/O			149	BI/O			201	MI/O
46	OI/O		98	DI/O			150	BI/O			202	MI/O
47	OI/O		99	DI/O			151	BI/O			203	MI/O
48	OI/O		100	DI/O			152	GND			204	MI/O
49	OI/O		101	DI/O			153	AI/O			205	MI/O
50	GND		102	DI/O			154	AI/O			206	MI/O
51	NC		103	NC			155	NC			207	NC
52	NC		104	NC			156	NC			208	NC

NC = NO CONNEOT

FIGURE 2. Terminal connections - Continued.

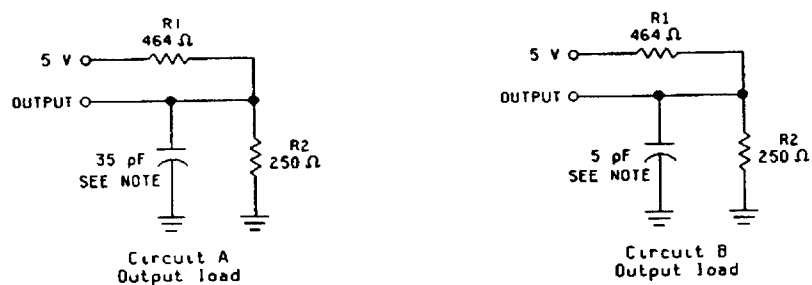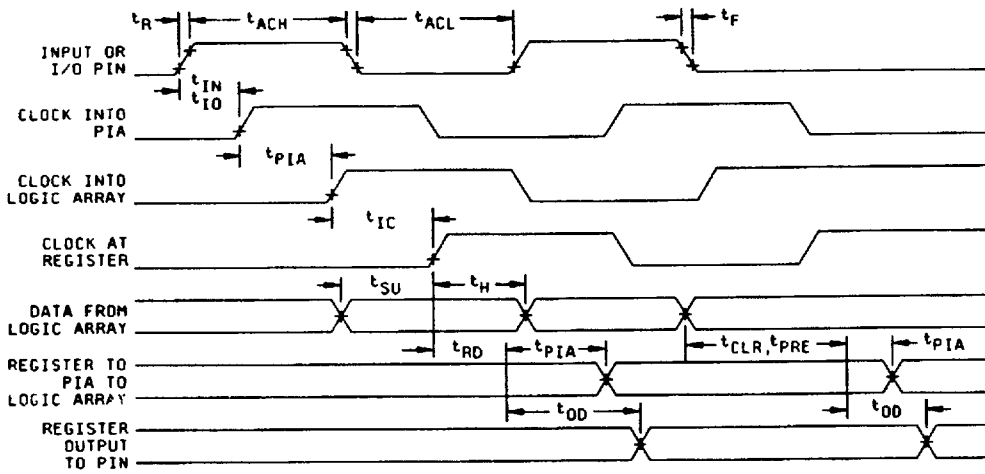| STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93247
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Truth table				
Input pins				Output pins
CLRn/I	OE2n/I	CLK/I	I	I/O
X	X	X	X	Z

NOTES:
1. X = Don't care.
2. Z = High impedance.

FIGURE 3. Truth table (unprogrammed).

R1
464 Ω

5 V
OUTPUT
35 pF
SEE NOTE
R2
250 Ω

Circuit A
Output load

R1
464 Ω

5 V
OUTPUT
5 pF
SEE NOTE
R2
250 Ω

Circuit B
Output load

NOTE: Including scope and jig (minimum values).

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Input pulses

3.0 V
90%
90%
GND
10%
10%
t_r
t_f
≤ 3 ns
≤ 3 ns
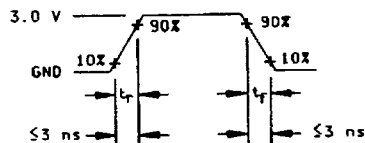
FIGURE 4. Output load circuits and test conditions.

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INPUT PIN t_{IN}

I/O PIN t_{IO}

PIA PIN t_{PIA}

SHARED EXPANDER DELAY t_{SEXP}

LOGIC ARRAY INPUT t_{LAC}, t_{LAD}

PARALLEL EXPANDER DELAY t_{PEXP}
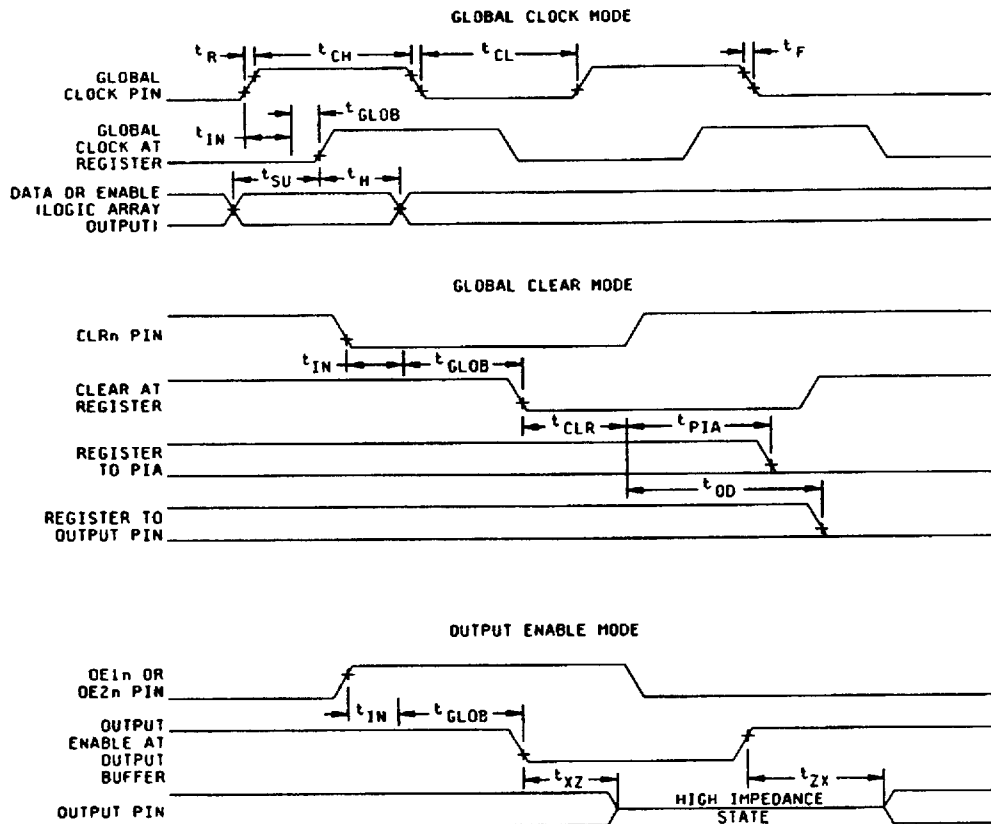
LOGIC ARRAY OUTPUT t_{COMB}

t_{OD}

OUTPUT PIN
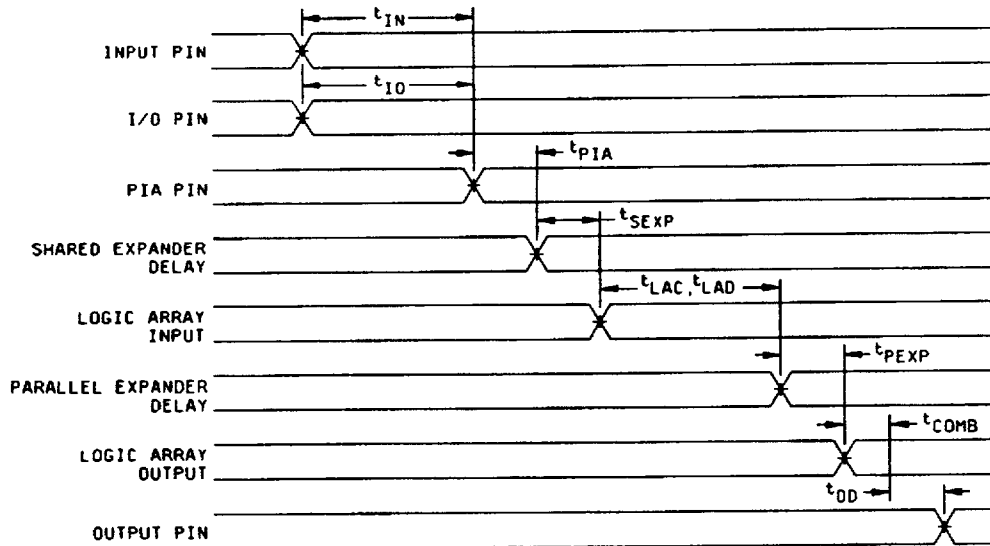
FIGURE 5. Switching waveforms.

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FIGURE 5. Switching waveforms - Continued.

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FIGURE 5. Switching waveforms - Continued.

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4.4.1 <u>Group A inspection</u>.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of Table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For
device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device;
these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5
herein).

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After
completion of all testing, the devices shall be erased and verified, (except devices submitted for groups B,
C, and D testing).

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process
changes which may affect the performance of the device. For device class M procedures and circuits shall be
maintained under document revision level control by the manufacturer and shall be made available to the
preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and
circuits shall be under the control of the device manufacturer's (TRB) in accordance with MIL-I-38535 and
shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on
all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information
contained in JEDEC standard number 17 may be used for reference.

f. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any
process or design changes which may affect input or output capacitance. Capacitance shall be measured
between the designated terminal and GND at a frequency of 1MHz. Sample size is five devices with no
failures, and all input and output terminal tested.

4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table
IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in
table IIB herein.

4.4.2.1 <u>Additional criteria for device class M</u>. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. The devices selected for testing shall be programmed (see 3.2.3.1 herein). After completion of all testing
the devices shall be erased and verified (except devices submitted to group D).

b. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document
revision level control and shall be made available to the preparing or acquiring activity upon request. The
test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance
with the intent specified in test method 1005.

b. $T_A = +125°C$, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition, and
test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance
with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device
manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity
upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in
accordance with the intent specified in test method 1005.

4.4.3 <u>Group D inspection</u>. For group D inspection end-point electrical parameters shall be as specified in table
IIA herein. The devices selected for testing shall be programmed (see 3.2.3.2 herein). After completion of all
testing, the devices shall be erased and verified.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1f.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1e.

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TABLE IIB. **Delta limits at +25°C.**

Parameter 1/	Device types
	All
I_{CC2}	±1% of specified limit in table I.
I_{IX}	±1% of specified limit in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES
(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory).

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

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6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535, MIL-STD-1331, and as follows:

C_{IN} C_{OUT} . . . . Input and bidirectional output, terminal-to-GND capacitance
GND . . . . Ground zero voltage potential
I_{CC} . . . . Supply current
I_{IL} . . . . Input current low
I_{IH} . . . . Input current high
T_C . . . . Case temperature
T_A . . . . Ambient temperature
V_{CC} . . . . Positive supply voltage
o/v . . . . Latch-up over-voltage

6.5.1 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	OML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

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6.7 Sources of supply.

   6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

   6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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