T-51-10-08

National Semiconductor

ADC08061/ADC08062/ADC08064/ADC08068 500 ns A/D Converter with S/H Function and Input Multiplexer

General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08061, ADC08062, ADC08064, and ADC08068 CMOS A/D converters offer 500 ns conversion time, internal sample-and-hold (S/H), and dissipate only 100 mW of power. The ADC08062, ADC08064, and ADC08068 include, respectively, a 2-, 4-, and 8-channel multiplexer. The ADC08061/2/4/8 family performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LSBs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08061/2/4/8 family can perform accurate conversions of full-scale input signals at frequencies from dc to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, these parts have been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

■ Resolution	8 bits
■ Conversion Time	560 ns max ($\overline{\text{WR}}$-$\overline{\text{RD}}$ Mode)
■ **Full Power Bandwidth**	**300 kHz**
■ Throughput rate	1.5 MHz
■ Power Dissipation	100 mW max
■ Total Unadjusted Error	±½ LSB and ±1 LSB

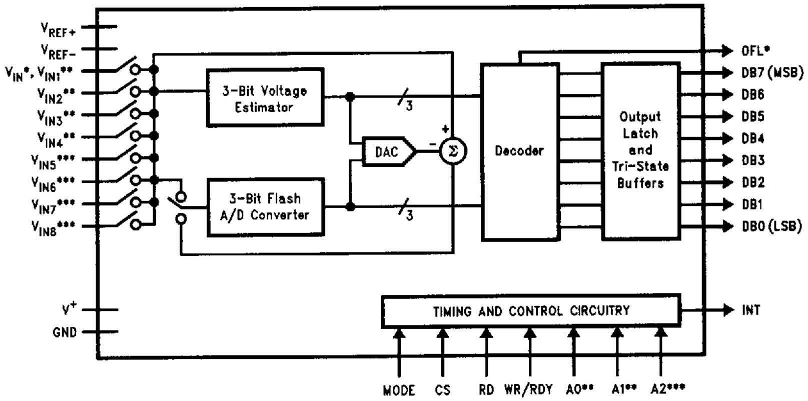
Features

- 1, 2, 4, or 8 input channels
- No external clock required
- Analog input voltage range from GND to V^+
- Overflow output available for cascading (ADC08061)
- ADC08061 pin-compatible with the industry standard ADC0820
- ADC08064 and ADC08068 are pin compatible with AD7824 and AD7828, respectively

Applications

- Mobile telecommunications
- Hard disk drives
- Instrumentation
- High-speed data acquisition systems

Block Diagram



TL/H/11086-1

*ADC08061

**ADC08062, ADC08064, and ADC08068

***ADC08064 and ADC08068

****ADC08068

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+)	6V
Logic Control Inputs	$-0.3V$ to $V^+ + 0.3V$
Voltage at Other Inputs and Outputs	$-0.3V$ to $V^+ + 0.3V$
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	
N Package	875 mW
J Package	875 mW
WM Package	875 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Note 5)	
N Package (Soldering, 10 sec.)	+260°C
J Package (Soldering, 10 sec.)	+300°C
WM Package (Vapor Phase, 60 sec.)	+215°C
WM Package (Infrared, 15 sec.)	+220°C
ESD Susceptibility (Note 6)	2 kV

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08061/2/4/8BIN, ADC08061/2/4/8CIN, ADC08061/2/4/8BIWM, ADC08061/2/4/8CIWM, ADC08061/2/4/8BIJ, ADC08061/2/4/8CIJ	$-40°C \le T_A \le 85°C$
ADC08061/2/4/8CMJ	$-55°C \le T_A \le 125°C$
Supply Voltage, (V^+)	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $\overline{RD}$ Mode, $V^+ = 5V$, $V_{REF+} = 5V$, and $V_{REF-} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
INL	Integral Non Linearity	ADC08061/2/4/8 BIN, BIJ, BIWM		**±½**	LSB (max)
		ADC08061/2/4/8 CIN, CIJ, CIWM, CMJ		**±1**	LSB (max)
TUE	Total Unadjusted Error	ADC08061/2/4 BIN, BIJ, BIWM		**±½**	LSB (max)
		ADC08068BIN, BIJ, BIWM (Note 12)		**±1**	LSB (max)
		ADC08061/2/4/8 CIN, CIJ, CIWM, CMJ		**±1**	LSB (max)
	Missing Codes			**0**	Bits (max)
	Reference Input Resistance		700 700	**500** **1250**	Ω(min) Ω (max)
V_{REF+}	Positive Reference Input Voltage			**V_{REF-}** **V^+**	V (min) V (max)
V_{REF-}	Negative Reference Input Voltage			**GND** **V_{REF+}**	V (min) V (max)
V_{IN}	Analog Input Voltage	(Note 10)		**GND − 0.1** **$V^+ + 0.1$**	V (min) V (max)
	On Channel Input Current	On Channel Input = 5V, Off Channel Input = 0V (Note 11)	−0.4	**−20**	μA (max)
		On Channel Input = 0V, Off Channel Input = 5V (Note 11)	−0.4	**−20**	μA (max)
PSS	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.75V$ All Codes Tested CMJ Suffix	±1/16	**±½** **±¾**	LSB (max)
	Effective Bits		7.8		Bits
	Full-Power Bandwidth		300		kHz
THD	Total Harmonic Distortion		0.5		%
S/N	Signal-to-Noise Ratio		50		dB
IMD	Intermodulation Distortion		50		dB

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $t_r = t_f = 10$ ns, $V_{REF+} = 5V$, $V_{REF-} = 0V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
t_{WR}	Write Time	Mode Pin to V^+; (*Figures 2a, 2b,* and *3*)	100	**100**	ns (min)
$t_{\overline{RD}}$	Read Time (Time from Falling Edge of $\overline{WR}$ to Falling Edge of $\overline{RD}$)	Mode Pin to V^+; *(Figure 2a)* CMJ Suffix	350	**350** **515**	ns (min)
$t_{\overline{RD}W}$	$\overline{RD}$ Width	Mode Pin to GND; *(Figure 4)*	200 400	**250** **400**	ns (min) ns (max)
t_{CONV}	$\overline{WR}$-$\overline{RD}$ Mode Conversion Time ($t_{\overline{WR}} + t_{\overline{RD}} + t_{ACC1}$)	Mode Pin to V^+; *(Figure 2a)* CMJ Suffix	500	**560** **790**	ns (max)
$t_{C\overline{RD}}$	$\overline{RD}$ Mode Conversion Time	Mode Pin to GND; *(Figure 1)* CMJ Suffix	655	**900** **940**	ns (max)
t_{ACC0}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 100$ pF Mode Pin to GND; *(Figure 1)* CMJ Suffix	640	**900** **940**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 10$ pF $C_L = 100$ pF Mode Pin to V^+, $t_{\overline{RD}} \leq t_{\overline{INTL}}$ *(Figure 2a)* CMJ Suffix	45 50	**110** **175**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 10$ pF $C_L = 100$ pF $t_{\overline{RD}} > t_{\overline{INTL}}$; (*Figures 2b* and *4*) CMJ Suffix	25 30	**55** **60**	ns (max)
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$R_L = 3\ k\Omega$, $C_L = 10$ pF	30	**60**	ns (min)
$t_{\overline{INTL}}$	Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	(*Figures 2b,* and *3*) Mode Pin = V^+, $C_L = 50$ pF	520	**690**	ns (max)
$t_{\overline{INTH}}$	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF; (*Figures 1, 2a, 2b,* and *4*) CMJ Suffix	50	**95** **100**	ns (max)
$t_{\overline{INTH}}$	Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF; *(Figure 3)* CMJ Suffix	45	**95** **100**	ns (max)
t_{RDY}	Delay from $\overline{CS}$ to RDY	Mode Pin = 0V, $C_L = 50$ pF, $R_L = 3\ k\Omega$ *(Figure 1)* CMJ Suffix	25	**45** **50**	ns (max)
t_{ID}	Delay from $\overline{INT}$ to Output Valid	$R_L = 3\ k\Omega$, $C_L = 100$ pF; *(Figure 3)*	0	**15**	ns (max)
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$	Mode Pin = V^+, $t_{\overline{RD}} \leq t_{\overline{INTL}}$; *(Figure 2a)* CMJ Suffix	60	**115** **175**	ns (max)
t_N	Time between End of $\overline{RD}$ and Start of New Conversion	(*Figures 1, 2a, 2b, 3* and *4*)	50	**50**	ns (min)
t_{AH}	Channel Address Hold Time	(*Figures 1, 2a, 2b, 3* and *4*)	10	**60**	ns (min)
t_{AS}	Channel Address Setup Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (max)
$t_{\overline{CSS}}$	$\overline{CS}$ Setup Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (max)
$t_{\overline{CSH}}$	$\overline{CS}$ Hold Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (min)
C_{VIN}	Analog Input Capacitance		25		pF
C_{OUT}	Logic Output Capacitance		5		pF
C_{IN}	Logic Input Capacitance		5		pF

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
V_{IH}	Logic "1" Input Voltage	$V^+ = 5.5V$ $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins Mode Pin		**2.0** **3.5**	V (min) V (min)
V_{IL}	Logic "0" Input Voltage	$V^+ = 4.5V$ $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins Mode Pin		**0.8** **1.5**	V (max) V (max)
I_{IH}	Logic "1" Input Current	$V_{IH} = 5V$ $\overline{CS}$, $\overline{RD}$, A0, A1, A2 Pins $\overline{WR}$ Pin Mode Pin	0.005 0.1 50	**1** **3** **200**	μA (max) μA (max) μA (max)
I_{IL}	Logic "0" Input Current	$V_{IL} = 0V$ $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, A1, A2 Pins Mode Pin	−0.005	**−2**	μA (max)
V_{OH}	Logic "1" Output Voltage	$V^+ = 4.75V$ $I_{OUT} = -360\ \mu A$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$ $I_{OUT} = -10\ \mu A$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$		**2.4** **4.5**	V (min) V (min)
V_{OL}	Logic "0" Output Voltage	$V^+ = 4.75V$ $I_{OUT} = 1.6\ mA$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		**0.4**	V (max)
I_O	TRI-STATE Output Current	$V_{OUT} = 5.0V$ DB0–DB7, RDY	0.1	**3**	μA (max)
		$V_{OUT} = 0V$ DB0–DB7, RDY	−0.1	**−3**	μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$	−26	**−6**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY	24	**7**	mA (min)
I_C	Supply Current	$\overline{CS} = \overline{WR} = \overline{RD} = 0$	11.5	**20**	mA (max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltage ($V_{IN} < GND$ or $V_{IN} > V^+$), the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current specification limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: The power dissipation of this device under normal operation should never exceed 875 mW (Quiescent Power Dissipation + TTL Loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (e.g., when any input or output exceeds the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{JMAX} and θ_{JA} for the various packages and versions of the ADC08061/2/4/8.

Part Number	T_{JMAX}	θ_{JA}
ADC08061/2BIJ	105	96
ADC08061/2CIJ	105	96
ADC08061/2CMJ	145	59
ADC08061/2BIN	105	51
ADC08061/2CIN	105	51
ADC08061/2BIWM	105	85
ADC08061/2CIWM	105	85
ADC08064BIJ	105	83
ADC08064CIJ	105	83
ADC08064CMJ	145	53
ADC08064BIN	105	44
ADC08064CIN	105	44
ADC08064BIWM	105	82
ADC08064CIWM	105	82
ADC08068BIJ	105	81
ADC08068CIJ	105	81
ADC08068CMJ	145	51
ADC08068BIN	105	43
ADC08068CIN	105	43
ADC08068BIWM	105	78
ADC08068CIWM	105	78

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at 25°C and represent most likely parametric norm.

Note 8: Limits are guaranteed to National's AOQL (Average Output Quality Level).

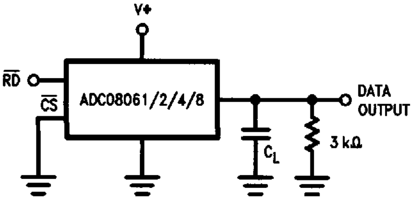
Note 9: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 10: Two on-chip diodes are tied to each analog input and are reversed biased during normal operation. One is connected to V^+ and the other is connected to GND. They will become forward biased and conduct when an analog input voltage is equal to or greater than one diode drop above V^+ or below GND. Therefore, caution should be exercised when testing with $V^+ = 4.5V$. Analog inputs with magnitudes equal to 5V can cause an input diode to conduct, especially at elevated temperatures. This can create conversion errors for analog signals near full-scale. The specification allows 50 mV forward bias on either diode; e.g., the output code will be correct as long as the analog input signal does not exceed the supply voltage by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. An absolute analog input signal voltage range of $0V \leq V_{IN} \leq 5V$ can be achieved by ensuring that the minimum supply voltage applied to V^+ is 4.950V over temperature variations, initial tolerance, and loading.

Note 11: Off-channel leakage current is measured after the on-channel selection.

Note 12: For the "B" grade parts, the offset error for V_{IN7} and V_{IN8} is up to ¼ LSB larger than for the other channels. Therefore, the Total Unadjusted Error (TUE) for the ADC08068 is ½ LSB larger than for the ADC08061, ADC08062, and ADC08064. Linearity error is unaffected.

TRI-STATE Test Circuits and Waveforms



t_{1H}

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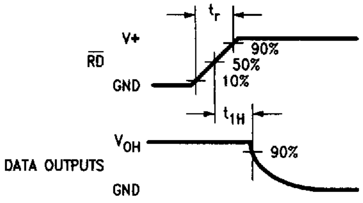

t_{1H}, C_L = 10 pF

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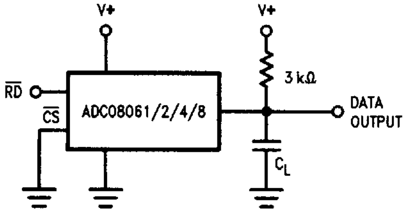
t_r = 10 ns



t_{0H}

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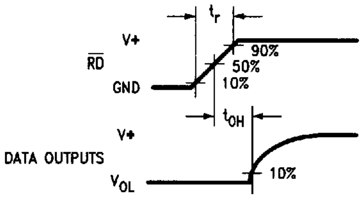

t_{0H}, C_L = 10 pF

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t_r = 10 ns

Timing Diagrams

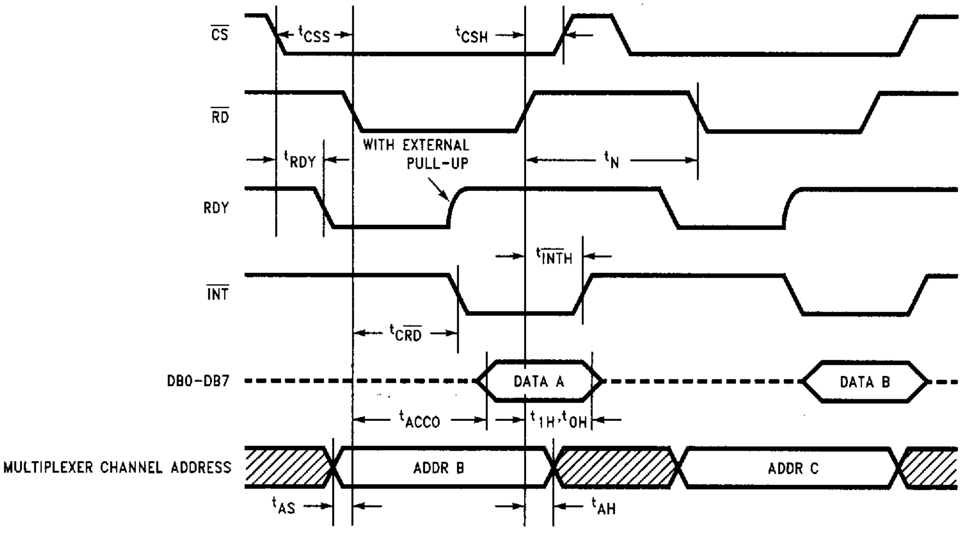

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FIGURE 1. $\overline{RD}$ Mode (Mode Pin is Low)

Timing Diagrams (Continued)

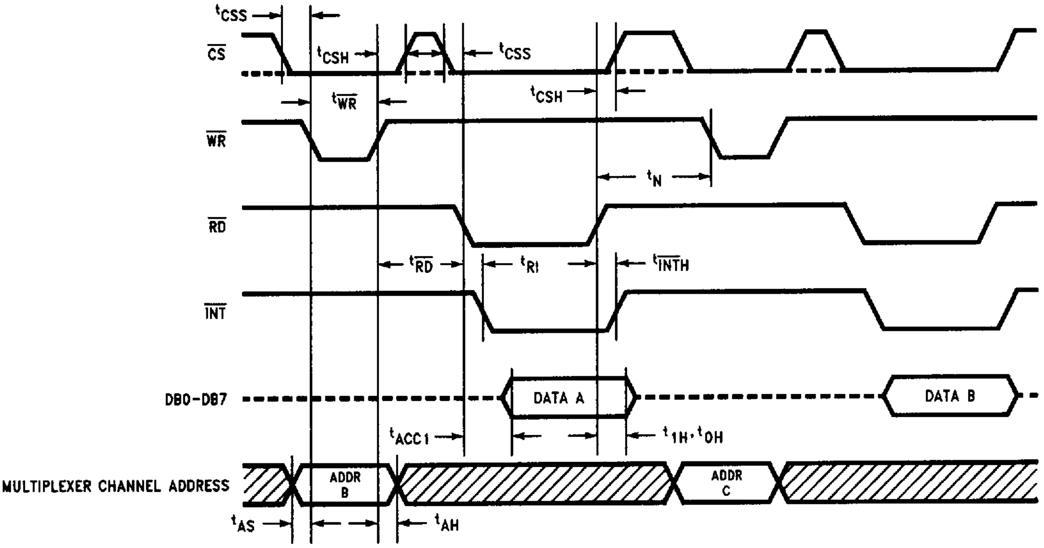

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FIGURE 2a. $\overline{WR}$-$\overline{RD}$ **Mode (Mode Pin is High and** $t_{\overline{RD}} \le t_{\overline{INTL}}$**)**

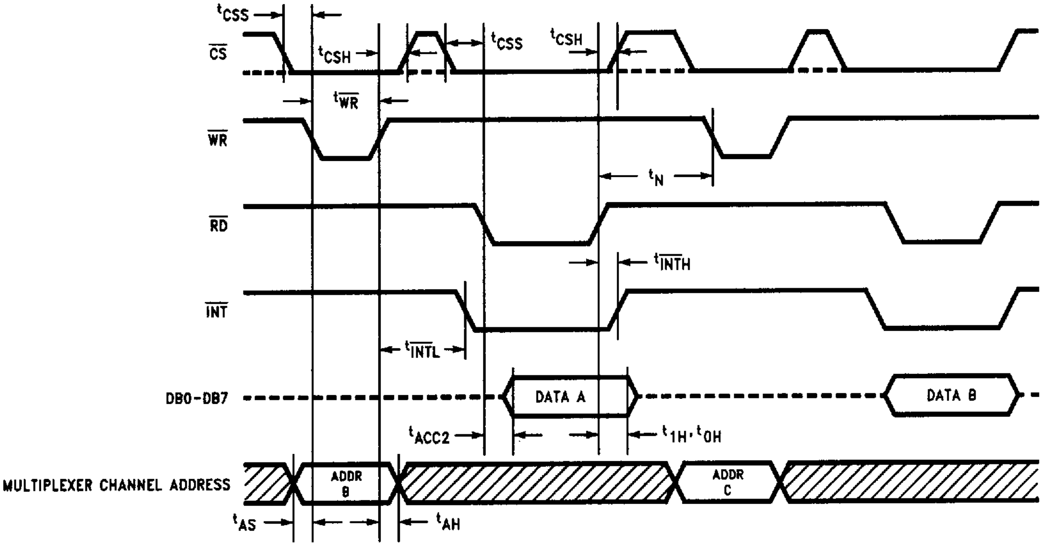

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FIGURE 2b. $\overline{WR}$-$\overline{RD}$ **Mode (Mode Pin is High and** $t_{\overline{RD}} > t_{\overline{INTL}}$**)**

Timing Diagrams (Continued)

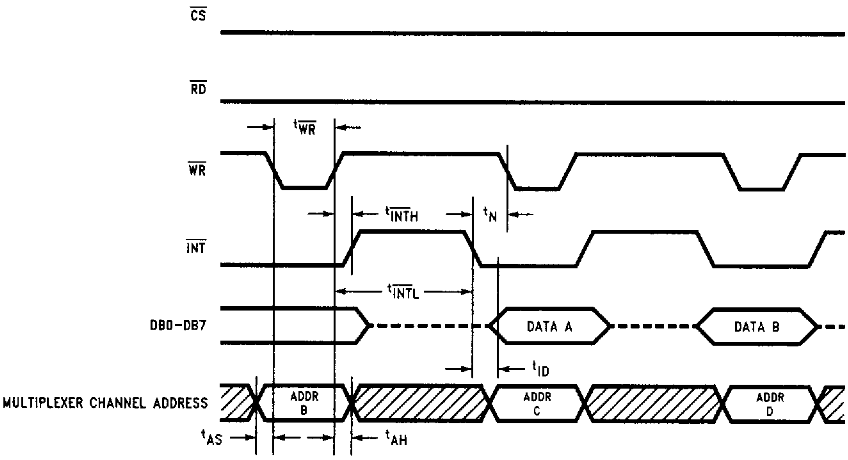

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FIGURE 3. $\overline{\text{WR}}$-$\overline{\text{RD}}$ **Mode (Mode Pin is High) Reduced Interface System Connection (**$\overline{\text{CS}} = \overline{\text{RD}} = 0$**)**

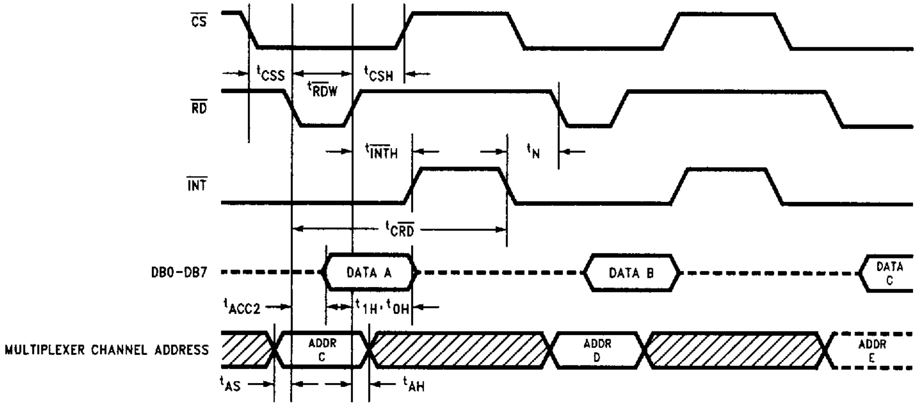

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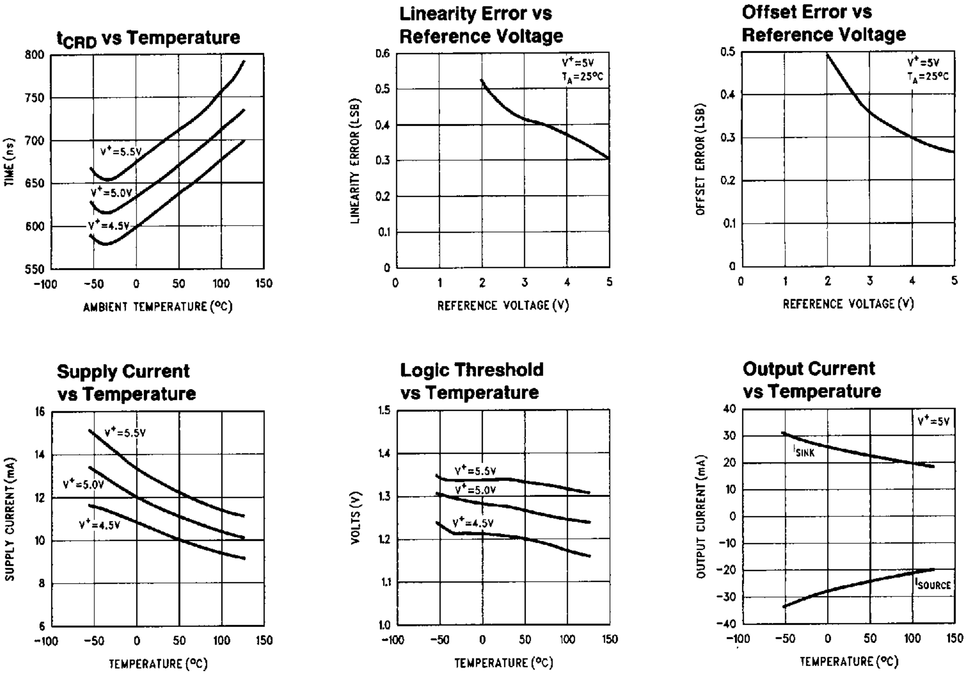
FIGURE 4. $\overline{\text{RD}}$ **Mode (Pipeline Operation) (Mode Pin is Low and** $t_{\overline{RDW}}$ **must be between 200 ns and 400 ns)**

Typical Performance Characteristics



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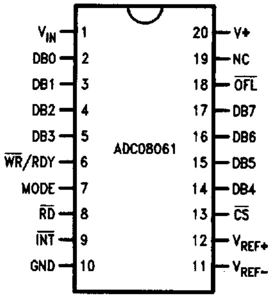
Connection Diagrams



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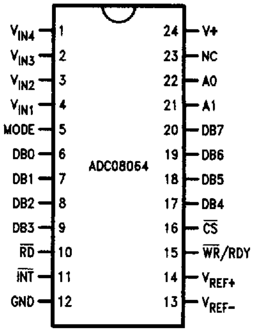
Dual-In-Line and Wide-Body Small-Outline Packages J20A, N20A or M20B



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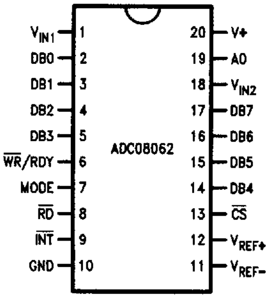
Dual-In-Line and Wide-Body Small-Outline Packages J24A, N24A or M24B



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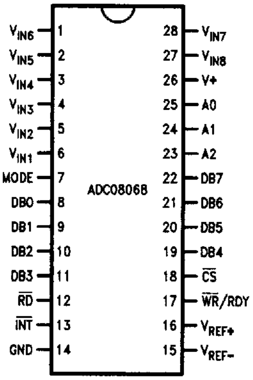
Dual-In-Line and Wide-Body Small-Outline Packages J20A, N20A or M20B



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Dual-In-Line and Wide-Body Small-Outline Packages J28A, N28B or M28B

Ordering Information

Industrial ($-40°C \le T_A \le 85°C$)	Package
ADC08061BIN, ADC08061CIN, ADC08062BIN, ADC08062CIN	N20A
ADC08064BIN, ADC08064CIN	N24C
ADC08068BIN, ADC08068CIN	N28B
ADC08061BIWM, ADC08061CIWM, ADC08062BIWM, ADC08062CIWM	M20B
ADC08064BIWM, ADC08064CIWM	M24B
ADC08068BIWM, ADC08068CIWM	M28B
ADC08061BIJ, ADC08061CIJ, ADC08062BIJ, ADC08062CIJ	J20A
ADC08064BIJ, ADC08064CIJ	J24A
ADC08068BIJ, ADC08068CIJ	J28A
Military ($-55°C \le T_A \le 125°C$)	**Package**
ADC08061CMJ, ADC08062CMJ	J20A
ADC08064CMJ	J24A
ADC08068CMJ	J28A

Pin Description

V_{IN}, V_{IN1-8}	These are analog inputs. The input range is GND−50 mV ≤ V_{INPUT} ≤ V^+ + 50 mV. The ADC08061 has a single input (V_{IN}), the ADC08062 has a two-channel multiplexer (V_{IN1-2}), the ADC08064 has a four-channel multiplexer (V_{IN1-4}), and the ADC08068 has an eight-channel multiplexer (V_{IN1-8}).
DB0–DB7	TRI-STATE data outputs—bit 0 (LSB) through bit 7 (MSB).
$\overline{WR}$/RDY	**$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin) **$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (see *Figures 2a, 2b,* and *3*). **$\overline{RD}$ Mode** (Logic low applied to MODE pin) **RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and return high at the end of conversion.
MODE	**Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input—This pin is pulled to a logic low through an internal 50 μA current sink when left unconnected. **$\overline{RD}$ Mode** is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears. **$\overline{WR}$-$\overline{RD}$ Mode** is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.
$\overline{RD}$	**$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin) This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (see *Figures 2a, 2b* and *3*). **$\overline{RD}$ Mode** (logic low on the MODE pin) With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (see *Figures 1* and *4*).
$\overline{INT}$	This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.
GND	This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.
V_{REF-} V_{REF+}	These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} − 1.5 LSB produces an output code of 255. For the ADC08062/4/8, an input voltage on any unselected input that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create errors in a selected channel that is operating within proper operating conditions.
$\overline{CS}$	This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.
$\overline{OFL}$	Overflow Output. If the analog input is higher than V_{REF+} − ½ LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08061s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.
NC	No connection.
A0, A1, A2	On the ADC08062, ADC08064 and ADC08068, these logic inputs are used to select one of the input multiplexer's channels. The ADC08062 has a single multiplexer control input (A0), the ADC08064 has two multiplexer control inputs (A0 and A1), and the ADC08064 has three multiplexer control inputs (A0, A1, and A2). A channel is selected as shown in the table below.

ADC08062	**ADC08064**		**ADC08068**			**Channel**
A0	**A1**	**A0**	**A2**	**A1**	**A0**	
0	0	0	0	0	0	V_{IN1}
1	0	1	0	0	1	V_{IN2}
	1	0	0	1	0	V_{IN3}
	1	1	0	1	1	V_{IN4}
			1	0	0	V_{IN5}
			1	0	1	V_{IN6}
			1	1	0	V_{IN7}
			1	1	1	V_{IN8}

V^+	Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 μF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

Application Information

1.0 FUNCTIONAL DESCRIPTION

The ADC08061, ADC08062, ADC08064, and ADC08068 perform an 8-bit analog-to-digital conversion using a multi-step flash technique. The first flash generates the five most significant bits (MSBs) and the second flash generates the three least significant bits (LSBs). *Figure 5* shows the major functional blocks of the ADC08061/2/4/8's multi-step flash converter. It consists of an over-encoded 2½-bit Voltage Estimator, an internal DAC with two different voltage spans, a 3-bit half-flash converter and a comparator multiplexer.

The resistor string near the center of the block diagram in *Figure 5* forms the internal main DAC. Each of the eight resistors at the bottom of the string is equal to 1/256 of the total string resistance. These resistors form the **LSB Ladder** and have a voltage drop of 1/256 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remaining resistors make up the **MSB Ladder**. They are made up of eight groups of four resistors connected in series. Each MSB Ladder section has ⅛ of the total reference voltage across it. Within a given MSB Ladder section, each of the MSB resistors has 8/256, or 1/32 of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB Ladders. Through the Comparator Multiplexer these tap points can be connected, in groups of eight, to the eight comparators shown at the right of *Figure 5*. This function provides the necessary reference voltages to the comparators during each flash conversion.

The six comparators, seven-resistor string (estimator DAC), and Estimator Decoder at the left of *Figure 5* form the Voltage Estimator. The estimator DAC connected between V_{REF+} and V_{REF-} generates the reference voltages for the six Voltage Estimator comparators. These comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is then used to control the Comparator Multiplexer, connecting the appropriate MSB Ladder section to the eight flash comparators. Only 14 comparators, six in the Voltage Estimator and eight in the flash converter, are needed to achieve the full eight-bit resolution, instead of 32 comparators that would be needed by traditional half-flash methods.

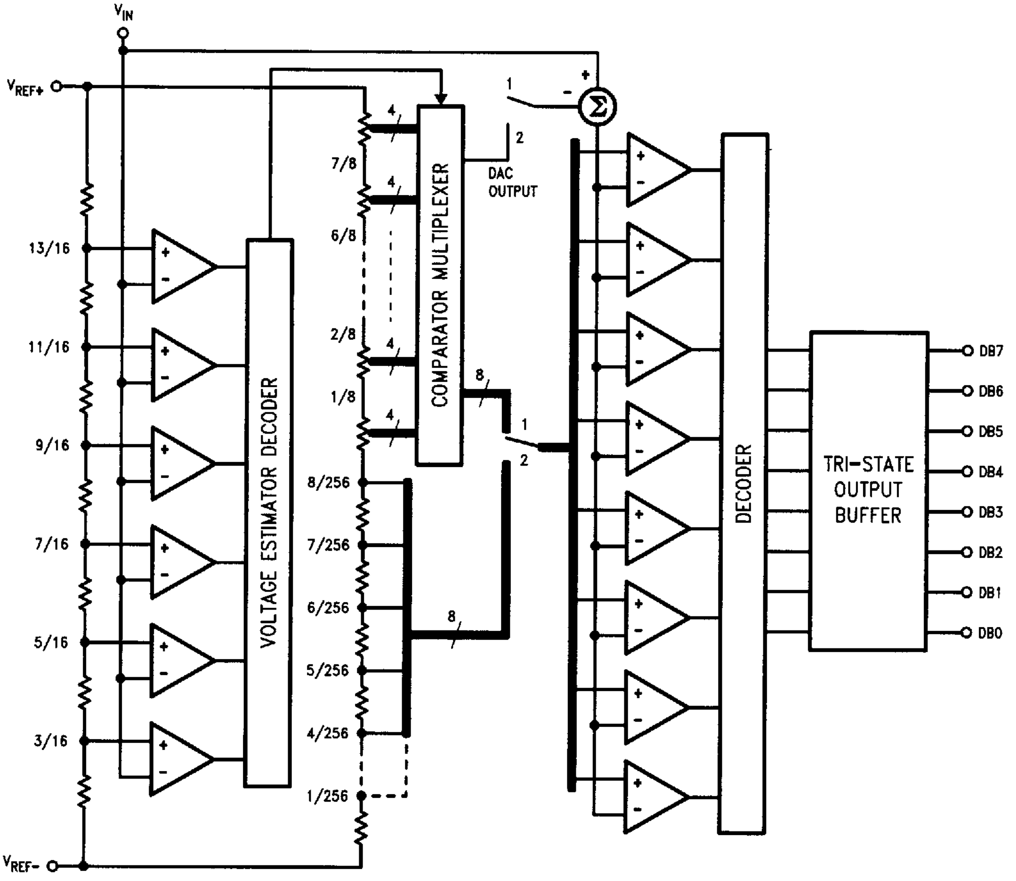

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FIGURE 5. Block Diagram of the ADC0806X Multi-Step Flash Architecture

Application Information (Continued)

A conversion begins with the Voltage Estimator comparing the analog input signal against the six tap voltages on the estimator DAC. The estimator decoder then selects one of the groups of tap points along the MSB Ladder. These eight tap points are then connected to the eight flash comparators. For example, if the analog input signal applied to V_{IN} is between 0 and $^{3}/_{16}$ of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the eight tap points between 8/256 and 2/8 of V_{REF} and connects them to the eight flash comparators. The first flash conversion is now performed, producing the five MSBs of data.

The remaining three LSBs are generated next using the same eight comparators that were used for the first flash conversion. As determined by the results of the MSB flash, a voltage from the MSB Ladder equivalent to the magnitude of the five MSBs is subtracted from the analog input voltage as the upper switch is moved from position one to position two. The resulting remainder voltage is applied to the eight flash comparators and, with the lower switch in position two, compared with the eight tap points from the LSB Ladder.

By using the same eight comparators for both flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard half-flash techniques.

Voltage Estimator errors as large as $^{1}/_{16}$ of V_{REF} (16 LSBs) will be corrected since the flash comparators are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if $^{7}/_{16}\ V_{REF} < V_{IN} < {}^{9}/_{16}\ V_{REF}$ the Voltage Estimator's comparators tied to the tap points below $^{9}/_{16}\ V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The eight flash comparators will be placed at the MSB Ladder tap points between $^{3}/_{8}\ V_{REF}$ and $^{5}/_{8}\ V_{REF}$. The overlap of $^{1}/_{16}\ V_{REF}$ on each side of the Voltage Estimator's span will automatically correct an error of up to 16 LSBs (16 LSBs = 312.5 mV for $V_{REF} = 5V$). If the first flash conversion determines that the input voltage is between $^{3}/_{8}\ V_{REF}$ and $4/8\ V_{REF} - LSB/2$, the Voltage Estimator's output code will be corrected by subtracting "1". This results in a corrected value of "01". If the first flash conversion determines that the input voltage is between $8/16\ V_{REF} - LSB/2$ and $^{5}/_{8}\ V_{REF}$, the Voltage Estimator's output code remains unchanged.

After correction, the 2-bit data from both the Voltage Estimator and the first flash conversion are decoded to produce the five MSBs. Decoding is similar to that of a 5-bit flash converter since there are 32 tap points on the MSB Ladder. However, 31 comparators are not needed since the Voltage Estimator places the eight comparators along the MSB Ladder where reference tap voltages are present that fall above and below the magnitude of V_{IN}. Comparators are not needed outside this selected range. If a comparator's output is a "0", all comparators above it will also have outputs of "0" and if a comparator's output is a "1", all comparators below it will also have outputs of "1".

2.0 DIGITAL INTERFACE

The ADC08061/2/4/8 has two basic interface modes which are selected by connecting the **MODE** pin to a logic high or low.

2.1 $\overline{RD}$ Mode

With a logic low applied to the **MODE** pin, the converter is set to **Read** mode. In this configuration (see *Figure 1*), a complete version is done by pulling $\overline{RD}$ low, and holding low, until the conversion is complete and output data appears. This typically takes 655 ns. The $\overline{INT}$ (interrupt) line goes low at the end of conversion. A typical delay of 50 ns is needed between the rising edge of $\overline{RD}$ (after the end of a conversion) and the start of the next conversion (by pulling $\overline{RD}$ low). The RDY output goes low after the falling edge of $\overline{CS}$ and goes high at the end-of-conversion. It can be used to signal a processor that the converter is busy or serve as a system Transfer Acknowledge signal. For the ADC08062/4/8 the data generated by the first conversion cycle after power-up is from an unknown channel.

2.2 $\overline{RD}$ Mode Pipelined Operation

Applications that require shorter $\overline{RD}$ pulse widths than those used in the **Read** mode as described above can be achieved by setting $\overline{RD}$'s width between 200 ns–400 ns *(Figure 4)*. $\overline{RD}$ pulse widths outside this range will create conversion linearity errors. These errors are caused by exercising internal interface logic circuitry using $\overline{CS}$ and/or $\overline{RD}$ during a conversion.

When $\overline{RD}$ goes low, a conversion is initiated and the data from the previous conversion is available on the DB0–DB7 outputs. Reading D0–D7 for the first two times after power-up produces random data. The data will be valid during the third $\overline{RD}$ pulse that occurs after the first conversion.

2.3 $\overline{WR}$-$\overline{RD}$ ($\overline{WR}$ then $\overline{RD}$) Mode

The ADC08061/2/4/8 is in the **$\overline{WR}$-$\overline{RD}$ mode** with the **MODE** pin tied high. A conversion starts on the falling edge of the $\overline{WR}$ signal. There are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for the $\overline{INT}$ output to go low before reading the conversion result (see *Figure 2b*). Typically, $\overline{INT}$ will go low 520 ns, maximum, after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 350 ns (see *Figure 2a*). If $\overline{RD}$ is pulled low before $\overline{INT}$ goes low, $\overline{INT}$ will immediately go low and data will appear at the outputs. This is the fastest operating mode ($t_{RD} \le t_{INTL}$) with a conversion time, including data access time, of 560 ns. Allowing 100 ns for reading the conversion data and the delay between conversions gives a total throughput time of 660 ns (throughput rate of 1.5 MHz).

2.4 $\overline{WR}$-$\overline{RD}$ Mode with Reduced Interface System Connection

$\overline{CS}$ and $\overline{RD}$ can be tied low, using only $\overline{WR}$ to control the start of conversion for applications that require reduced digital interface while operating in the **$\overline{WR}$-$\overline{RD}$ mode** *(Figure 3)*. Data will be valid approximately 705 ns following $\overline{WR}$'s rising edge.

2.5 Multiplexer Addressing

The ADC08062, ADC08064, and ADC08068 have, respectively, 2, 4, and 8 channel multiplexed inputs. These are

Application Information (Continued)

selected using A0 (ADC08062), A0–A1 (ADC08064), and A0–A2 (ADC08068) multiplexer channel selection inputs. Table I shows the input code needed to select a given channel. The multiplexer address is latched when received but the multiplexer channel is updated after the completion of the current conversion.

TABLE I. Multiplexer Addressing

ADC08062	ADC08064		ADC08068			Channel
A0	A1	A0	A2	A1	A0	
0	0	0	0	0	0	V_{IN1}
1	0	1	0	0	1	V_{IN2}
	1	0	0	1	0	V_{IN3}
	1	1	0	1	1	V_{IN4}
			1	0	0	V_{IN5}
			1	0	1	V_{IN6}
			1	1	0	V_{IN7}
			1	1	1	V_{IN8}

The multiplexer address data must be valid at the time of $\overline{RD}$'s falling edge, remain valid during the conversion, and can go high after $\overline{RD}$ goes high when operating in the **Read Mode**.

The multiplexer address data should be valid at or before the time of $\overline{WR}$'s falling edge, remain valid while $\overline{WR}$ is low, and go invalid after $\overline{WR}$ goes high when operating in the **$\overline{WR}$-$\overline{RD}$ Mode**.

3.0 REFERENCE INPUTS

The two V_{REF} inputs of the ADC08061/2/4/8 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to vary the span of the analog input since this range will be equivalent to the voltage difference between V_{REF+} and V_{REF-}. Transducers with minimum output voltages above GND can also be compensated by connecting V_{REF-} to a voltage that is equal to this minimum voltage. By reducing V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF} = 2.5V$, then 1 LSB = 9.8 mV). The ADC08061/2/4/8's reference arrangement also facilitates ratiometric operation and in many cases the ADC08061/2/4/8's power supply can be used for transducer power as well as the V_{REF} source. Ratiometric operation is achieved by connecting V_{REF-} to GND and connecting V_{REF+} and a transducer's power supply input to V^+. The ADC08061/2/4/8's linearity degrades when $V_{REF+} - |V_{REF-}|$ is less than 2.0V.

The voltage at V_{REF-} sets the input level that produces a digital output of all zeros. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for some measurement applications. *Figure 6* shows one possible differential configuration.

It should be noted that, while the two V_{REF} inputs are fully differential, the digital output will be zero for any analog input voltage if $V_{REF-} \geq V_{REF+}$.

4.0 ANALOG INPUT AND SOURCE IMPEDANCE

The ADC08061/2/4/8's analog input circuitry includes an analog switch with an "on" resistance of 70Ω and capacitance of 1.4 pF and 12 pF (see *Figure 6*). The switch is closed during the A/D's input signal acquisition time (while $\overline{WR}$ is low when using the $\overline{WR}$-$\overline{RD}$ Mode). A small transient current flows into the input pin each time the switch closes. A transient voltage, whose magnitude can increase as the source impedance increases, may be present at the input. So long as the source impedance is less than 500Ω, the input voltage transient will not cause errors and need not be filtered.

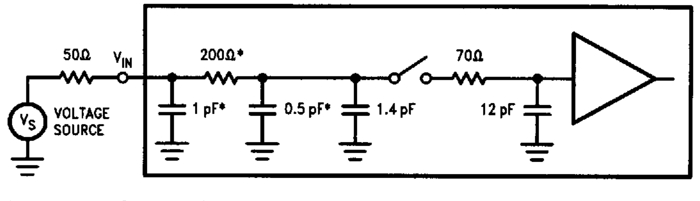
Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (100 ns maximum). A signal source with a high output impedance should have its output buffered with an operational amplifier. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 100 mV and less than V^+ + 100 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than V^+, or more than 300 mV lower than GND. The current flowing through any analog input pin should be limited to 5 mA or less to avoid permanent damage to the IC if an analog input pin is forced beyond these voltages. The sum of all the overdrive currents into all pins must be less than 20 mA. Some sort of protection scheme should be used when the input signal is expected to extend more than 300 mV beyond the power supply limits. A simple protection network using resistors and diodes is shown in *Figure 8*.

6.0 INHERENT SAMPLE-AND-HOLD

An important benefit of the ADC08061/2/4/8's input architecture is the inherent sample-and-hold (S/H) and its ability to measure relatively high speed signals without the help of an external S/H. In a non-sampling converter, regardless of its speed, the input must remain stable to at least ½ LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion.

The ADC08061, ADC08062, ADC08064, and ADC08068 are suitable for DSP-based systems because of the direct



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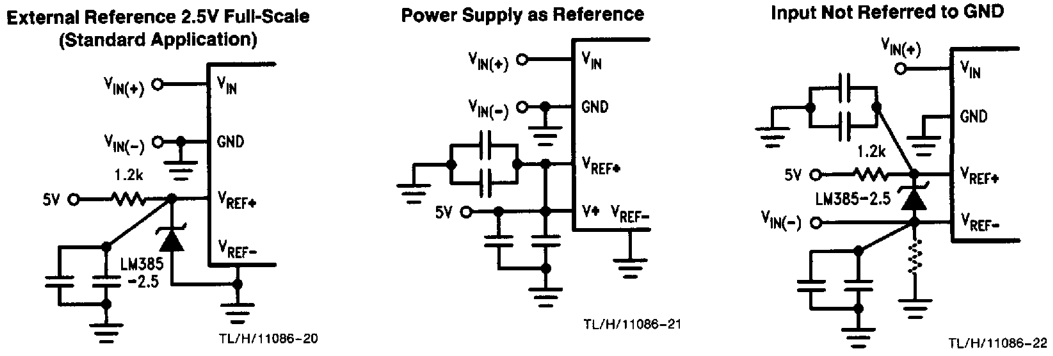
*Represents a multiplexer channel in the ADC08062, ADC08064, and ADC08068.

FIGURE 6. ADC08061, ADC08062, ADC08064, and ADC08068 Equivalent Input Circuit Model

Application Information (Continued)



External Reference 2.5V Full-Scale (Standard Application)

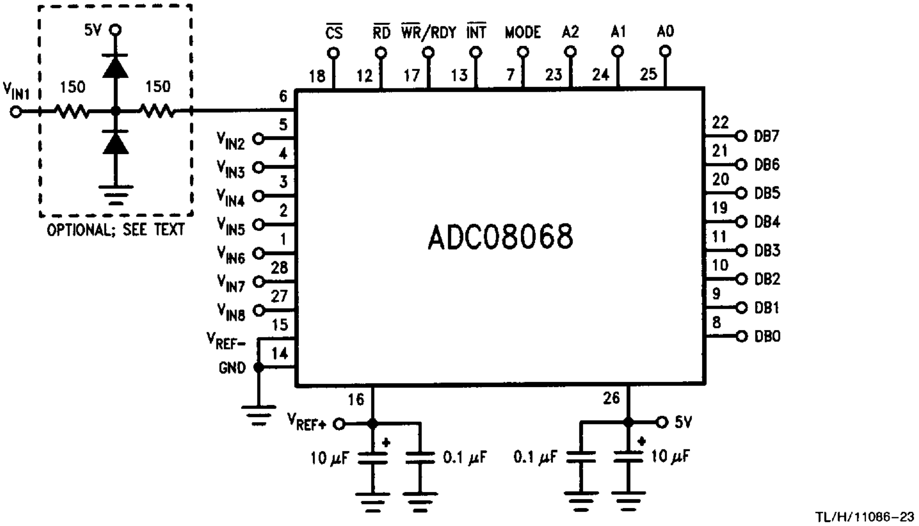
Power Supply as Reference

Input Not Referred to GND

*Signal source driving $V_{IN}(-)$ must be capable of sinking 5 mA.

Note: Bypass capacitors consist of a 0.1 μF ceramic in parallel with a 10 μF bead tantalum.

FIGURE 7. Analog Input Options



Note the multiple bypass capacitors on the reference and power supply pins. V_{REF-} should be bypass to analog ground using multiple capacitors if it is not grounded (see Section 7.0 "Layout, Grounds, and Bypassing"). V_{IN1} is shown with an optional input protection network.

FIGURE 8. Typical Connection

control of the S/H through the $\overline{WR}$ signal. The $\overline{WR}$ input signal allows the A/D to be synchronized to a DSP system's sampling rate or to other ADC08061, ADC08062, ADC08064, and ADC08068s.

The ADC08061 can perform accurate conversions of full-scale input signals at frequencies from dc to more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

7.0 LAYOUT, GROUNDS, AND BYPASSING

In order to ensure fast, accurate conversions from the ADC08061/2/4/8, it is necessary to use appropriate circuit board layout techniques. Ideally, the analog-to-digital converter's ground reference should be low impedance and free of noise from other parts of the system. Digital circuits can produce a great deal of noise on their ground returns and, therefore, should have their own separate ground lines. Best performance is obtained using separate ground planes for the digital and analog parts of the system.

The analog inputs should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., an input filter capacitor) connected across the inputs should be returned to a very clean ground point. Incorrectly grounding the ADC08061/2/4/8 will result in reduced conversion accuracy.

The V^+ supply pin, V_{REF+}, and V_{REF-} (if not grounded) should be bypassed with a parallel combination of a 0.1 μF ceramic capacitor and a 10 μF tantalum capacitor placed as close as possible to the supply pin using short circuit board traces. See *Figures 7* and *8*.