BR6216B-10LL

Static RAM, 2k × 8 bit

The BR6216B-10LL is a CMOS static random access memory (SRAM) with a memory size of 2048 words × 8 bits.

It can be operated from a single 5-V power supply and it has inputs and outputs that can be directly connected to other TTL devices.

Access and cycle times are both 100 ns (maximum) so timing design is simple and data can be processed very quickly.

Features

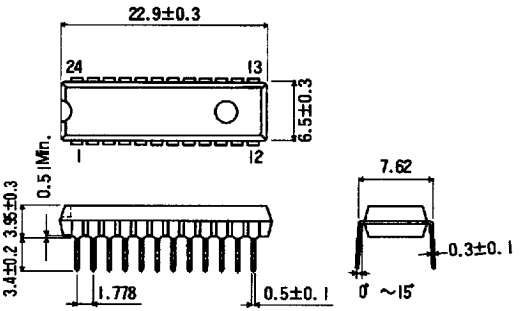
- available in an SDIP-24 package
- single 5 V power supply (±10%). Can maintain information at voltages as low as 2 V. Suitable for equipment with small battery backup.
- fast read access time, typically 100 ns
- input and output pins are common: three output states
- clock is unnecessary since it is an asynchronous static circuit
- common mode input and output data
- Both $\overline{CS}$ and $\overline{OE}$ signals are supported so it can be connected to other devices through an OR gate.

Applications

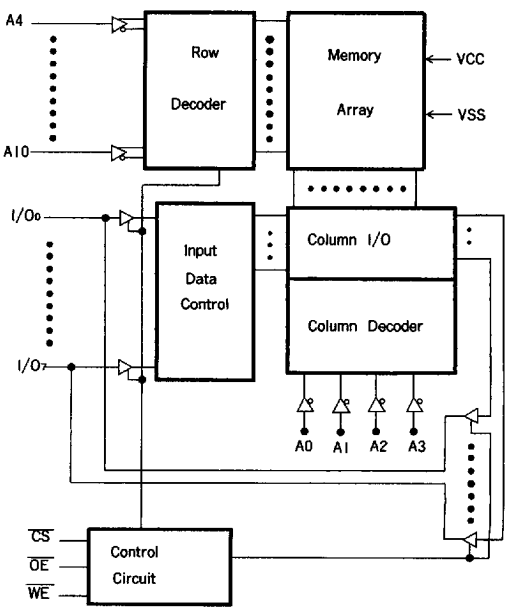
- multipurpose memory chip

Dimensions (Units : mm)

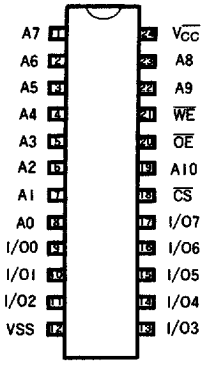
BR6216B-10LL (SDIP-24)



Block diagram



Pin description



Pin no.	Pin name	Function
24	V_{CC}	5 V ±10% power supply
12	V_{SS}	Standard input and output voltage, 0 V
1 ~ 8, 19, 22 ~ 23	A0 ~ A10	2048-word memory address input
9 ~ 11, 13 ~ 17	I/00 ~ I/07	8-bit data input/output
18	$\overline{CS}$	Chip select control input
20	$\overline{OE}$	Output enable control input
21	$\overline{WE}$	Write enable control input

Absolute maximum ratings

Parameter	Symbol	Limits	Unit	Conditions
Applied voltage	V_{CC}	–0.5 ~ +7.0	V	For a 50 ns pulse width, –3.0 V minimum
Power dissipation	P_d	600	mW	Reduce power by 6 mW/°C for each degree above 25°C.
Voltage for each pin input/output voltage	V_I	–55 ~ V_{CC} +0.5	V	
Storage temperature	T_{stg}	–55 ~ +125	°C	
Operating temperature	T_{opr}	0 ~ +70	°C	

Recommended operating conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
High level input/output voltage	V_{IH}	2.2		V_{CC} +0.5	V
Low level input/output voltage	V_{IL}	–0.3		0.8	V
Ambient temperature	T_a	0		70	°C

Electrical characteristics (unless otherwise noted, V_{CC} = 5 V, T_a = 25°C)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Input voltage low	V_{IL}	–0.3		0.8	V	For a 50 ns or less pulse width at a voltage of –3.0 V
Input voltage high	V_{IH}	2.2		V_{CC}+0.5	V	
Output voltage low	V_{OL}	0		0.4	V	I_{OL} = 2.1 mA
Output voltage high	V_{OH}	2.4		V_{CC}	V	I_{OH} = –1.0 mA
Input leak current	I_{LI}			±1	µA	V_{IN} = 0 V ~ V_{CC}
Output leak current	I_{LO}			±1	µA	V_{OUT} = 0 V ~ V_{CC}
Operating current 1	I_{CC1}			30	mA	$\overline{CS}$ = V_{IL}, I/O: OPEN
Operating current 2	I_{CC2}			10	mA	$\overline{CS}$ = V_{IL}, I/O: OPEN, f = 1 MHz
Standby current 1	I_{SB}			3	mA	$\overline{CS}$ = V_{IH}
Standby current 2	I_{SB1}		1	20	µA	$\overline{CS}$ ≥ V_{CC} –0.2 V

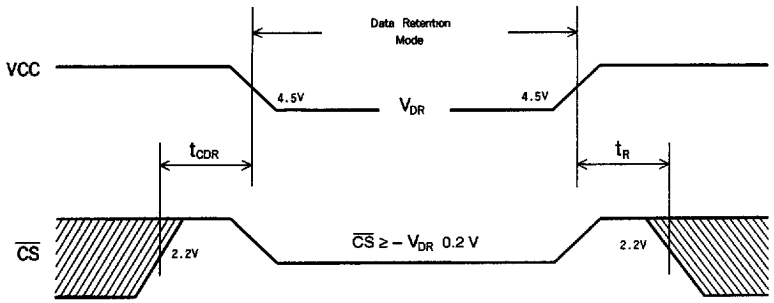
Operating mode

Control pin			Mode	I/O	Power consumption
$\overline{OE}$	$\overline{CS}$	$\overline{WE}$			
X	H	X	Wait state	High impedance	Wait state
H	L	H	Output disable	High impedance	Operating state
L	L	H	Read	Data output	Operating state
X	L	L	Write	Data output	Operating state
where: X = V_{IL} or V_{IH}					

Data holding characteristics at low voltage (T_a = 0 ~ 70°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typical	Max		
Voltage required to hold data	V_{DR}	2.0		5.5	V	$\overline{CS}$ ≥ V_{DR} –0.2 V
Data holding current	I_{CCR}		0.5	10	µA	$\overline{CS}$ ≥ V_{DR} –0.2 V, V_{DR} = 3.0 V. When T_a = 0 ~ 40°C, I_{CCR} = 2 µA max
$\overline{CS}$ holding time	t_{CDR}	0			ns	
Operating recovery time	t_R	t_{RC}			ns	t_{RC} = read cycle time

Figure 1 Data holding waveform at low voltage



Note: In the data hold mode, all inputs except $\overline{CS}$ are in a high impedance state.

AC test conditions (T_a = 0 ~ 70°C, V_{CC} = 5 V ±10%)

Input pulse level: 0.8 ~ 2.4 V
Input rise, fall time: 5 ns
Input output timing level: 1.5 V
Output load: One TTL gate and CL = 100 pF

Read cycle timing

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	100		ns
Address access time	t_{AA}		100	ns
Chip enable access time ($\overline{CS}$)	t_{ACS}		100	ns
Output enable access time	t_{OE}		40	ns
Output hold time	t_{OH}	10		ns
$\overline{CS}$ output set time	t_{LZ}	10		ns
Output enable output set time	t_{OLZ}	5		ns
Chip deselect output floating	t_{HZ}		35	ns
Chip disable output floating	t_{OHZ}		35	ns

Write cycle timing

Parameter	Symbol	Min	Max	Unit
Write cycle time	t_{WC}	100		ns
Chip select time	t_{CW}	80		ns
Address valid time	t_{AW}	80		ns
Address set up time	t_{AS}	0		ns
Write pulse width	t_{WP}	60		ns
$\overline{WE}$ output delay time	t_{WR}	0		ns
$\overline{CS}$ output delay time	t_{WR1}	0		ns
$\overline{WE}$ - output floating time	t_{WHZ}		35	ns
Input data set time	t_{DW}	40		ns
Input data holding time	t_{DH}	0		ns
$\overline{WE}$ - output set time	t_{OW}	5		ns

Figure 2 Read cycle timing chart 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

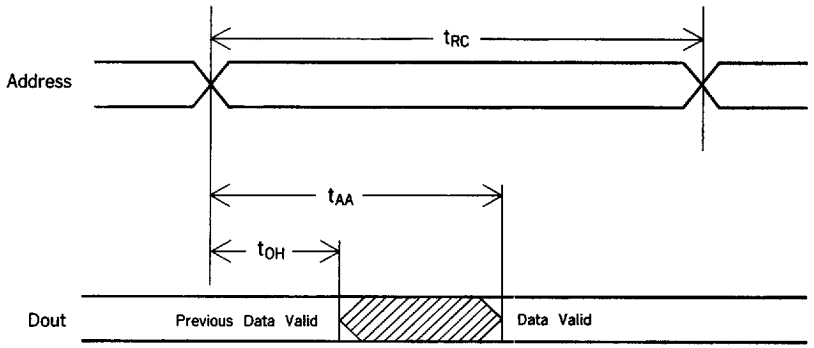


Figure 3 Read cycle timing chart 2 ($\overline{WE}$ = V_{IH})

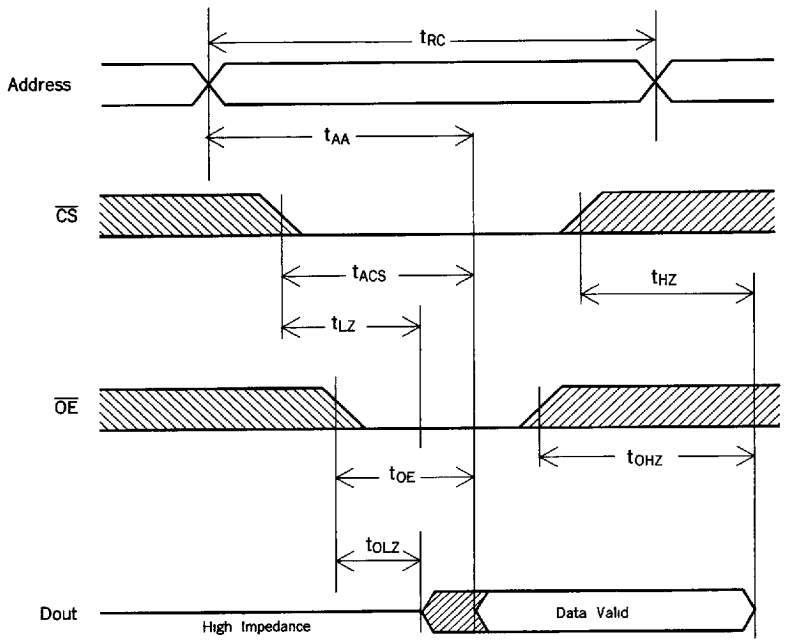


Figure 4 Write cycle timing chart 1 ($\overline{WE}$ control)

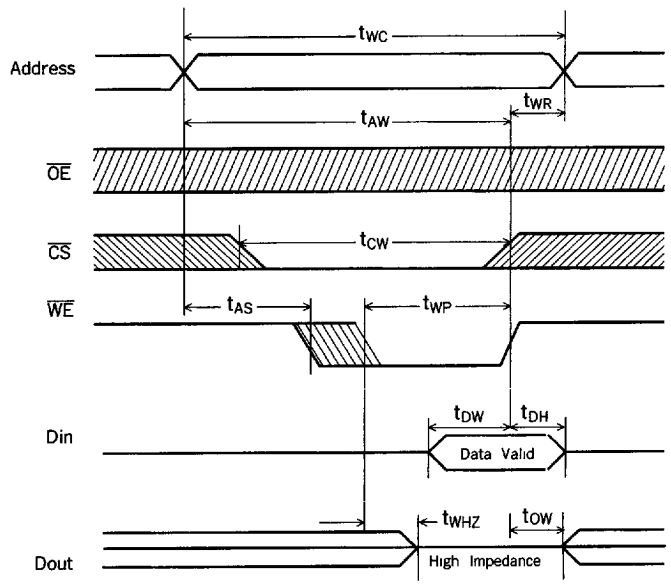
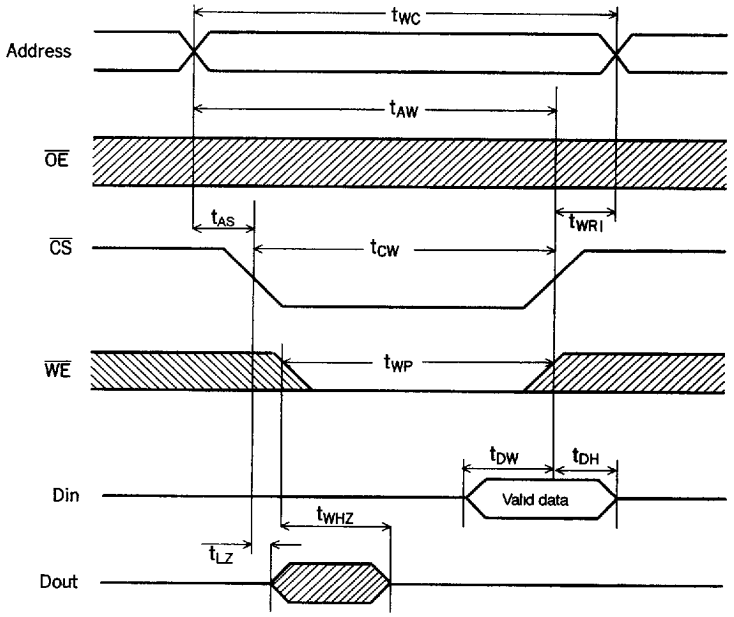


Figure 5 Write cycle timing chart 1 ($\overline{CS}$ control)



Note 1: Do not apply an input signal of the opposite phase to the output signal while the I/O pin is in the output state.

Note 2: The write occurs while the $\overline{CS}$ low level and the $\overline{WE}$ low level overlap.

Note 3: When $\overline{OE}$ is at a high level, the output is in a high impedance state.

Electrical characteristic curves

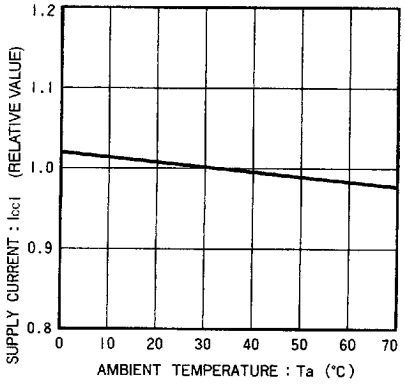


Figure 6

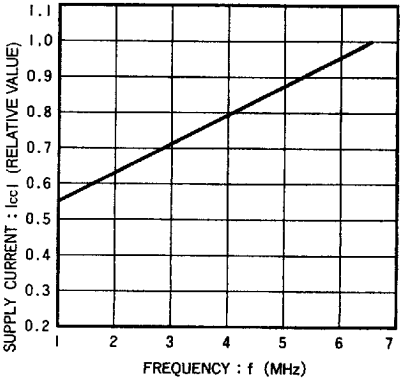


Figure 7

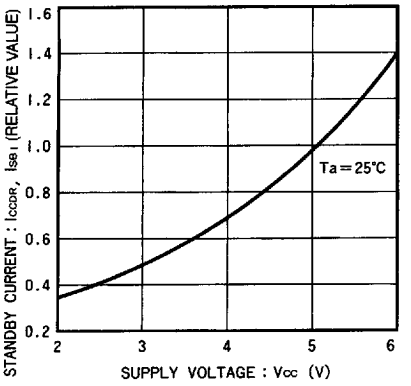


Figure 8

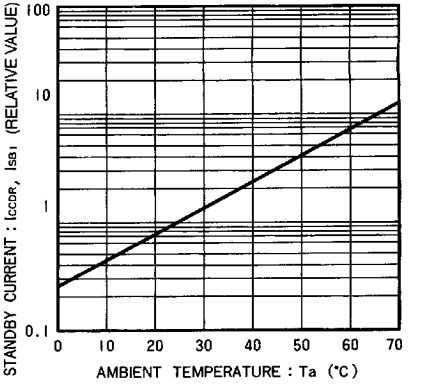


Figure 9

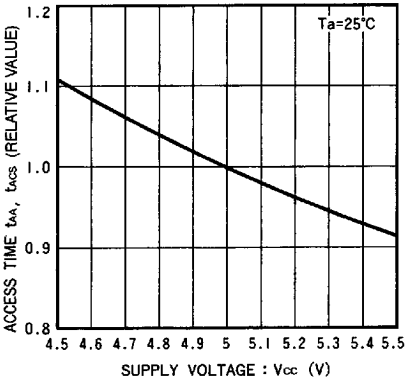


Figure 10

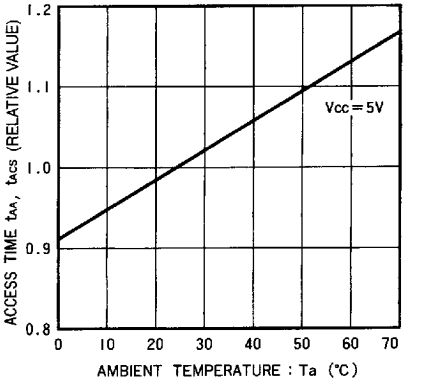


Figure 11

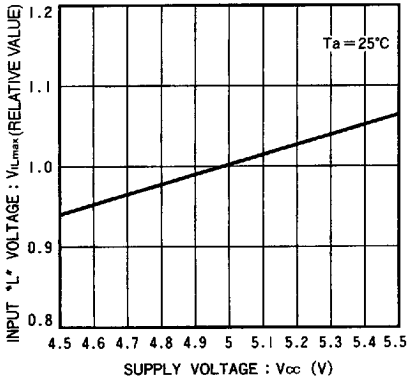


Figure 12

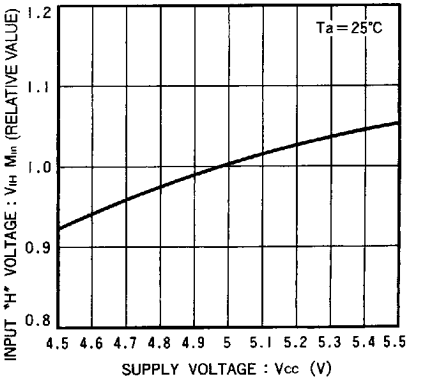


Figure 13

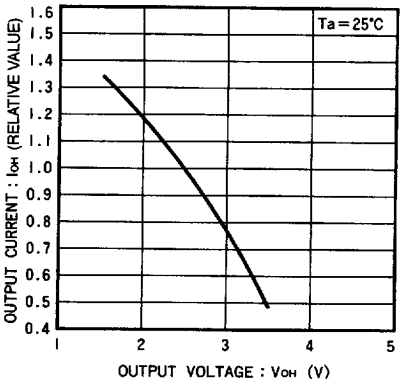


Figure 14

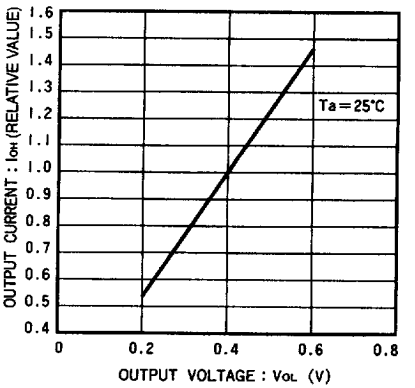


Figure 15