8,192 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 10 ns**
- **Low active power**
  - **— 935 mW**
- **Low Standby Power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

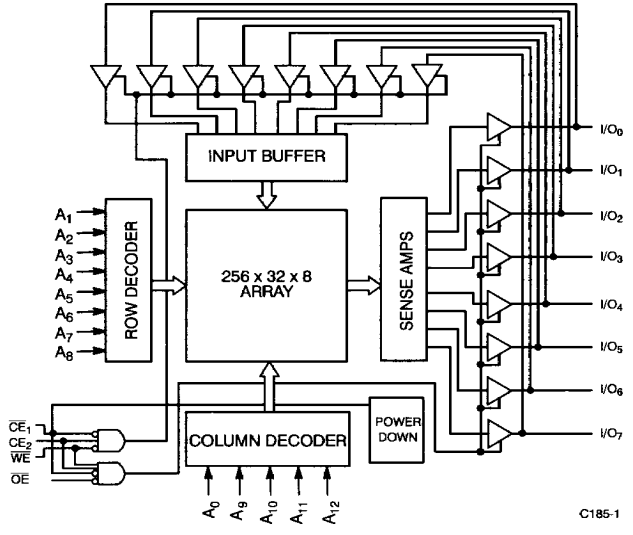
Functional Description

The CY7C185 and CY7C186 are high-performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by over 75% when deselected. The CY7C185 is in the space-saving 300-mil-wide DIP package and leadless chip carrier. The CY7C186 is in the standard 600-mil-wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

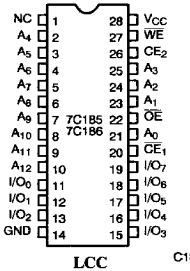
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to insure alpha immunity.

Logic Block Diagram

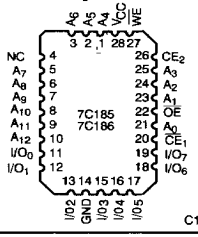


Pin Configurations

DIP/SOJ
Top View



LCC
Top View



Selection Guide[1]

	7C185–10	7C185–12	7C185–15	7C185–20 7C186–20	7C185–25 7C186–25	7C185–35 7C186–35	7C185–45 7C186–45	7C185–55 7C186–55
Maximum Access Time (ns)	20	25	35	20	25	35	45	55
Maximum Operating Current (mA)	170	170	160	120	100	100	100	80
Maximum Standby Current (mA)	40/20	40/20	40/20	20/20	20/20	20/20	20/20	20/20

Shaded areas contain advanced information.

Note:
1. For military specifications, see the CY7C185A/CY7C186A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C185–10		7C185–12		7C185–15		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		–3.0	0.8	–3.0	0.8	–3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–10	+10	–10	+10	–10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–10	+10	–10	+10	–10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–350		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		170		170		160	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		40		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V		20		20		20	mA

Shaded areas contain advanced information.

Electrical Characteristics Over the Operating Range (continued)

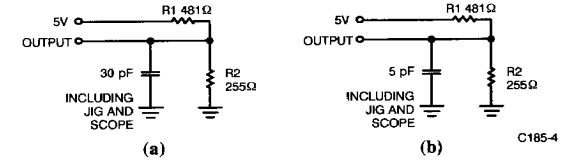
Parameters	Description	Test Conditions	7C185–20 7C186–20		7C185–25,35,45 7C186–25,35,45		7C185–55 7C186–55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		120		100		80	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%		20		20		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		20		20		20	mA

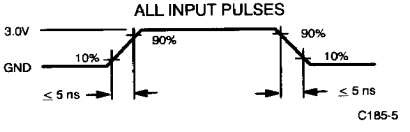
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

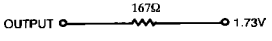
Notes:
2. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5]

Parameters	Description	7C185–10		7C185–12		7C185–15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		10		12		15	ns
t_{ACE2}	CE_2 HIGH to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		5		7		8	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[7]	2		3		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z	2		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[8, 9] CE_2 LOW to High Z		5		7		8	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		10		12		15	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		8		12		ns
t_{SCE2}	CE_2 HIGH to Write End	8		8		12		ns
t_{AW}	Address Set-Up to Write End	8		9		12		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		8		12		ns
t_{SD}	Data Set-Up to Write End	5		6		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8]		6		6		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		3		3		ns

Shaded areas contain advanced information.

Notes:

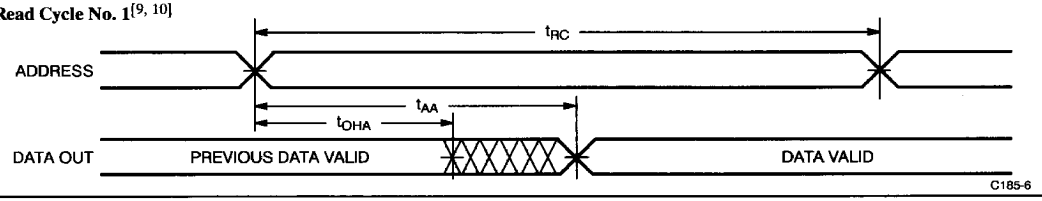
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[5] (continued)

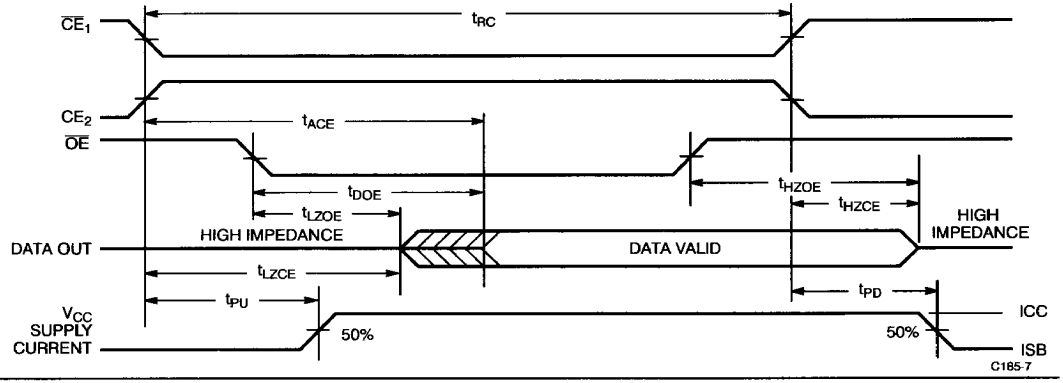
Parameters	Description	7C185–20 7C186–20		7C185–25 7C186–25		7C185–35 7C186–35		7C185–45 7C186–45		7C185–55 7C186–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		35		45		55		ns
t_{AA}	Address to Data Valid		20		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		20		25		35		45		55	ns
t_{ACE2}	CE_2 HIGH to Data Valid		20		25		25		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		8		10		12		15		20	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[7]	5		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[8, 9] CE_2 LOW to High Z		8		10		15		15		20	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	20		20		25		40		50		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	15		20		25		30		40		ns
t_{SCE2}	CE_2 HIGH to Write End	15		20		20		25		30		ns
t_{AW}	Address Set-Up to Write End	15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		20		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8]		7		7		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Switching Waveforms

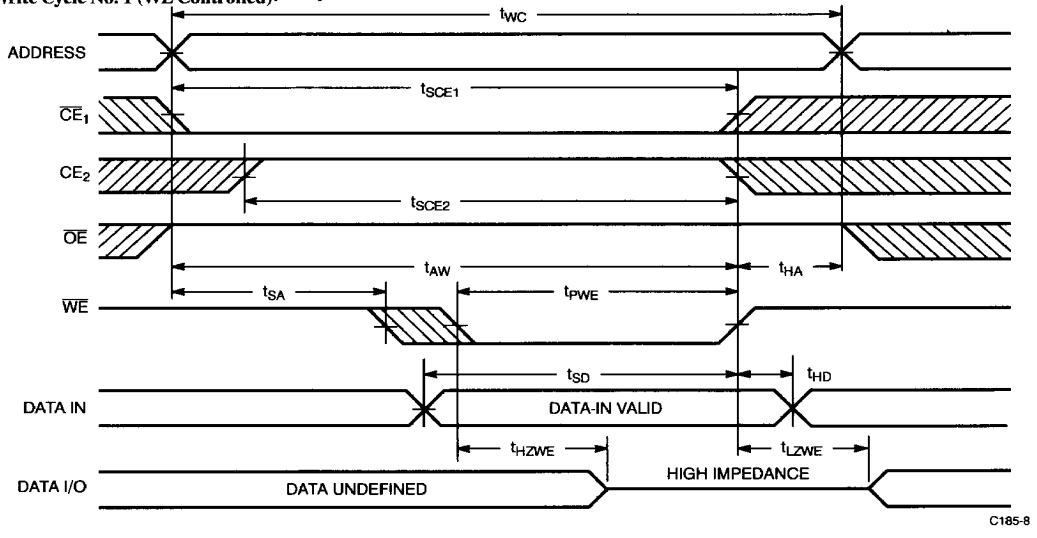
Read Cycle No. 1[9, 10]



Read Cycle No. 2[11, 12]



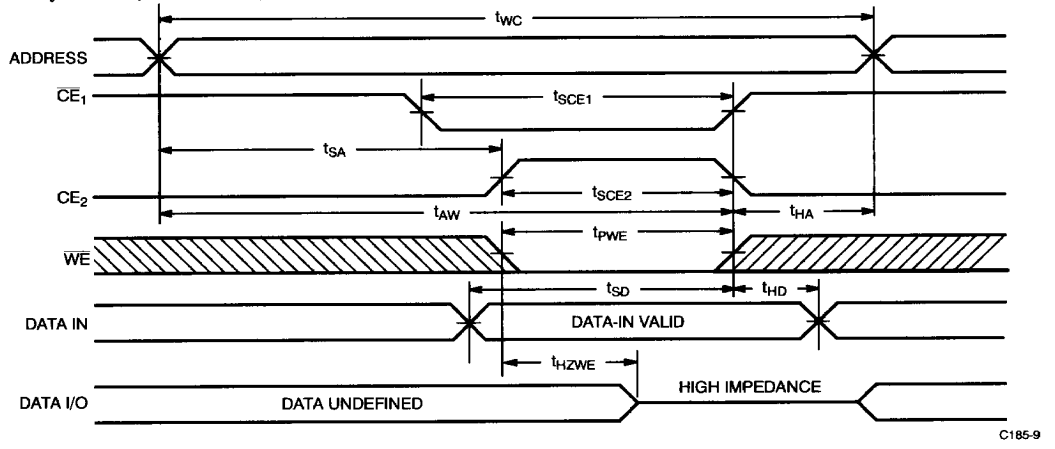
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10, 12]



Notes:
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. $\overline{WE}$ is HIGH for read cycle.
12. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

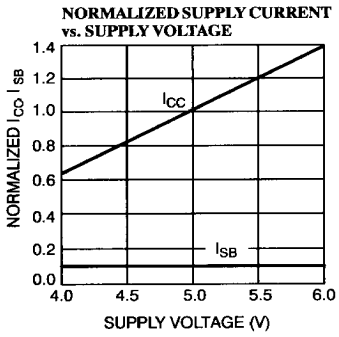
Switching Waveforms (continued)

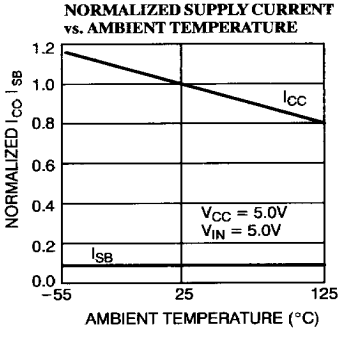
Write Cycle No. 2 ($\overline{CE}$ Controlled) [10, 12, 13]

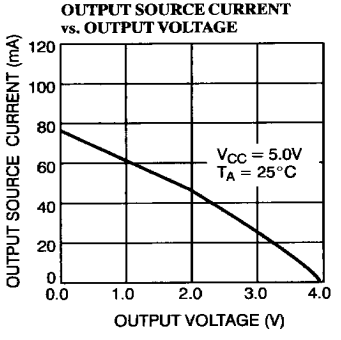


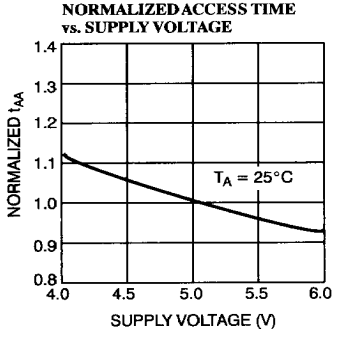
Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

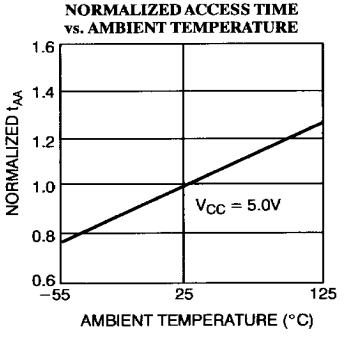
Typical DC and AC Characteristics

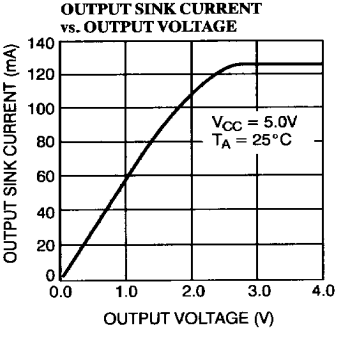






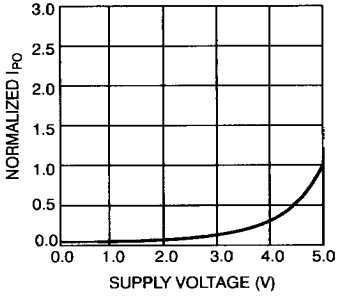




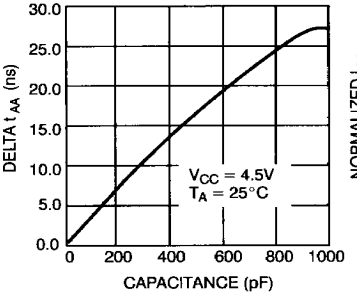


Typical DC and AC Characteristics (continued)

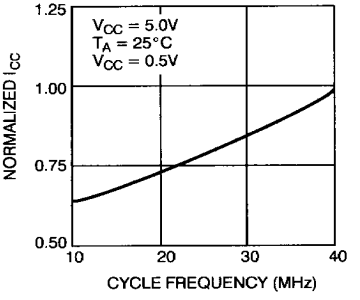
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C185–10DC	D22	Commercial
	CY7C185–10PC	P21	
	CY7C185–10VC	V21	
12	CY7C185–12DC	D22	Commercial
	CY7C185–12PC	P21	
	CY7C185–12VC	V21	
15	CY7C185–15DC	D22	Commercial
	CY7C185–15PC	P21	
	CY7C185–15VC	V21	
20	CY7C185–20DC	D22	Commercial
	CY7C185–20LC	L54	
	CY7C185–20PC	P21	
	CY7C185–20VC	V21	
25	CY7C185–25DC	D22	Commercial
	CY7C185–25LC	L54	
	CY7C185–25PC	P21	
	CY7C185–25VC	V21	
35	CY7C185–35DC	D22	Commercial
	CY7C185–35LC	L54	
	CY7C185–35PC	P21	
	CY7C185–35VC	V21	
45	CY7C185–45DC	D22	Commercial
	CY7C185–45LC	L54	
	CY7C185–45PC	P21	
	CY7C185–45VC	V21	
55	CY7C185–55DC	D22	Commercial
	CY7C185–55LC	L54	
	CY7C185–55PC	P21	
	CY7C185–55VC	V21	

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C186–20DC	D16	Commercial
	CY7C186–20PC	P15	
25	CY7C186–25DC	D16	Commercial
	CY7C186–25PC	P15	
35	CY7C186–35DC	D16	Commercial
	CY7C186–35PC	P15	
45	CY7C186–45DC	D16	Commercial
	CY7C186–45PC	P15	
55	CY7C186–55DC	D16	Commercial
	CY7C186–55PC	P15	

Shaded areas contain advanced information.

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