CYPRESS SEMICONDUCTOR

128K Write-Through Secondary Cache Module

Features

- **128-Kbyte direct-mapped, write-through, zero-wait-state secondary cache module**
- **Operates with 33-MHz Intel 486 processors**
- **Uses low-cost CMOS asynchronous SRAMs as cache data storage and cache tag storage**
- **Supports self-invalidation**
- **64-position dual-read-out SIMM with 128 leads**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

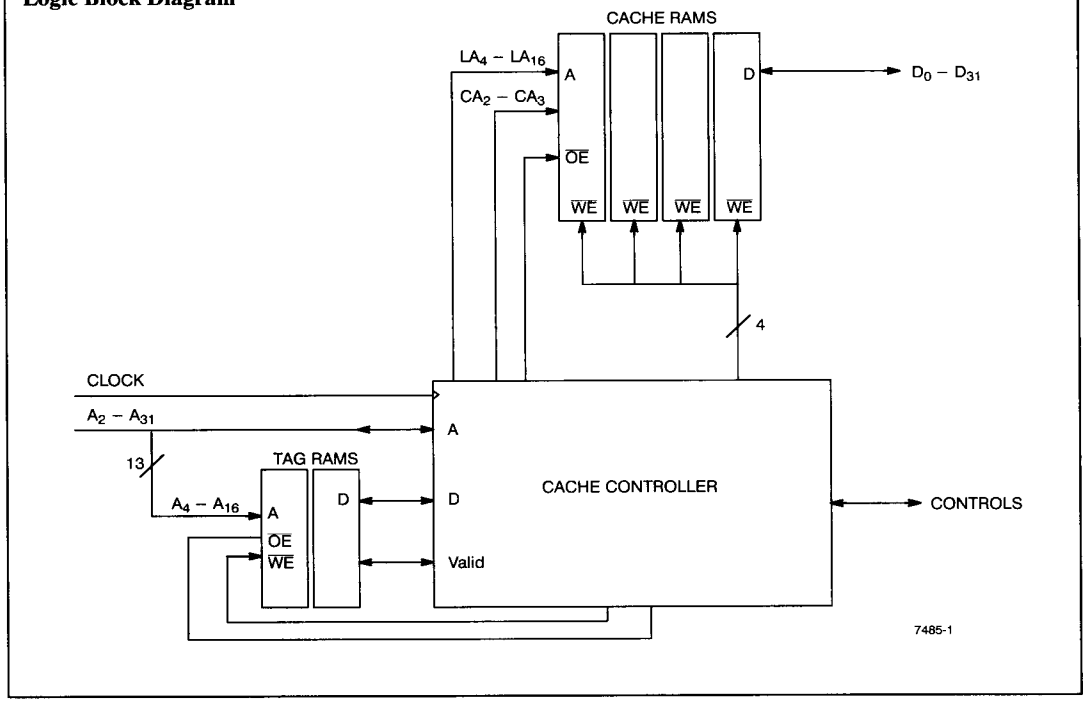
Functional Description

The CYM7485 is a self-contained 128-Kbyte direct-mapped, zero-wait-state, write-through secondary cache module designed for use in Intel 486-based systems. The line size is 16 bytes. Cache data is stored in four 32K by 8 asynchronous SRAMs, and the tag addresses are stored in two 8K by 8 asynchronous SRAMs.The address from the processor is captured by high-speed transparent latches at the beginning of each access and the lowest two address bits are incremented according to the Intel burst sequence during burst reads and cache line fills.

The on-board cache controller coordinates accesses to the cache memory. During a read hit, four 32-bit words are read from the cache RAMs and returned to the processor without wait states. If the read location requested by the processor is not found in the cache, the memory controller will hold the processor and retrieve the missing line from the main memory. During write cycles, the main memory is always updated with the data from the processor. If the write location is found in the cache, then the cache content is updated as well.

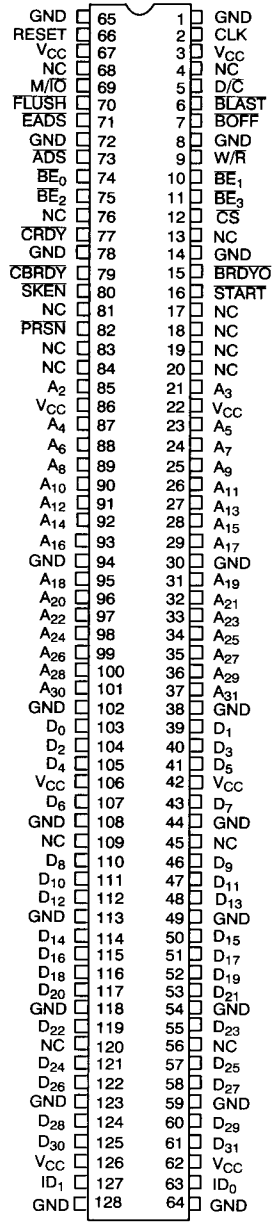
All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) board.The package dimensions are 3.85″ x 0.200″ x 1.5″. All inputs and outputs of the CYM7485 are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 5 micro-inches of gold flash.

Logic Block Diagram



Pin Configuration

SIMM
Top View



7485-2

Pin Descriptions

Symbol	Parameter	Type	Pins	Active	Description
CLK	Clock	I	1	N/A	This input is the timing reference for all module functions. It is the same as the i486 clock.
RESET	Reset the Cache	I	1	HIGH	RESET is sampled at each clock rise. If it is true, the cache logic will be placed in the idle state. RESET will not invalidate the cache contents.
$\overline{ADS}$	Address Strobe	I	1	LOW	$\overline{ADS}$ is connected to the $\overline{ADS}$ signal from the i486. It is used to start read or write cycles. $\overline{CS}$ must be asserted for $\overline{ADS}$ to be recognized.
M/$\overline{IO}$	Memory/IO	I	1	N/A	This signal is used by the i486 to distinguish between memory and IO accesses. The module will not cache IO accesses.
W/$\overline{R}$	Write/Read	I	1	N/A	A LOW indicates a read cycle. A HIGH indicates a write cycle.
D/$\overline{C}$	Data/Control	N/A	1	N/A	This signal is not used by the CYM7485.
$\overline{START}$	Memory Start	O	1	LOW	$\overline{START}$ is asserted during read miss and write cycles. It signals the main memory to service the current access.
$\overline{BRDYO}$	Burst Ready Out	O	1	LOW	This signal is asserted during read hits only. It indicates to the i486 that valid data from the cache is available. $\overline{BRDYO}$ is deasserted during other accesses.
$\overline{CBRDY}$	Cache Burst Ready In	I	1	LOW	This signal is asserted when burst data from the system is ready to be sampled by the i486 and the cache module.
$\overline{CRDY}$	Cache Ready In	I	1	LOW	This signal is asserted when non-burst data from the system is ready to be sampled by the i486 and the cache module.
$\overline{BLAST}$	Burst Last	I	1	LOW	$\overline{BLAST}$ is asserted by the i486 when the current cycle is the last cycle of a burst access.
$\overline{BOFF}$	Back-off	I	1	LOW	$\overline{BOFF}$ is sampled at each clock rise except the rising edge of T1 in a i486 access. If $\overline{BOFF}$ is asserted, the cache module will place its data lines in a three-stated condition. In addition, $\overline{START}$ and $\overline{BRDYO}$ will be deasserted.
$\overline{PRSN}$	Presence	O	1	LOW	This signal is tied to ground. It indicates to the system that the cache module is present.
$A_2 - A_{31}$	Address Lines	I	30	N/A	Address inputs to the CYM7485.
$\overline{BE_0} - \overline{BE_3}$	Byte Enables	I	4	LOW	These signals are used during write cycles to determine which byte(s) will be written.
$\overline{CS}$	Chip Select	I	1	LOW	For normal accesses, $\overline{CS}$ must be LOW before $\overline{ADS}$ or $\overline{EADS}$ can be recognized. If $\overline{CS}$ is HIGH and $\overline{ADS}$ is LOW, the cache line selected by the address on $A_2 - A_{31}$ will be invalidated.
$D_0 - D_{31}$	Data Lines	I/O	32	N/A	Data lines to/from the i486, main memory, and other system components. $D_0 - D_7$ is the low byte.
$\overline{SKEN}$	System Cache Enable	I	1	LOW	This signal is generated by the system to inform the i486 and the cache module that the current line is cachable. During a cache line fill, $\overline{SKEN}$ is sampled one clock cycle before the first word is returned and one clock cycle before the last word of the line is returned.
$\overline{FLUSH}$	Cache Flush	I	1	LOW	If $\overline{FLUSH}$ is LOW and $\overline{ADS}$ is LOW, then the cache line selected by the address on $A_2 - A_{31}$ will be invalidated.
$\overline{EADS}$	Valid External Address	I	1	LOW	If $\overline{EADS}$ is asserted together with $\overline{CS}$, then the cache line selected by the address on $A_2 - A_{31}$ will be invalidated if a match is found.
$ID_0 - ID_1$	Cache Size Selector	O	2	N/A	These two lines are not connected on the cache module. They are tied externally to V_{CC} to select a cache size of 128K bytes.

Basic Operation

The CYM7485 is a complete 128-Kbyte, direct-mapped secondary cache subsystem designed to work with 33-MHz Intel 486 processors. The cache memory is divided into 8K 16-byte lines and each line is assigned a dedicated entry in the cache tag RAM. The CYM7485 supports zero-wait-state operations: it can return four words from its cache memory in five clock cycles (i.e., 2-1-1-1). A write-through cache policy is implemented to provide data integrity.

Four 32K by 8 asynchronous SRAMs provide the 128-Kbyte cache storage and two 8K by 8 asynchronous SRAMs store the 8K 16-bit tag entries. Each tag entry is divided into a 15-bit tag field (to support the 4-Gbyte processor address space) and a valid bit. During an access, the contents of the tag entry selected by processor address bits, A_4 – A_{16}, are delivered to two 8-bit comparators where they are matched against the 15 upper order address bits from the i486. A match is declared only if the two set of addresses are identical and the valid bit of the tag entry is set.

Addresses from the processor are captured by transparent latches before they are delivered to the cache memory. The lowest two address bits (A_2 and A_3) are incremented by the cache controller according to the Intel burst order during read hits and line fills (see *Table 1*).

The following functions are not supported in the CYM7485: data parity (DP_0 - DP_3), write protect ($\overline{WP}$), write protect strap ($\overline{WPSTRAP}$), cache enable to CPU ($\overline{CKEN}$), software flushes, and global cache invalidation.

Read Cycles

A read cycle is initiated when $\overline{ADS}$, $\overline{CS}$, and W/$\overline{R}$ are sampled LOW at clock rise with M/$\overline{IO}$ sampled HIGH. The processor address is captured by a set of transparent latches as soon as the access is started. The latch will remain closed until the access is completed or until $\overline{BOFF}$ is asserted (LOW). $\overline{BE_0}$ – $\overline{BE_3}$ are ignored in all read accesses.

Tag look-up begins whenever a valid processor address is available. Processor address lines are connected to the two tag RAMs directly to reduce the tag match delay. If the requested location is found in the cache, the CYM7485 will return the first burst word in the first T2 cycle. This is followed by three more words delivered once every clock until the last word is returned or until $\overline{BLAST}$ is asserted. $\overline{START}$ is pulled HIGH in T2 to signal a cache hit to main memory and $\overline{BRDYO}$ is pulled LOW in T2 to signal the processor that valid data is available from the cache. $\overline{BRDYO}$ remains LOW until the last word is returned.

If the requested location is not in the cache, then the cache controller will assert $\overline{START}$ (LOW) to initiate the main memory access and deassert $\overline{BRDYO}$ (HIGH) to hold the processor.The CYM7485 cannot accept data from main memory in zero wait states.The earliest cycle in which main memory data is accepted is the second clock cycle after $\overline{START}$ is asserted. The minimum cache line fill sequence from main memory is 4/3/3/3.

$\overline{BLAST}$ is sampled concurrently with $\overline{CBRDY}$ and $\overline{CRDY}$. If $\overline{BLAST}$ is sampled LOW before the fourth data transfer, then the line fill operation is aborted. Data from main memory is considered cachable if $\overline{SKEN}$ is sampled LOW at least one clock cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is first asserted (LOW). If this condition is satisfied, the data returned from main memory will be written into the cache each time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW. If $\overline{SKEN}$ is sampled HIGH when the first $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW, or if $\overline{SKEN}$ is sampled LOW concurrently with the first $\overline{CBRDY}$ or $\overline{CRDY}$, then the data is considered to be non-cachable and the cache module will not act on the information.

$\overline{SKEN}$ is sampled again at the end of the line fill to validate the cache line. If $\overline{SKEN}$ is sampled LOW one cycle before the fourth time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW, then the cache line will be validated.

In order to process the read miss line fill correctly, A_4–A_{31} from the processor must remain stable throughout the line fill. Otherwise, the cache tag will not be updated properly. In addition, $\overline{SKEN}$ must be LOW t_{14} before the end of T2 and remain LOW until the line fill is completed.

If the read access is not cachable, then $\overline{SKEN}$ will be sampled HIGH after T2. The CYM7485 supports the following types of non-cachable read accesses. If a single read hit is detected, then the data word will be returned with $\overline{BRDYO}$ asserted. If a single read miss is found, $\overline{START}$ will be asserted to begin the main memory access. However, the data returned will not be stored into the cache memory and the selected cache line is not validated. If a burst read hit is detected, the cache module will treat it in the same manner as a cachable burst read hit (i.e., four words will be retrieved from the cache memory with $\overline{BRDYO}$ asserted). On the other hand, if a burst read miss is found, then $\overline{START}$ will be asserted to begin the main memory access. However, the four words returned by the main memory will not be stored into the cache and the selected cache line is not invalidated. *Table 2* illustrates the various cachable/non-cachable and single/burst access combinations.

Table 1. Intel Burst Sequence

First Address	Second Address	Third Address	Fourth Address
0	4	8	C
4	0	C	8
8	C	0	4
C	8	4	0

Table 2. Cachable/Non-cachable and Single/Burst Read Access Combinations

SKEN	BLAST at end of T2	Hit / Miss	Action
0	0	Read hit	Cachable single read access. Cache module will return the word from its memory, assert BRDYO, and then return to the idle state.
0	1	Read hit	Cachable burst access. This is the normal read hit case. Cache module will return 4 words from its memory with BRDYO asserted. Less than 4 words will be returned if BLAST is asserted before the end of the burst sequence.
1	0	Read hit	Non-cachable single read access. Cache module will return the word from its memory, assert BRDYO, and return to the idle state.
1	1	Read hit	Non-cachable burst access. The cache module will process this access like a normal burst read hit. The 4 words in the line will be returned with BRDYO asserted. Less than 4 words will be returned if BLAST is asserted before the end of the burst sequence.
0	0	Read miss	Cachable single read access. Cache module will assert START and wait for CBRDY or CRDY to complete the cycle. The selected cache line is invalidated.
0	1	Read miss	Cachable burst read access. This is the normal read miss case. The cache module will assert START and wait for the 4 words to return from main memory accompanied by CBRDY or CRDY. The words will be written into the cache memory and the cache line will be validated when the fourth word is returned (because SKEN is LOW). If BLAST is asserted before the fourth word is returned, the line fill is aborted and the selected cache line will remain invalidated.
1	0	Read miss	Non-cachable single read access. The cache module will assert START and wait for CBRDY or CRDY to complete the cycle. The word returned from main memory will not be stored into the cache memory and the valid bit of the selected cache line is not changed.
1	1	Read miss	Non-cachable burst read access. The cache module will process this access like a normal cachable burst read miss. START will be asserted but the 4 words returned from main memory not will be stored into the cache. In addition, the valid bit of the selected cache entry is not changed.

Write Cycles

A write cycle is initiated when ADS and CS are sampled LOW at clock rise with W/R and M/IO sampled HIGH. The address from the processor is latched for two clock cycles to allow cache RAM update in case of a write hit. The latch then reopens to accept new addresses.

Tag look-up begins as soon as a valid processor address is available. If the location specified by the processor is found in the cache, the cache RAMs are updated with the data from the processor immediately. Byte enable signals BE0 – BE3 are used to determine which bytes in the 32-bit words are to be modified. If the location is not found in the cache, the cache RAMs are not modified.

Because the CYM7485 implements the write-through cache policy, write data from the processor is always written into the main memory regardless of cache hits or cache misses. In every write cycle, START is asserted (LOW) in T2 to trigger the main memory write operation.This signal will remain LOW until the system indicates write completion by asserting (LOW) CBRDY or CRDY. BRDYO is kept HIGH throughout the write cycle. The minimum write cycle contains one wait state (i.e., three clocks in the cycle) and the minimum data-hold time is 6 ns.

All write cycles require one wait state.

Invalidations

Individual tag invalidation is supported in the CYM7485. If EADS, CS, and W/R are sampled LOW and M/IO is sampled HIGH at clock rise, then the tag entry selected by the processor address is invalidated if a tag match is detected. In other words, memory read cycles never cause invalidation. The address must be stable a minimum of 14 ns before the clock edge at which EADS is sampled LOW.

The CYM7485 will recognize invalidation requests under two conditions only:

1. Self invalidation during a write cycle (initiated by asserting ADS). The earliest time at which EADS can be asserted is the third clock rise after the one clock cycle in which ADS is sampled LOW. For each invalidation, the address to be invalidated must be stable for two full clock cycles after EADS is asserted. CBRDY or CRDY can be asserted as early as the second clock rise after the one in which EADS is asserted to complete the write cycle. The CYM7485 can support consecutive EADS invalidations once every three clock cycles before CBRDY or CRDY is returned. For consecutive write cycles with self-invalidation, the CYM7485 can support one such operation every six clock cycles (see Self-Invalidation Timing Diagram).
2. When the cache module is in the "back-off" state (BOFF is asserted).The cache module can be placed in the "back-off" state by asserting BOFF in all normal access cycles except in T1. Once in the "back-off" state, the module can accept consecutive invalidations via CS and EADS once every three clock cycles. The earliest time CS and EADS can be asserted is the clock rise after the one in which BOFF is asserted. For each invalidation, the address to be invalidated has to remain stable for two full clock cycles after the EADS signal is asserted.

Flush

The CYM7485 cannot support global cache flushes where the entire cache is invalidated by the assertion of the $\overline{\text{FLUSH}}$ input. To flush the cache in the CYM7485, the processor has to

1. Assert $\overline{\text{FLUSH}}$ and $\overline{\text{ADS}}$ at clock rise (i.e., $\overline{\text{FLUSH}}$=LOW and $\overline{\text{ADS}}$=LOW) with M/$\overline{\text{IO}}$ set to HIGH, or assert $\overline{\text{ADS}}$ and deassert $\overline{\text{CS}}$ at clock rise (i.e., $\overline{\text{ADS}}$=LOW and $\overline{\text{CS}}$=HIGH) with M/$\overline{\text{IO}}$ set to HIGH. Note that $\overline{\text{CS}}$, $\overline{\text{ADS}}$, and M/$\overline{\text{IO}}$ must satisfy the set-up time requirements (i.e., t8, t6, and t6 respectively).
2. Access (read or write) the 8K locations in the cache tag.

During each access, the cache module will invalidate the cache entry selected by the address lines. The CYM7485 can accept new flush accesses no faster than once every three clock cycles (see the Flush Timing Diagrams). $\overline{\text{START}}$ and $\overline{\text{BRDY0}}$ will remain deasserted (HIGH) during flush cycles. $\overline{\text{CBRDY}}$ and $\overline{\text{CRDY}}$ are not required to complete the flush cycle.

Back-Off

A cache back-off can be initiated by the assertion of the $\overline{\text{BOFF}}$ in any normal access cycles except in T1 where the $\overline{\text{BOFF}}$ signal is ignored. Once $\overline{\text{BOFF}}$ is sampled LOW at clock rise, the data lines will be placed in a three-stated condition in the same clock cycle. In addition, both $\overline{\text{START}}$ and $\overline{\text{BRDYO}}$ will be pulled HIGH. When $\overline{\text{BOFF}}$ is asserted, the cache module will ignore all cache cycles except RESET, invalidation via $\overline{\text{CS}}$, $\overline{\text{EADS}}$, and M/$\overline{\text{IO}}$, and flush operations via $\overline{\text{FLUSH}}$, $\overline{\text{CS}}$, $\overline{\text{ADS}}$, and M/$\overline{\text{IO}}$.

Reset

If RESET is sampled HIGH at clock rise, the cache controller will enter the idle state and all module outputs will be deasserted. The cache contents, however, are not invalidated. Refer to the Flush section for information on cache invalidation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7485−33		Unit
			Min.	Max.	
V_{OHD}	Output HIGH Voltage (Data)	V_{CC}=Min., I_{OH}=−4.0 mA	2.4		V
V_{OLD}	Output LOW Voltage (Data)	V_{CC}=Min., I_{OL}=8.0 mA		0.4	V
V_{OHC}	Output HIGH Voltage (Control)	V_{CC}=Min., I_{OH}=−3.2 mA	2.4		V
V_{OLC}	Output LOW Voltage (Control)	V_{CC}=Min., I_{OL}=16 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}, V_{CC}=Max.	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA

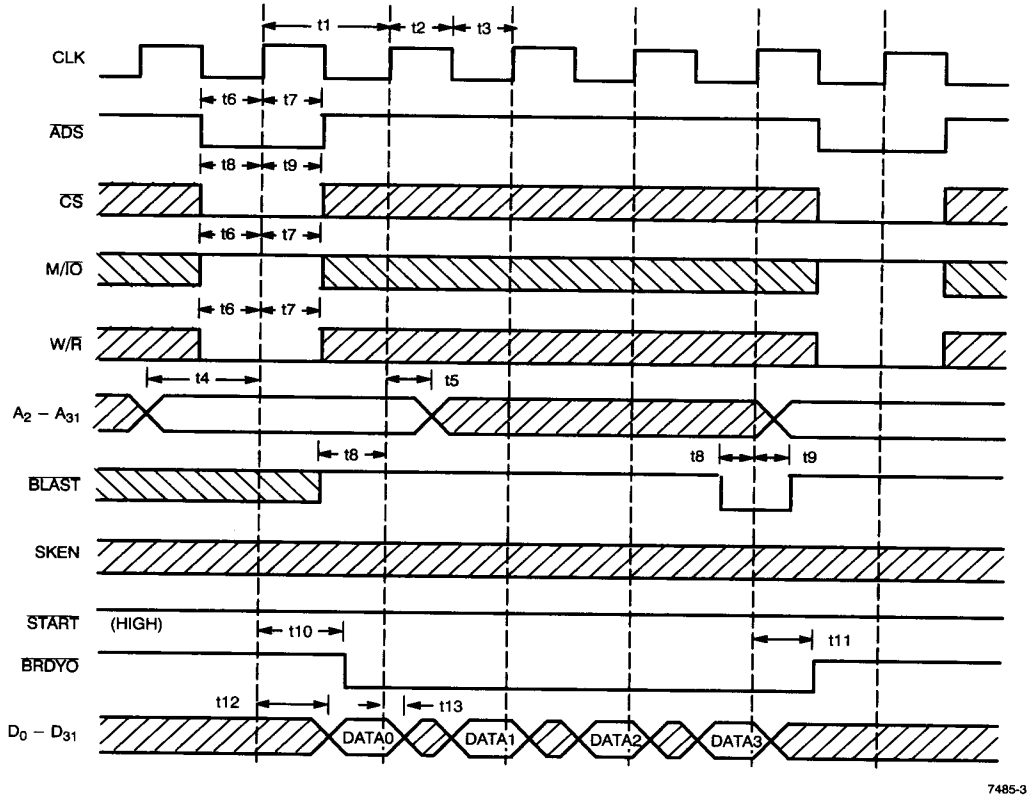
AC Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0° to 70°C, loading on $D_0 - D_{31}$ = 75 pF, loading on all other outputs = 50 pF)

Symbol	Parameter	Min.	Max.	Unit
t1	Clock Period	30		ns
t2	Clock HIGH Time	11		ns
t3	Clock LOW Time	11		ns
t4	$A_2 - A_{31}$, $\overline{BE}_0 - \overline{BE}_3$ Set-Up Before Clock Rise	14		ns
t5	$A_2 - A_{31}$, $\overline{BE}_0 - \overline{BE}_3$ Hold After Clock Rise	3		ns
t6	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Set-Up Before Clock Rise	14		ns
t7	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Hold After Clock Rise	3		ns
t8	$\overline{CS}$, $\overline{BLAST}$ Set-Up Before Clock Rise	9		ns
t9	$\overline{CS}$, $\overline{BLAST}$ Hold After Clock Rise	3		ns
t10	$\overline{BRDYO}$ Valid After Clock Rise		17	ns
t11	$\overline{BRDYO}$ Hold After Clock Rise	3		ns
t12	$D_0 - D_{31}$ Valid After Clock Rise During Read Hit		24	ns
t13	$D_0 - D_{31}$ Hold After Clock Rise	3		ns
t14	$\overline{SKEN}$ Set-Up Before Clock Rise	9		ns
t15	$\overline{SKEN}$ Hold After Clock Rise	3		ns
t16	$\overline{START}$ Valid After Clock Rise		17	ns
t17	$\overline{START}$ Hold After Clock Rise	3		ns
t18	$D_0 - D_{31}$ Set-Up Before Clock Rise During Line Fill	10		ns
t19	$D_0 - D_{31}$ Hold After Clock Rise During Line Fill	15		ns
t20	$\overline{CBRDY}$, $\overline{CRDY}$ Set-Up Before Clock Rise	14		ns
t21	$\overline{CBRDY}$, $\overline{CRDY}$ Hold After Clock Rise	3		ns
t22	$D_0 - D_{31}$ Set-Up Before Clock Rise During Processor Write Cycle	0		ns
t23	$D_0 - D_{31}$ Hold After Clock Rise During Processor Write Cycle	6		ns
t24	$\overline{EADS}$ Set-Up Before Clock Rise	9		ns
t25	$\overline{EADS}$ Hold After Clock Rise	3		ns
t26	$\overline{BOFF}$ Set-Up Before Clock Rise	9		ns
t27	$\overline{BOFF}$ Hold After Clock Rise	3		ns
t28	$\overline{START}$ Go HIGH After Clock Rise During $\overline{BOFF}$ or RESET		18	ns
t29	$\overline{BRDYO}$ Go HIGH After Clock Rise During $\overline{BOFF}$ or RESET		18	ns
t30	D_0-D_{31} High Z During $\overline{BOFF}$		18	ns
t31	RESET Set-Up Before Clock Rise	9		ns
t32	RESET Hold After Clock Rise	3		ns
t33	RESET Duration	2 t2 + 12		ns
t34	$\overline{FLUSH}$ Set-Up Before Clock Rise	9		ns
t35	$\overline{FLUSH}$ Hold After Clock Rise	3		ns

Switching Waveforms

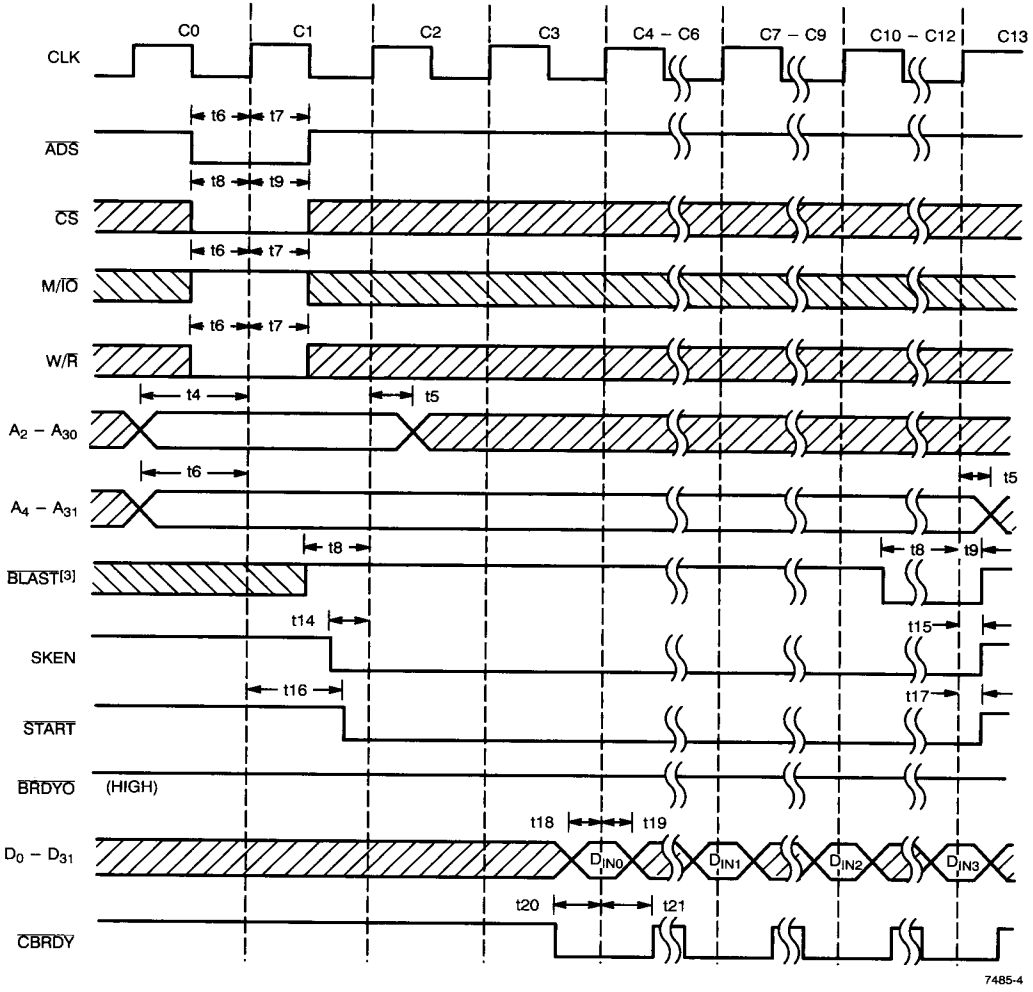
Read Hit[1]



Note:
1. Reset is LOW, $\overline{EADS}$ is HIGH, and $\overline{BOFF}$ is HIGH.

Switching Waveforms (continued)

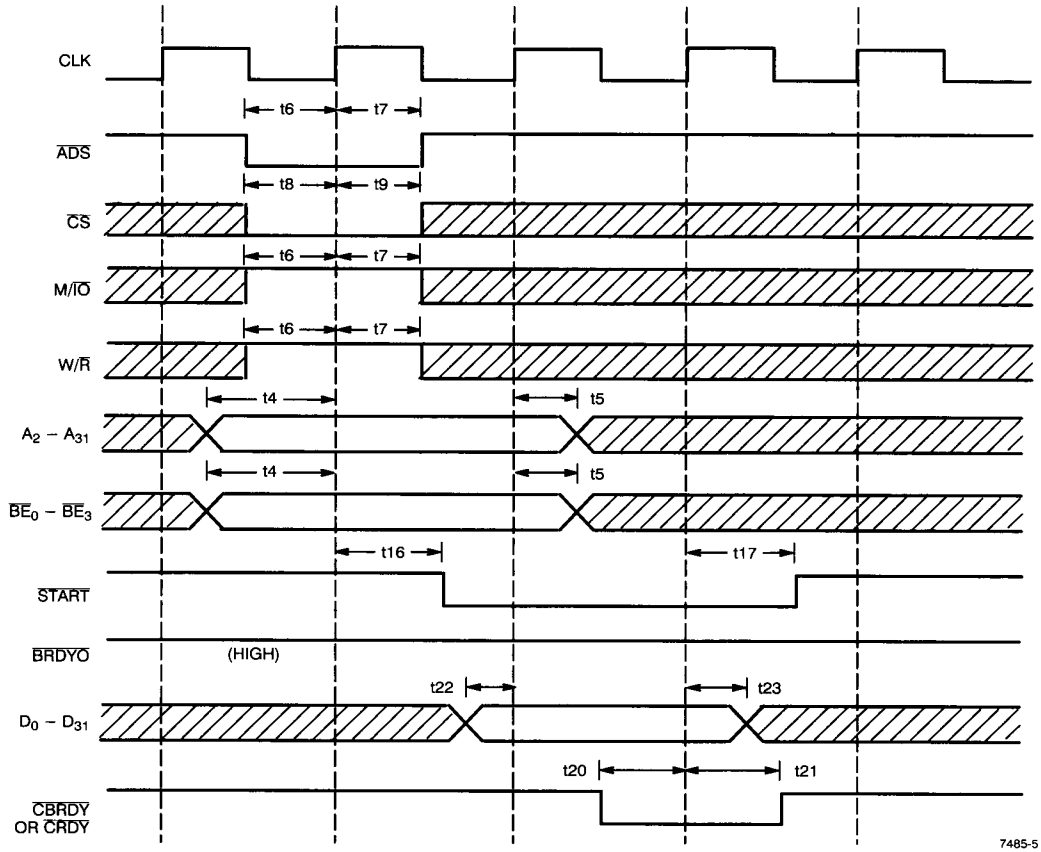
Read Miss, Line Fill (Min. DRAM Access is 4/3/3/3)[2]



Notes:
2. Reset is LOW, $\overline{EADS}$ is HIGH, $\overline{BOFF}$ is HIGH, and $\overline{CRDY}$ is HIGH.
3. $\overline{BLAST}$ is LOW t8 before the rising edge of clock period C11.

Switching Waveforms (continued)

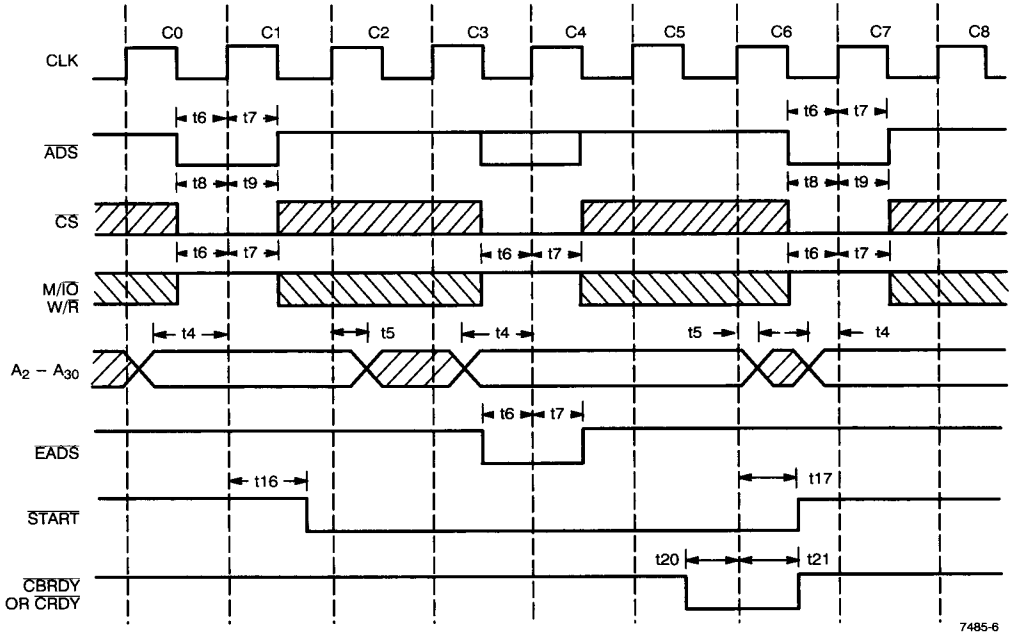
Write Cycle[4]



Note:
4. Reset is LOW, $\overline{\text{CBRDY}}$ is HIGH, $\overline{\text{EADS}}$ is HIGH, $\overline{\text{BOFF}}$ is HIGH. Access to DRAM must be a minimum of 3 cycles.

Switching Waveforms (continued)

Write Cycle with Self-Invalidation[5]

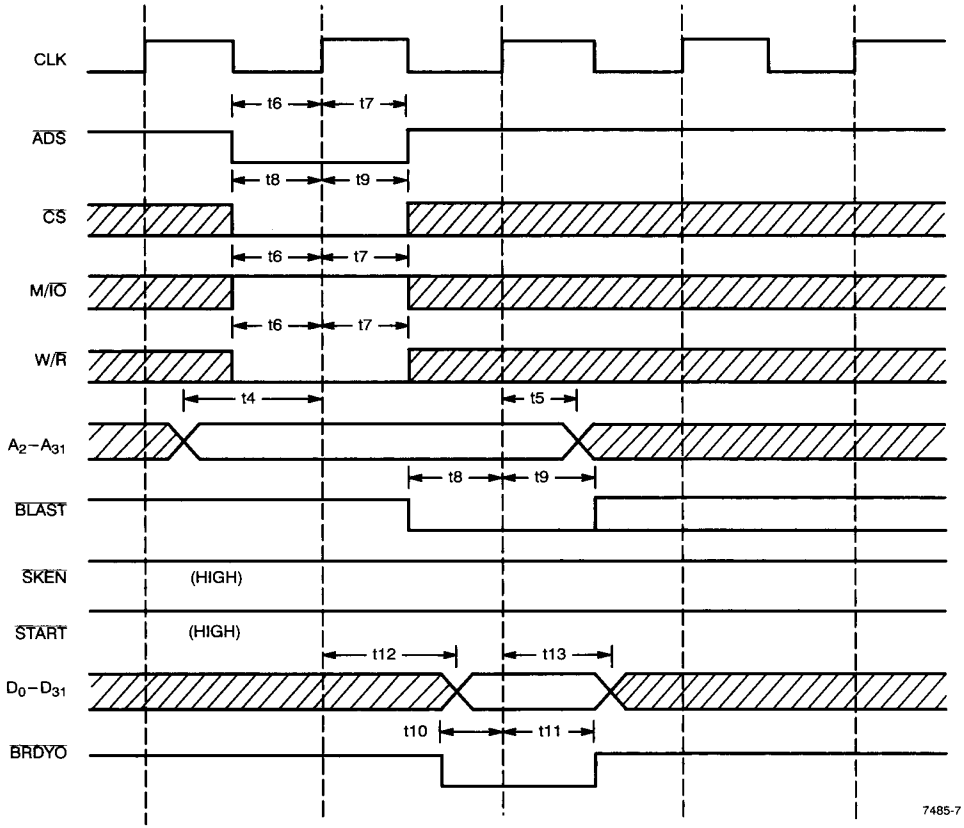


Note:

5. Reset is LOW. There is a minimum of 3 clocks between $\overline{ADS}$ and $\overline{EADS}$, a minimum of two clocks between $\overline{EADS}$ and $\overline{CBRDY}$ or $\overline{CRDY}$, a minimum of three clocks between consecutive $\overline{EADS}$ inside the same write cycle, and a minimum of 6 clocks between consecutive $\overline{ADS}$s.

Switching Waveforms (continued)

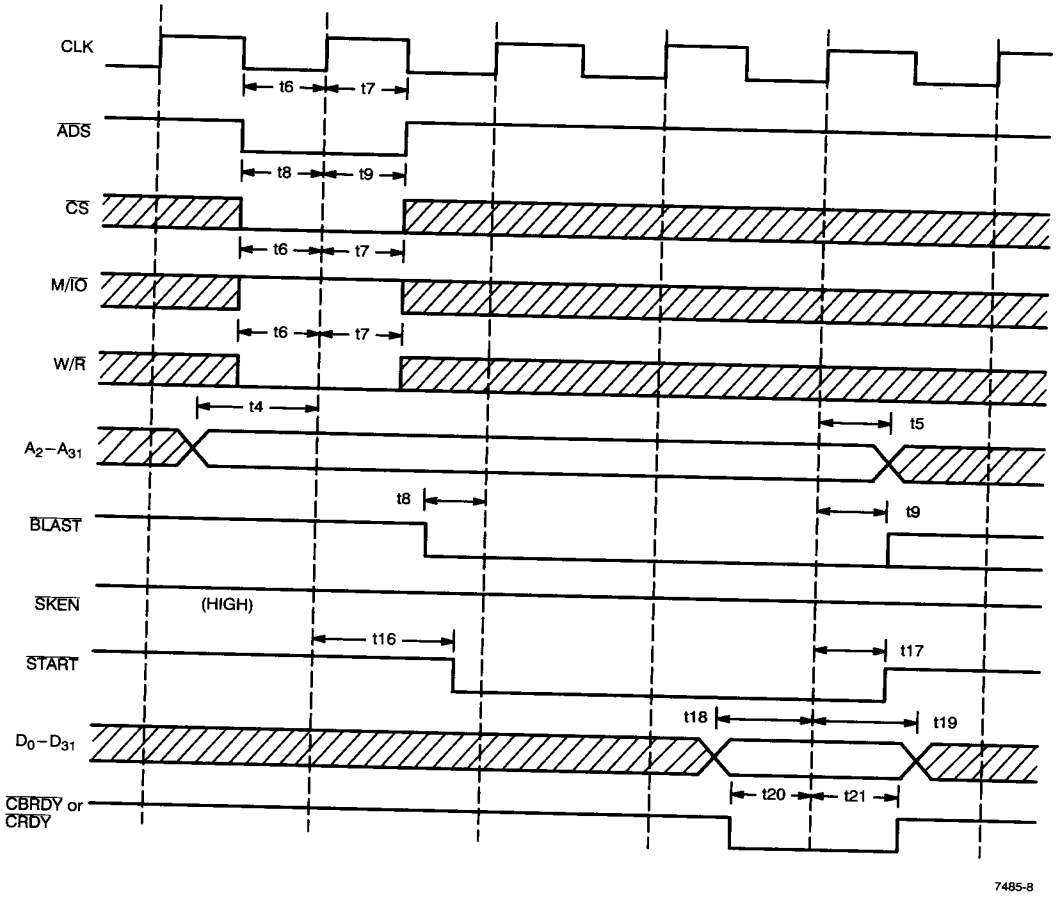
Single Non-Cachable Read (Cache Hit) [6]



Note:
6. Reset is LOW.

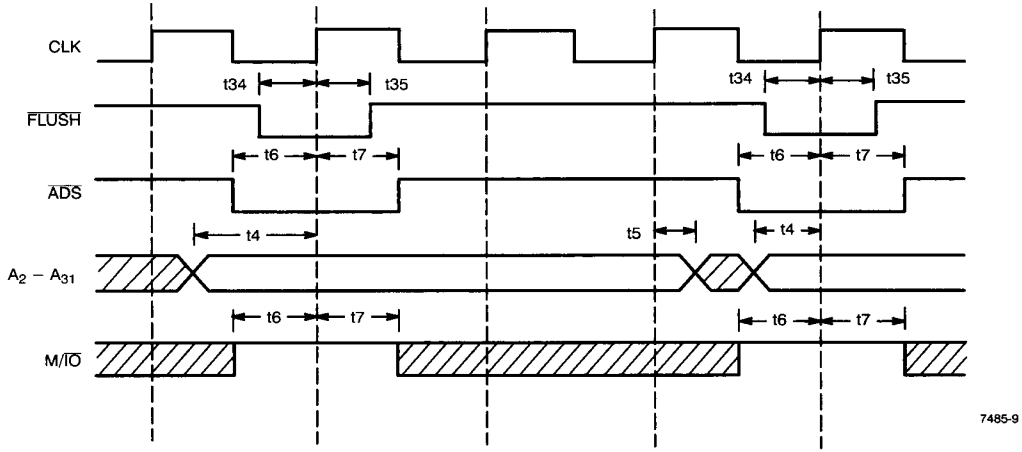
Switching Waveforms (continued)

Single Non-cachable Read (Cache Miss) Showing a Four-Clock Main Memory Access

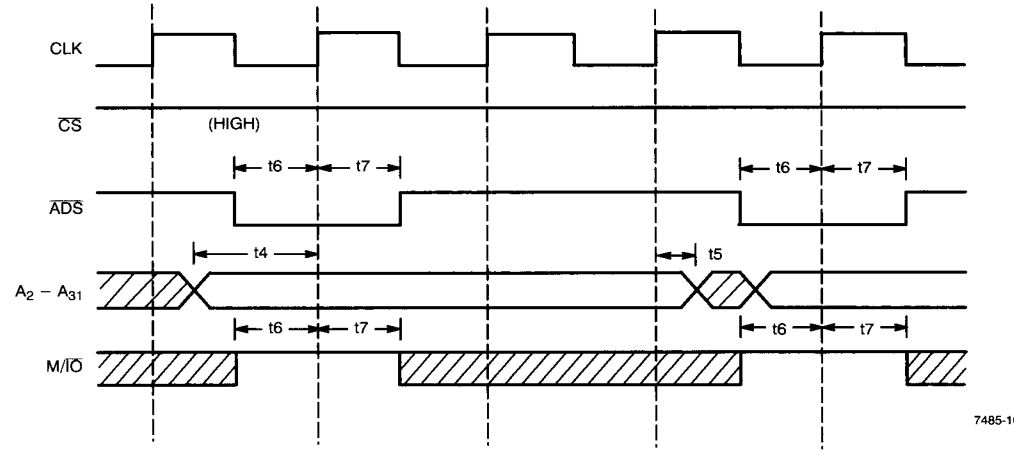


Switching Waveforms (continued)

Flush Cycle 1[7, 8]



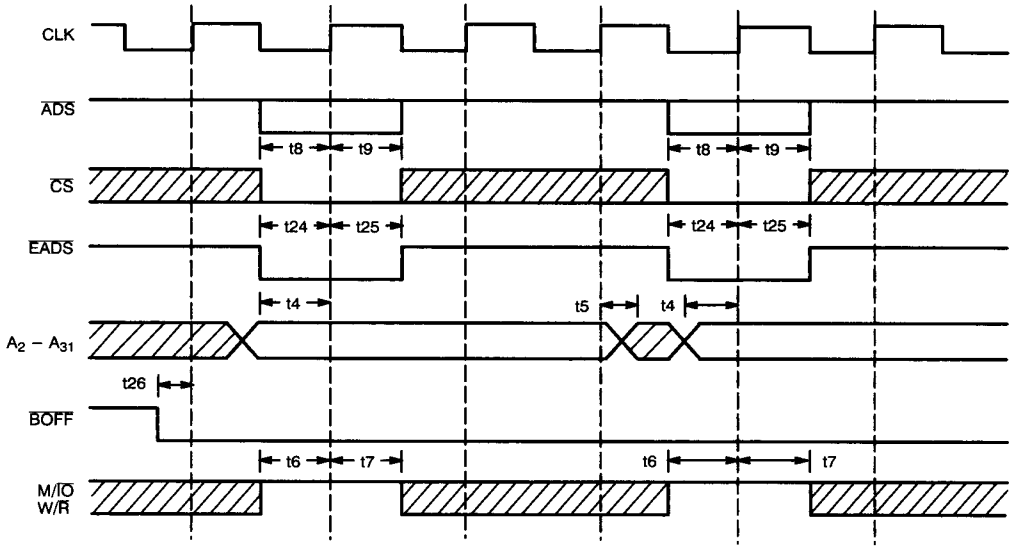
Flush Cycle 2[8, 9]



Notes:
7. Controlled by FLUSH, ADS, and M/IO; CS is a don't care.
8. A minimum of three clocks between consecutive ADS signals is required during Flush cycles. Reset is LOW.
9. Controlled by CS, ADS, and M/IO; FLUSH is a don't care.

Switching Waveforms (continued)

Consecutive Invalidations During $\overline{BOFF}$[10]

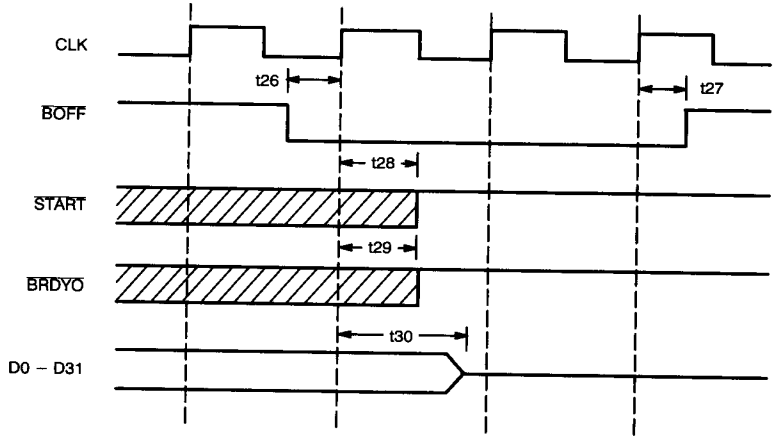


7485-11

Note:
10. Reset is LOW. There is a minimum of three clocks between $\overline{EADS}$, and a minimum of one clock between $\overline{BOFF}$ and $\overline{EADS}$.

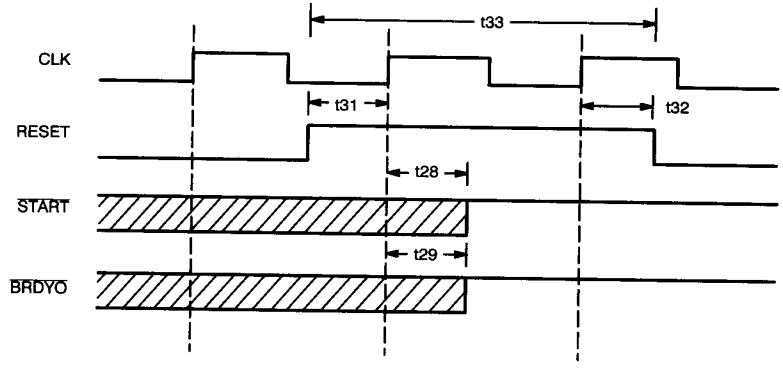
Switching Waveforms (continued)

Backoff Operation[11]



7485-12

Reset Operation



7485-13

Note:
11. Reset is LOW.

Ordering Information

Operating Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
33	CYM7485ZPM–33C	PM08	128-Pin Dual-Readout SIMM	Commercial

Document #: 38-M-00058–A