EM773

Energy metering IC; up to 32 kB flash and 8 kB SRAM

Rev. 1 — 1 September 2010 Objective data sheet

1. General description

The EM773 is an ARM Cortex-M0 based, low-cost 32-bit energy metering IC, designed for 8/16-bit smart metering applications. The EM773 offers programmability and on-chip metrology functionality combined with a low power, simple instruction set and memory addressing with reduced code size compared to existing 8/16-bit architectures.

The EM773 operates at CPU frequencies of up to 48 MHz.

The peripheral complement of the EM773 includes up to 32 kB of flash memory, up to 8 kB of data memory, one Fast-mode Plus I^{2}C-bus interface, one RS-485/EIA-485 UART, one SPI interface with SSP features, three general purpose counter/timers, up to 25 general purpose I/O pins, and a metrology engine for energy measurement.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 48 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - 32 kB on-chip flash programming memory.
  - 8 kB SRAM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- Digital peripherals:
  - Up to 25 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver (20 mA) on one pin.
  - High-current sink drivers (20 mA) on two I^{2}C-bus pins in Fast-mode Plus.
  - Three general purpose counter/timers with a total of two capture inputs and 10 match outputs.
  - Programmable WatchDog Timer (WDT).
- Analog peripherals:
  - Metrology Engine for Smart Metering with two current inputs and a voltage input.

- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - One SPI controller with SSP features and with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Available as 33-pin HVQFN package.

3. Applications

- Smart Metering

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
EM773FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a

5. Block diagram

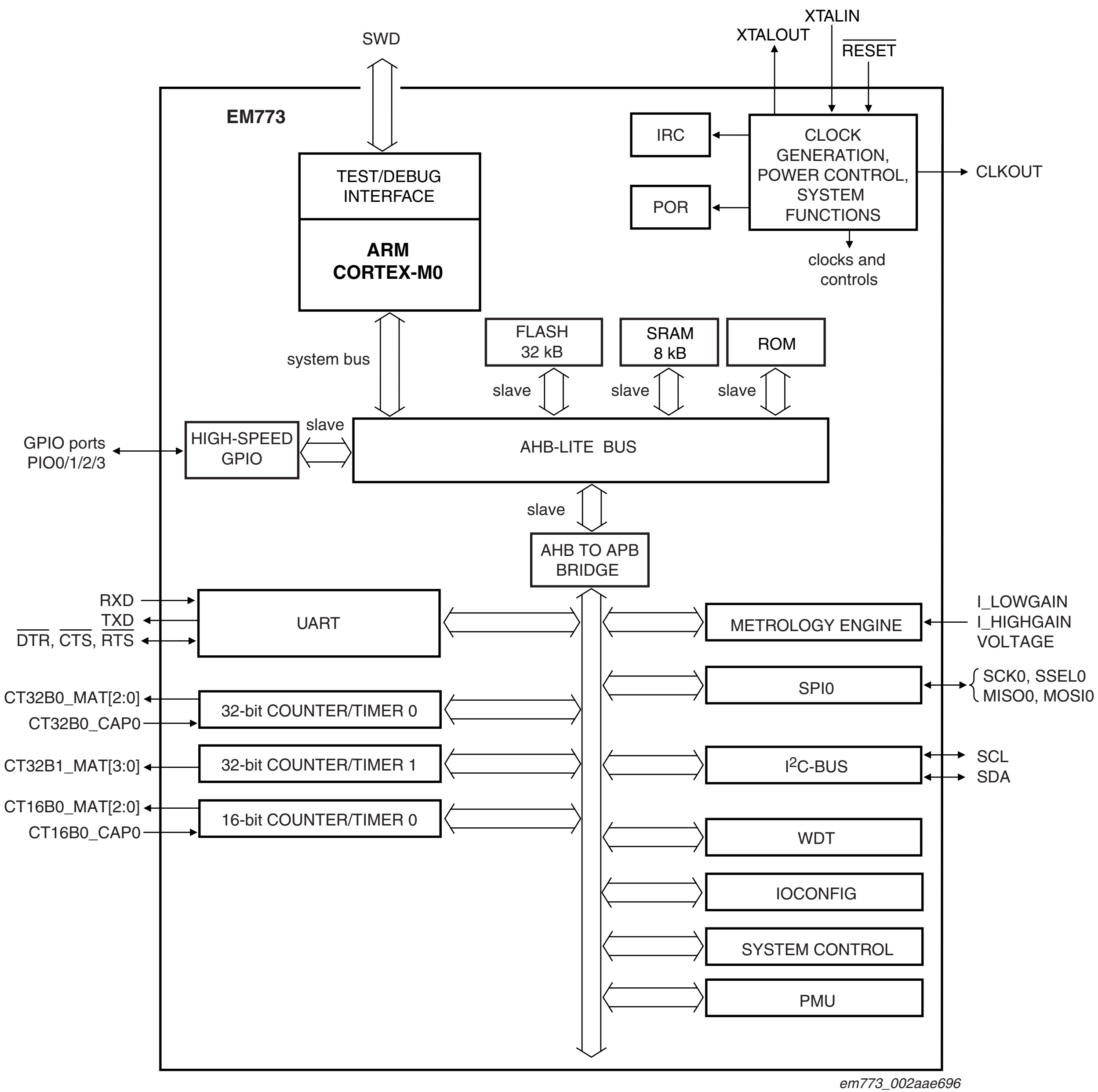


Fig 1. EM773 block diagram

6. Pinning information

6.1 Pinning

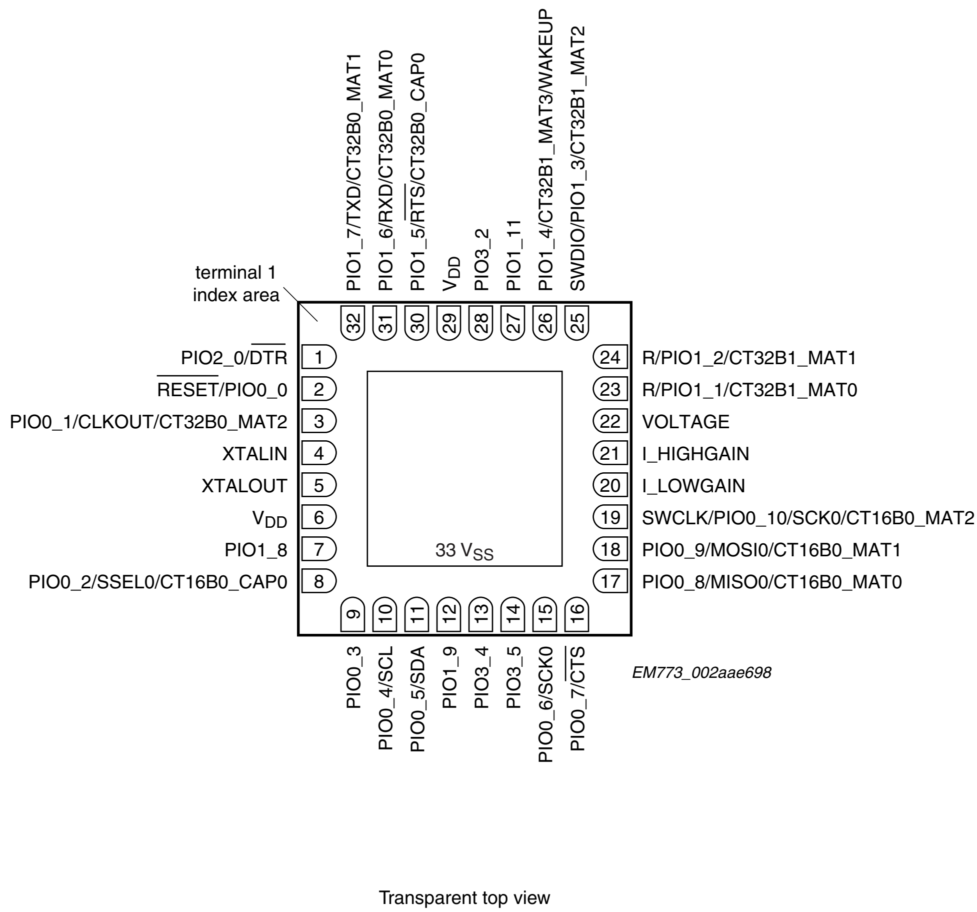


Fig 2. Pin configuration HVQFN 33 package

6.2 Pin description

Table 2. EM773 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_10			I/O		**Port 0** — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block. Pin PIO0_11 is not available.
$\overline{\text{RESET}}$/PIO0_0	2[2]	yes	I	I;PU	**$\overline{\text{RESET}}$** — External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
			I/O	-	**PIO0_0** — General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[3]	yes	I/O	I;PU	**PIO0_1** — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT** — Clock out pin.
			O	-	**CT32B0_MAT2** — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[3]	yes	I/O	I;PU	**PIO0_2** — General purpose digital input/output pin.
			I/O	-	**SSEL0** — Slave select for SPI0.
			I	-	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	**PIO0_3** — General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	IA	**PIO0_4** — General purpose digital input/output pin (open-drain).
			I/O	-	**SCL** — I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	IA	**PIO0_5** — General purpose digital input/output pin (open-drain).
			I/O	-	**SDA** — I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	**PIO0_6** — General purpose digital input/output pin.
			I/O	-	**SCK0** — Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	16[3]	yes	I/O	I;PU	**PIO0_7** — General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$** — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[3]	yes	I/O	I;PU	**PIO0_8** — General purpose digital input/output pin.
			I/O	-	**MISO0** — Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0** — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[3]	yes	I/O	I;PU	**PIO0_9** — General purpose digital input/output pin.
			I/O	-	**MOSI0** — Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.

Table 2. EM773 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19[3]	yes	I	I;PU	**SWCLK** — Serial wire clock.
			I/O	-	**PIO0_10** — General purpose digital input/output pin.
			I/O	-	**SCK0** — Serial clock for SPI0.
			O	-	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
I_HIGHGAIN	21[5]	no	I	I;PU	**I_HIGHGAIN** — High gain current input for metrology engine.
PIO1_1 to PIO1_9; PIO1_11			I/O		**Port 1** — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block. Pins PIO1_0 and PIO1_10 are not available.
VOLTAGE	22[5]	no	I	I;PU	**VOLTAGE** — Voltage input for the metrology engine.
R/PIO1_1/ CT32B1_MAT0	23[5]	no	O	I;PU	**R** — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1** — General purpose digital input/output pin.
			O	-	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
R/PIO1_2/ CT32B1_MAT1	24[5]	no	I	I;PU	**R** — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2** — General purpose digital input/output pin.
			O	-	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ CT32B1_MAT2	25[5]	no	I/O	I;PU	**SWDIO** — Serial wire debug input/output.
			I/O	-	**PIO1_3** — General purpose digital input/output pin.
			O	-	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO1_4/ CT32B1_MAT3/WAKEUP	26	no	I/O	I;PU	**PIO1_4** — General purpose digital input/output pin.
			O	-	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
			I	-	**WAKEUP** — Deep power-down mode wake-up pin. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	30[3]	no	I/O	I;PU	**PIO1_5** — General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$** — Request To Send output for UART.
			I	-	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31[3]	no	I/O	I;PU	**PIO1_6** — General purpose digital input/output pin.
			I	-	**RXD** — Receiver input for UART.
			O	-	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	32[3]	no	I/O	I;PU	**PIO1_7** — General purpose digital input/output pin.
			O	-	**TXD** — Transmitter output for UART.
			O	-	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO1_8	7[3]	no	I/O	I;PU	**PIO1_8** — General purpose digital input/output pin.
PIO1_9	12[3]	no	I/O	I;PU	**PIO1_9** — General purpose digital input/output pin.
I_LOWGAIN	20	no	I	I;PU	**I_LOWGAIN** — Low gain current input for metrology engine.

Table 2. EM773 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_11	27	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
PIO2_0			I/O		**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.
PIO2_0/$\overline{DTR}$	1[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{DTR}$ —** Data Terminal Ready output for UART.
PIO3_0 to PIO3_5		no	I/O		**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2	28[3]	no	I/O	I;PU	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
PIO3_5	14[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
V_{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the metrology engine.
XTALIN	4[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	33	-	-	-	Thermal pad. Connect to ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled.

[2] See Figure 24 for the reset pad configuration. $\overline{RESET}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 23).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input.

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The EM773 contains 32 kB of on-chip flash memory.

7.3 On-chip SRAM

The EM773 contains a total of 8 kB on-chip static RAM memory.

7.4 Memory map

The EM773 incorporates several distinct memory regions, shown in the following figures. Figure 3 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

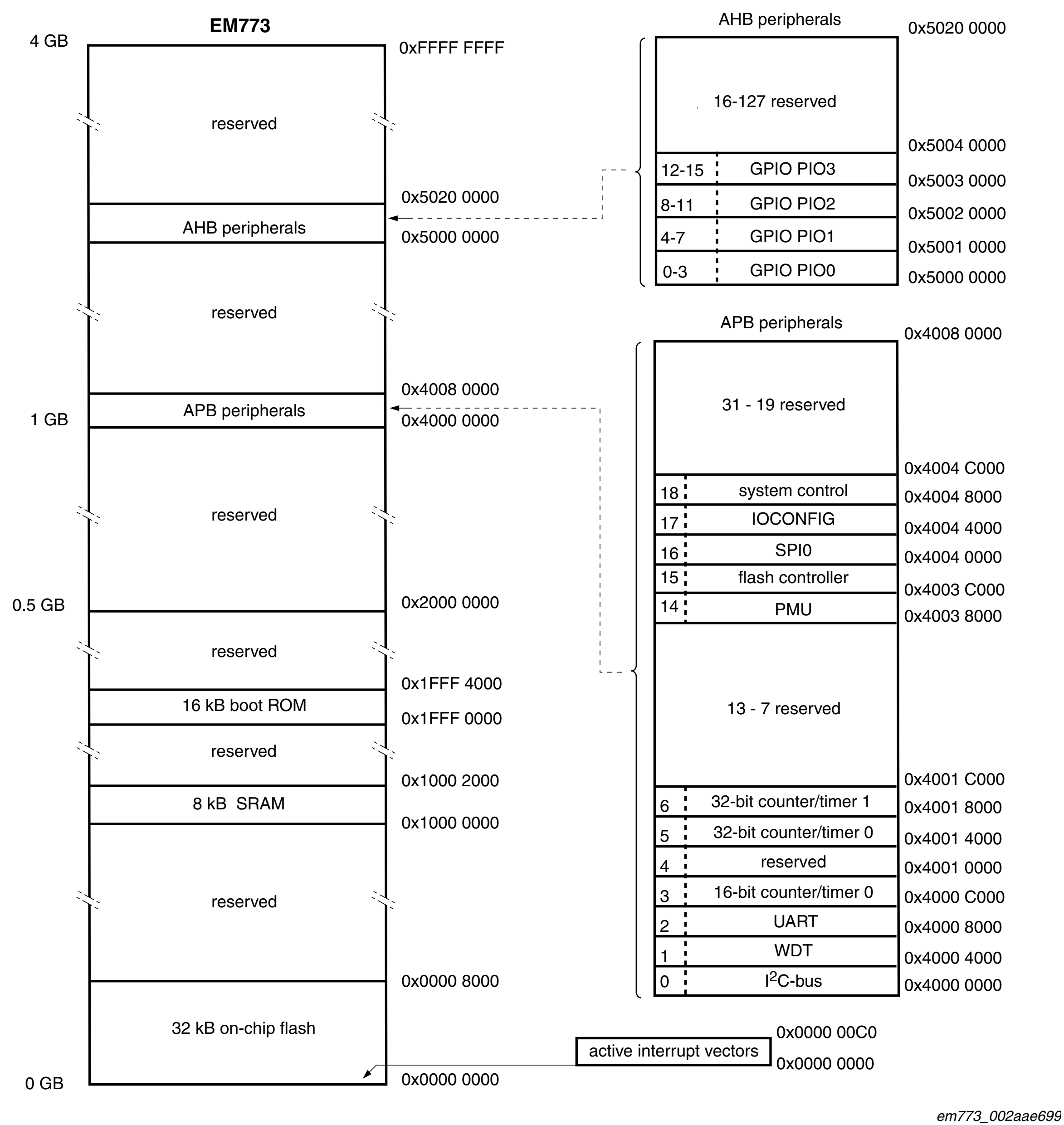


Fig 3. EM773 memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the EM773, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 25 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

EM773 uses accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 25 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.

7.8 UART

The EM773 contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SPI serial I/O controller

The EM773 contains one SPI controller.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I^2C-bus serial I/O controller

The EM773 contains one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^2C-interface is a standard I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 Metrology engine

The EM773 contains a metrology engine designed to collect voltage and current inputs to calculate the active power, reactive power, apparent power and power factor of a load. The purpose of the metrology engine is for non-billing applications such as plug meters, smart appliances, industrial and consumer sub-meters, etc.

7.11.1 Features

- 1 % accurate for scalable input sources up to 230 V/50 Hz/16 A and 110 V/60 Hz/20 A while maintaining this accuracy with a factor of 1 to 400 down from this maximum current.
- Automatically calculates active power in W, reactive power in VAr, apparent power in VA, power factor ratio, Vrms and Irms without ARM CPU intervention.
- Standard API for initializing, starting, stopping and reading data from the metrology engine using the ARM Cortex M0.

7.12 General purpose external event counter/timers

The EM773 includes two 32-bit counter/timers and one 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.

- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.14 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a selectable time period.

7.14.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the Watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.15 Clocking and power control

7.15.1 Crystal oscillators

The EM773 includes three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the EM773 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the EM773 clock generation.

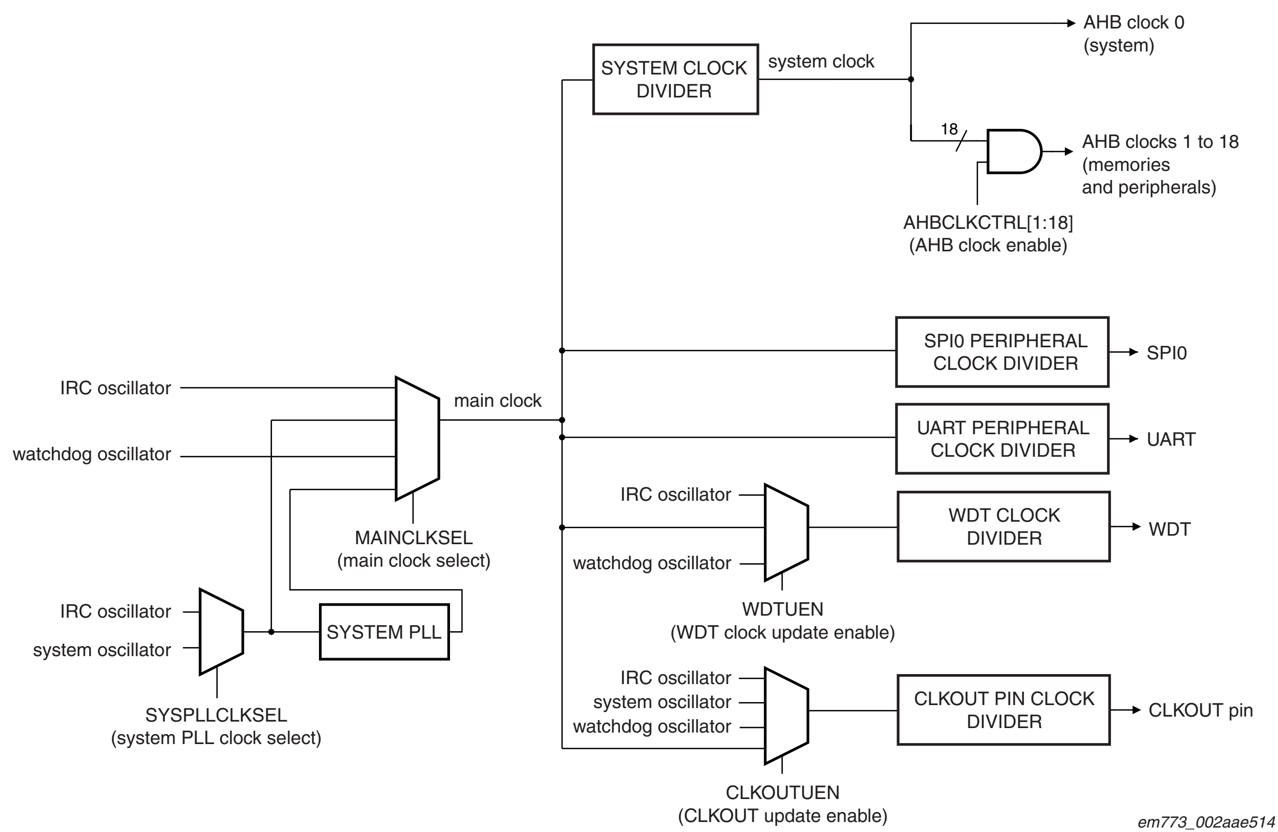


Fig 4. EM773 clock generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the EM773 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.15.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 %.

7.15.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.15.3 Clock output

The EM773 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.15.4 Wake-up process

The EM773 begins operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the system oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.15.5 Power control

The EM773 supports a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.15.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.15.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 13 pins total serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.15.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The EM773 can wake up from Deep power-down mode via the WAKEUP pin.

7.16 System control

7.16.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 2 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.16.2 Reset

Reset has four sources on the EM773: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.16.3 Brownout detection

The EM773 includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.16.4 Code security (Code Read Protection - CRP)

This feature of the EM773 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *EM773 user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *EM773 user manual*.

7.16.5 APB interface

The APB peripherals are located on one APB bus.

7.16.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.16.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	−0.5	+5.5	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

Table 4. Static characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4] [5][6]	-	3	-	mA
		system clock = 50 MHz V_{DD} = 3.3 V	[2][3][5] [6][7]	-	9	-	mA
		Sleep mode; system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4] [5][6]	-	2	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V	[2][3][8]	-	6	-	μA
		Deep power-down mode; V_{DD} = 3.3 V	[2][9]	-	220	-	nA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[10][11] [12]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = –4 mA		V_{DD} – 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OH} = –3 mA		V_{DD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA		-	-	0.4	V

Table 4. Static characteristics *...continued*
T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; $2.0\ V \le V_{DD} \le 3.6$ V		–4	-	-	mA
		$1.8\ V \le V_{DD} < 2.0$ V		–3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V $2.0\ V \le V_{DD} \le 3.6$ V		4	-	-	mA
		$1.8\ V \le V_{DD} < 2.0$ V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[13]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; $2.0\ V \le V_{DD} \le 3.6$ V		–15	–50	–85	µA
		$1.8\ V \le V_{DD} < 2.0$ V		–10	–50	–85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[10][11][12]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6$ V; I_{OH} = –20 mA		$V_{DD} - 0.4$	-	-	V
		$1.8\ V \le V_{DD} < 2.5$ V; I_{OH} = –12 mA		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.0\ V \le V_{DD} \le 3.6$ V; I_{OL} = 4 mA		-	-	0.4	V
		$1.8\ V \le V_{DD} < 2.0$ V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; $2.5\ V \le V_{DD} \le 3.6$ V		20	-	-	mA
		$1.8\ V \le V_{DD} < 2.5$ V		12	-	-	mA

Table 4. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V		–15	–50	–85	µA
		1.8 V ≤ V_{DD} < 2.0 V		–10	–50	–85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I²C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.5V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as standard mode pins 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins 2.0 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[14]	-	2	4	µA
		V_I = 5 V		-	10	22	µA

Table 4. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(xtal)}$	crystal input voltage		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage		−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] BOD disabled.

[6] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[7] IRC disabled; system oscillator enabled; system PLL enabled.

[8] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0xFFFF FDFF.

[9] WAKEUP pin pulled HIGH externally.

[10] Including voltage on outputs in 3-state mode.

[11] V_{DD} supply voltage must be present.

[12] 3-state outputs go into 3-state mode in Deep power-down mode.

[13] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[14] To V_{SS}.

9.1 BOD static characteristics

Table 5. BOD static characteristics[1]

T_{amb} = 25 °C.

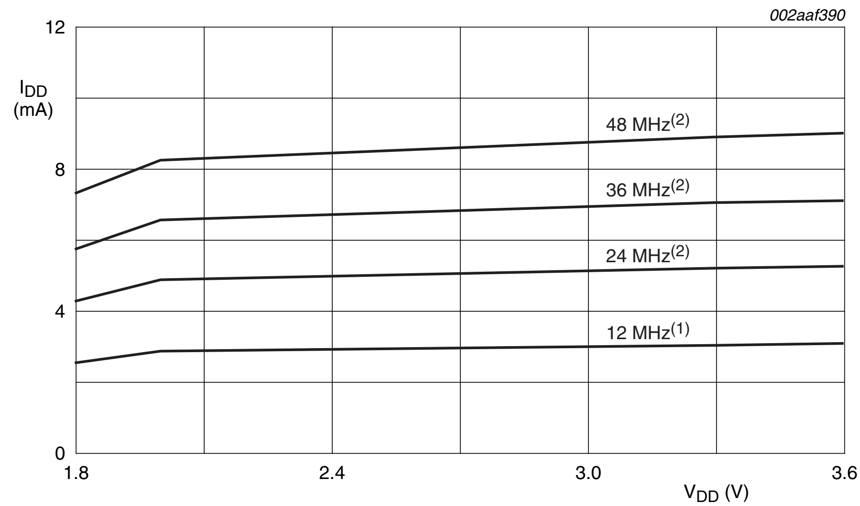
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *EM773 user manual*.

9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *EM773 user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

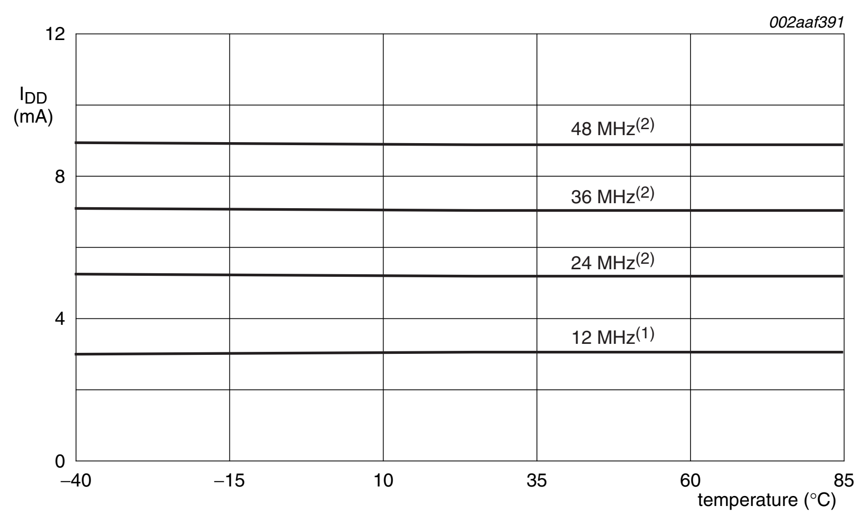


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the AHBCLKCTRL register (AHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 5. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies

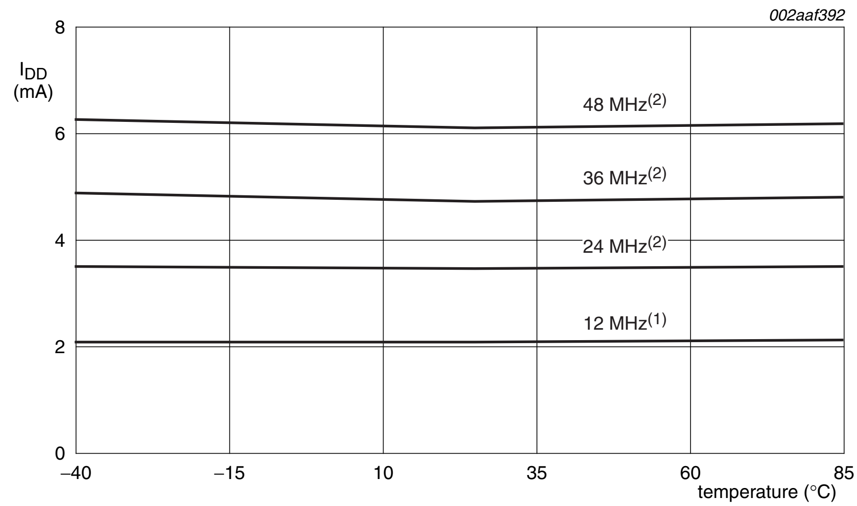


Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the AHBCLKCTRL register (AHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 6. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

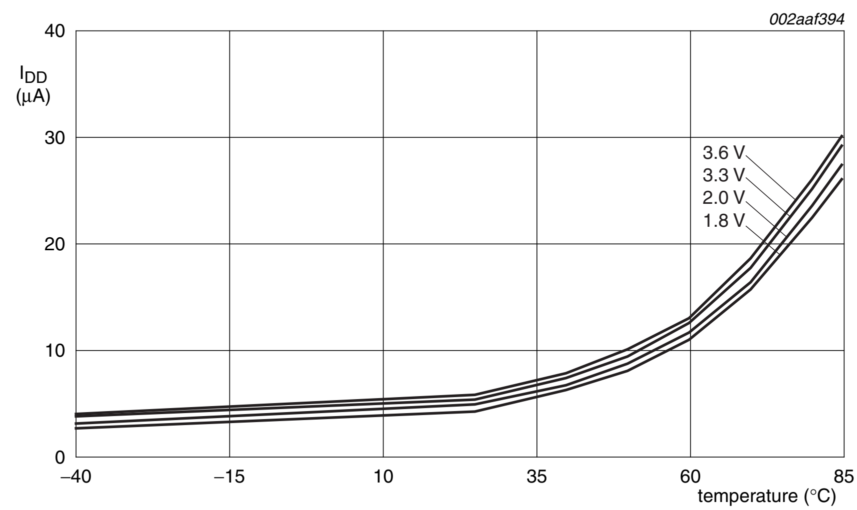


Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the AHBCLKCTRL register (AHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 7. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0xFFFF FDFF).

Fig 8. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

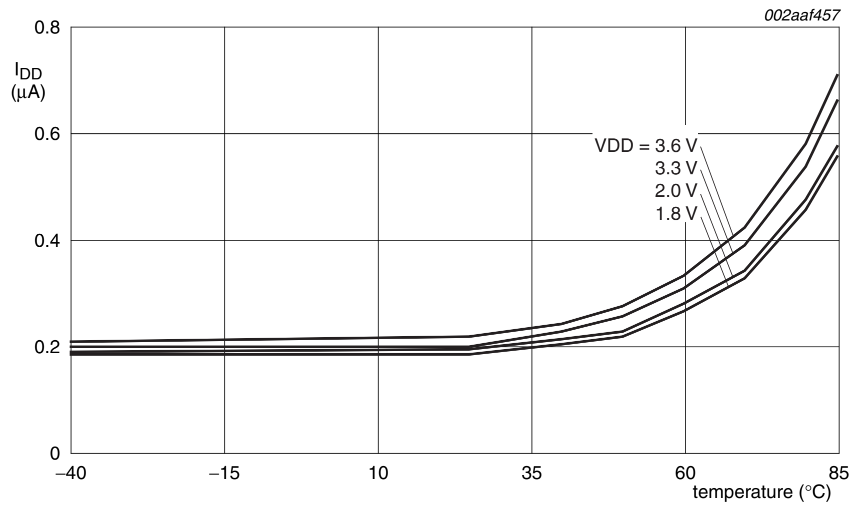
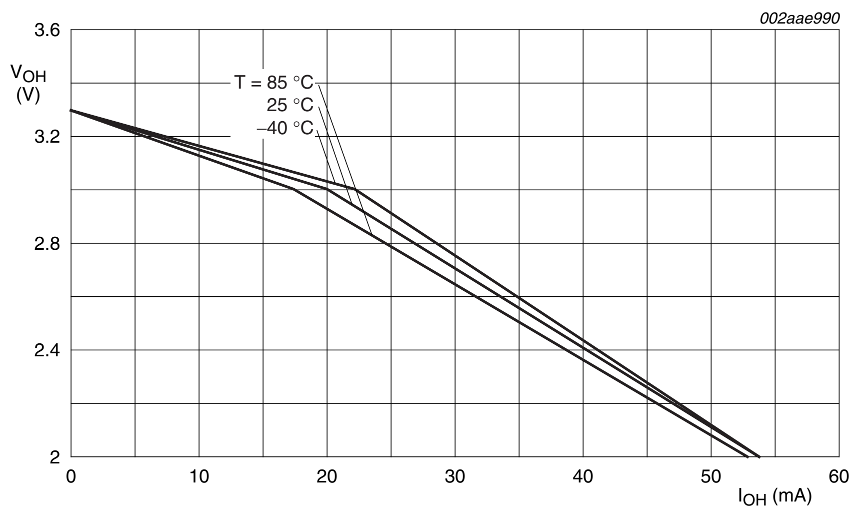


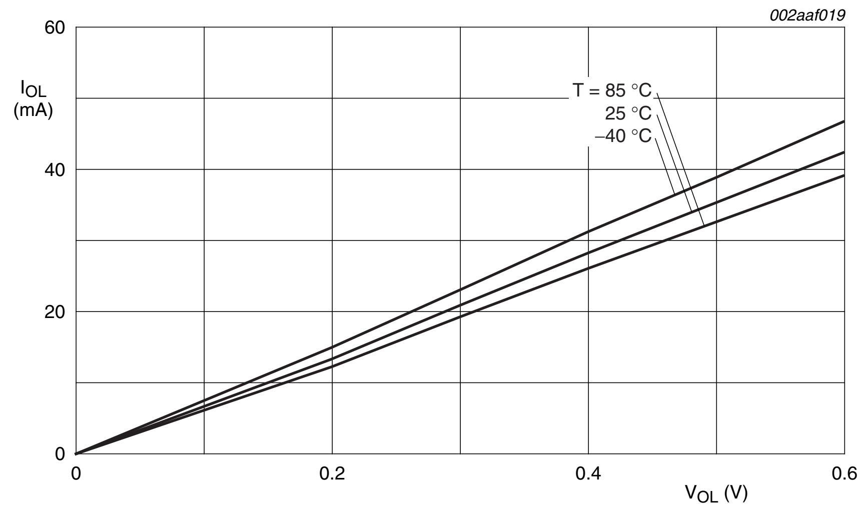
Fig 9. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

9.3 Electrical pin characteristics



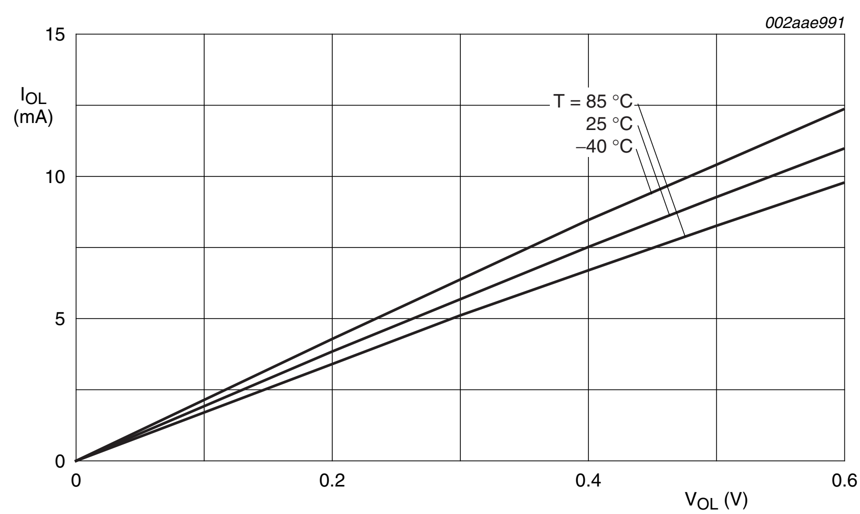
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 10. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



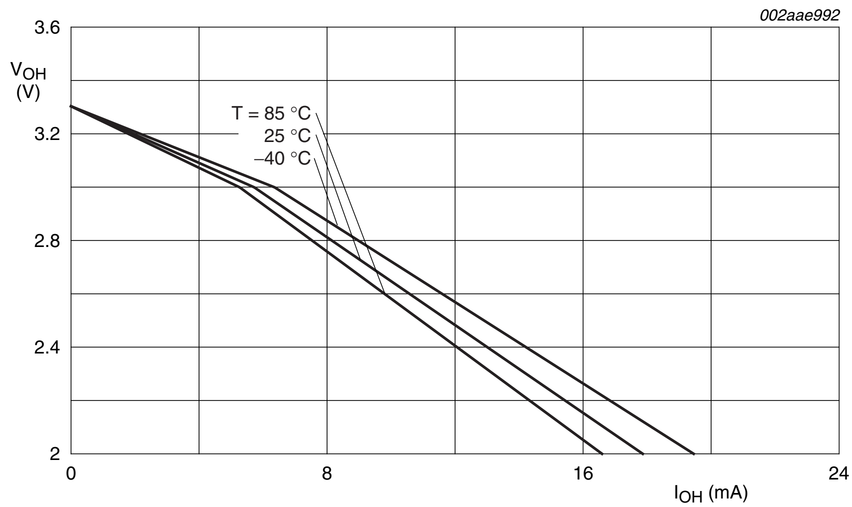
Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 11. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



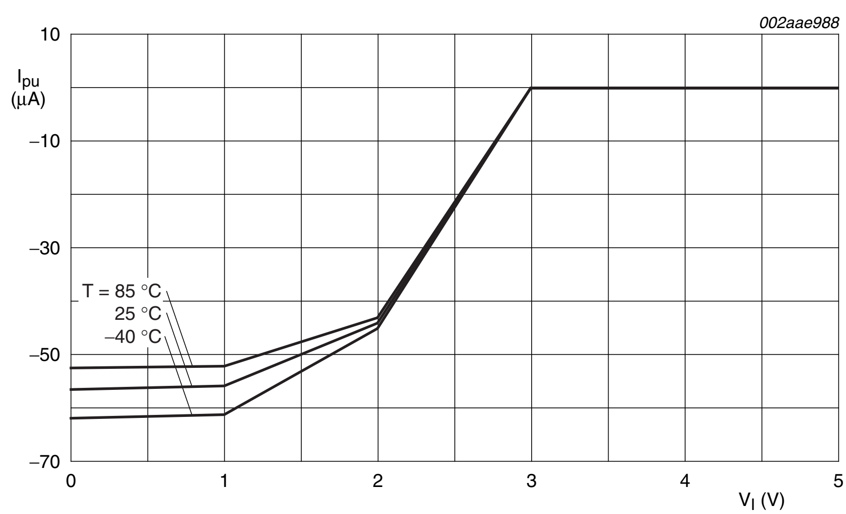
Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 12. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



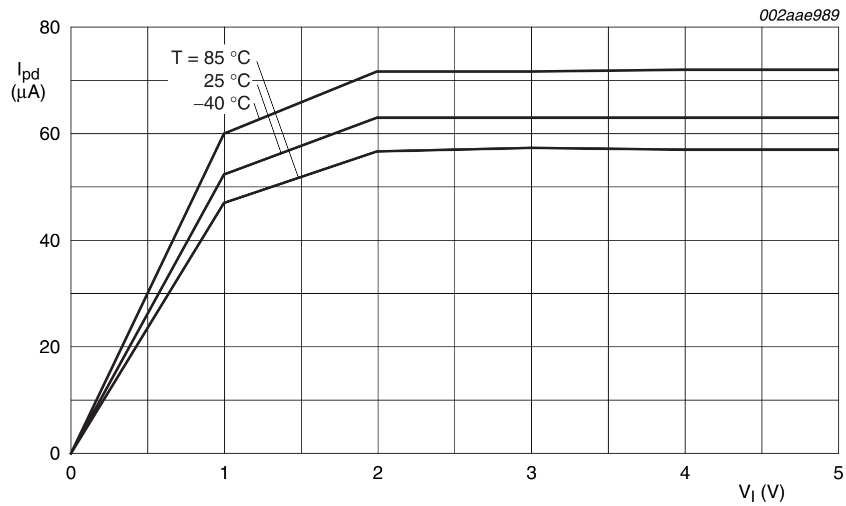
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 13. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 14. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 15. Typical pull-down current I_{pd} versus input voltage V_I

10. Dynamic characteristics

10.1 Flash memory

Table 6. Flash characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

10.2 External clock

Table 7. Dynamic characteristic: external clock

T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

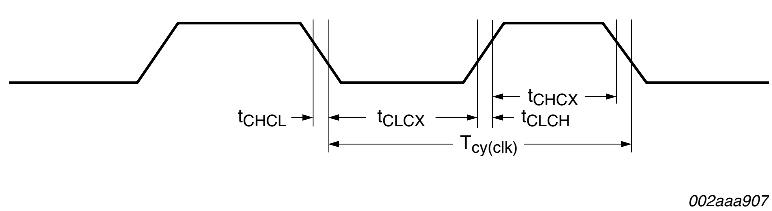


Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.3 Internal oscillators

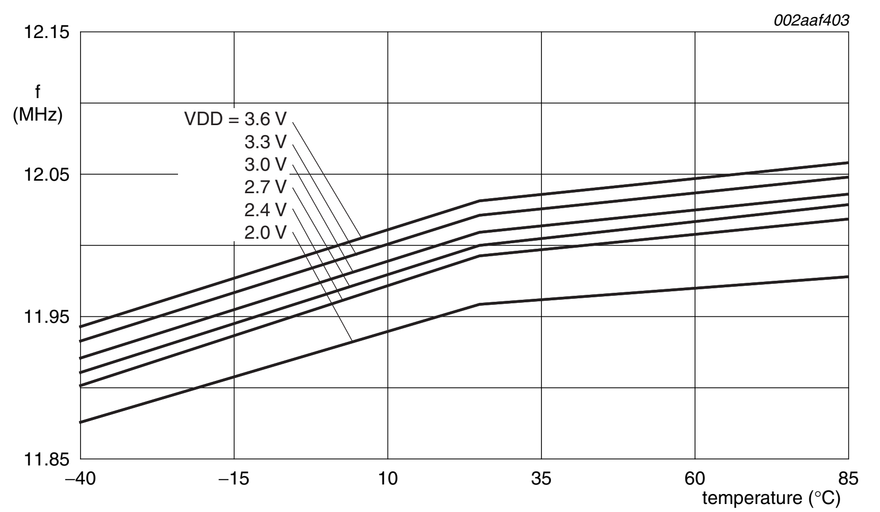
Table 8. Dynamic characteristic: internal oscillators

T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 17. Internal RC oscillator frequency vs. temperature

Table 9. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{osc}	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +85 °C) is ±40 %.

[3] See the *EM773 user manual*.

10.4 I/O pins

Table 10. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I²C-bus

Table 11. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	μs
			Fast-mode	1.3	-	μs
			Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	μs
			Fast-mode	0.6	-	μs
			Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	μs
			Fast-mode	0	-	μs
			Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

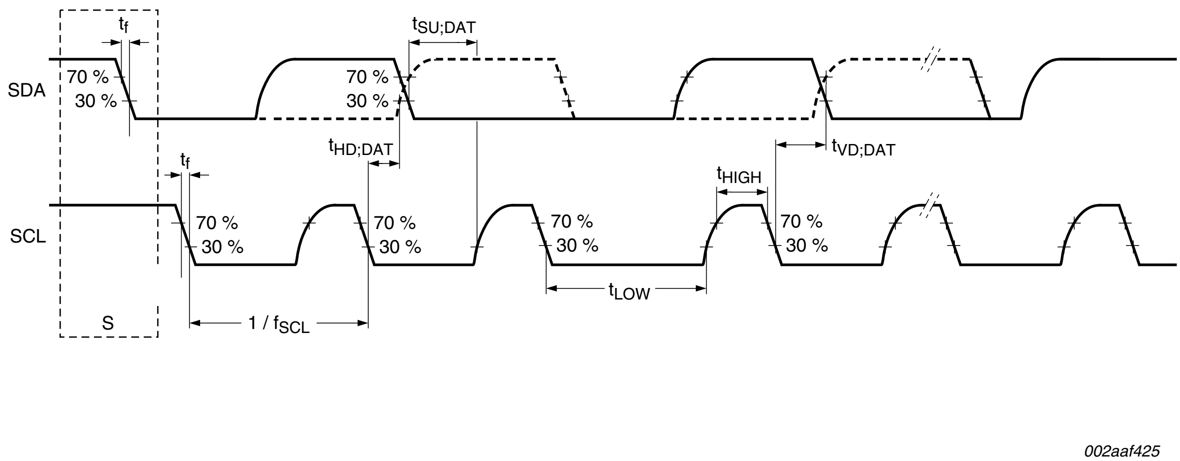


Fig 18. I²C-bus pins clock timing

10.6 SPI interfaces

Table 12. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	when only receiving	[1]	40	-	-	ns
		when only transmitting	[1]	27.8			ns
t_{DS}	data set-up time	in SPI mode 2.4 V ≤ V_{DD} ≤ 3.6 V	[2]	15	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V	[2]	20			ns
		1.8 V ≤ V_{DD} < 2.0 V	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns

Table 12. Dynamic characteristics of SPI pins in SPI mode

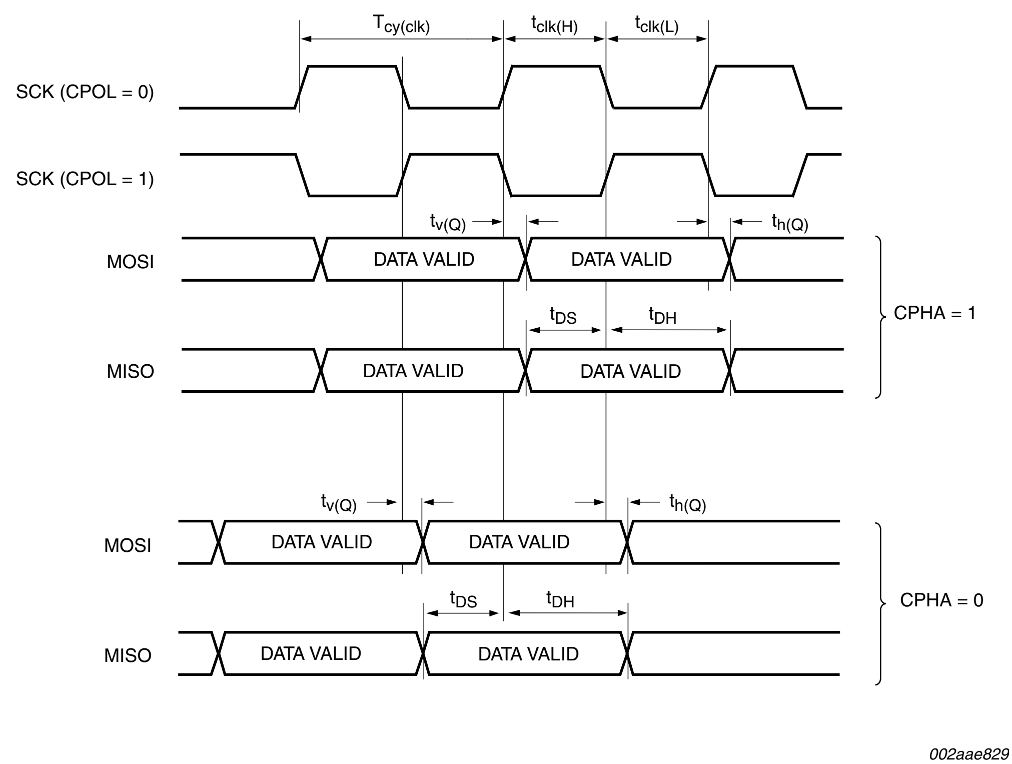
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40$ °C to 85 °C.

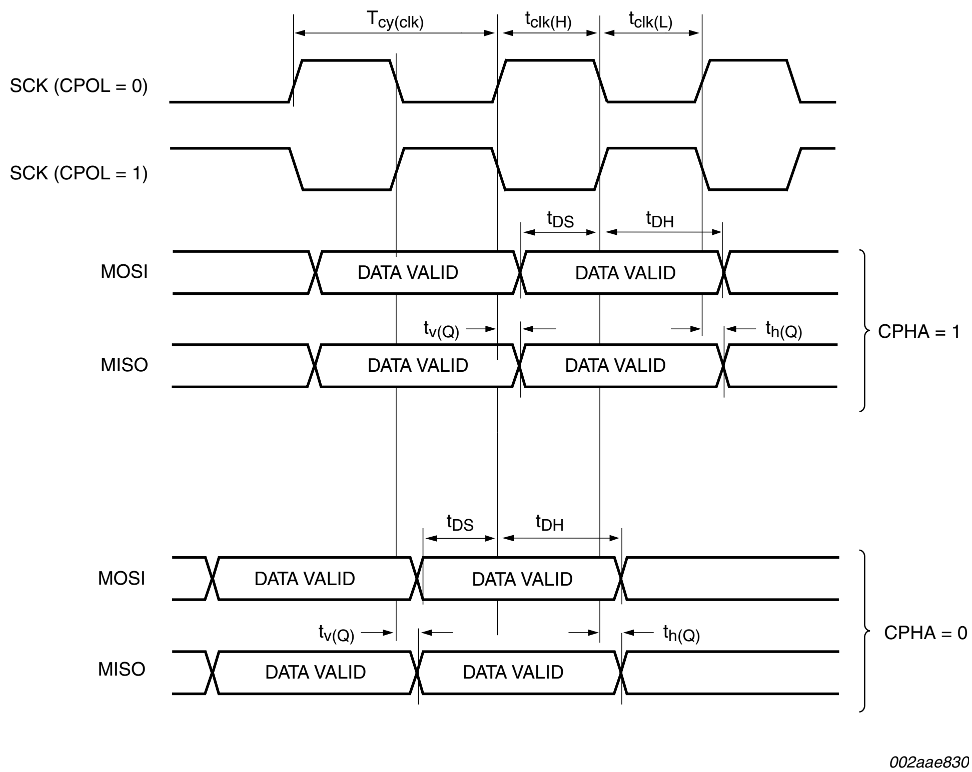
[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25$ °C; for normal voltage supply range: $V_{DD} = 3.3$ V.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 19. SPI master timing in SPI mode



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 20. SPI slave timing in SPI mode

11. Application information

11.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

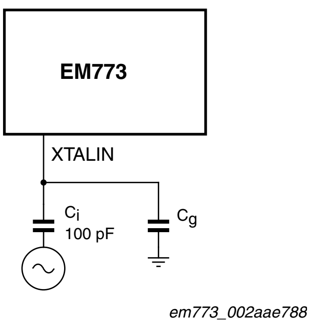


Fig 21. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 21), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 22 and in Table 13 and Table 14. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 22 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 13).

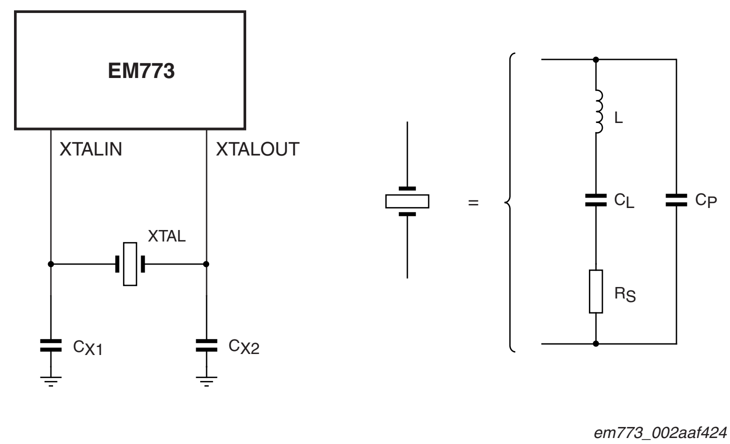


Fig 22. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 13. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 14. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

11.3 Standard I/O pad configuration

Figure 23 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

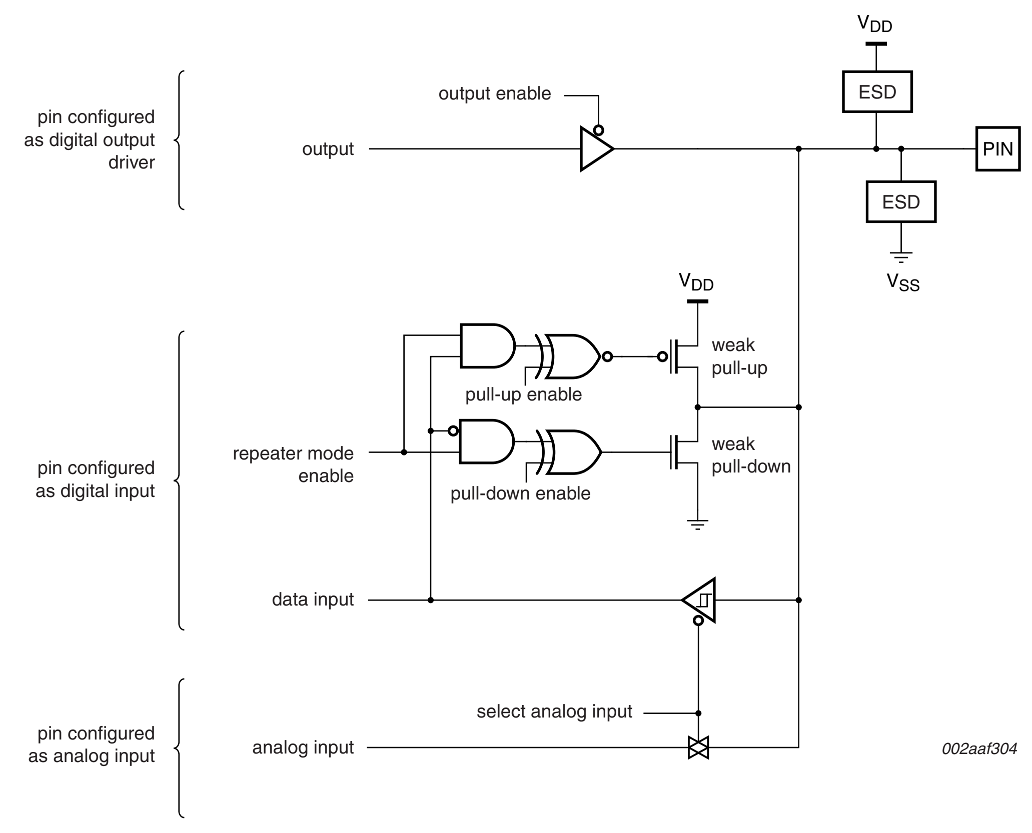


Fig 23. Standard I/O pad configuration

11.4 Reset pad configuration

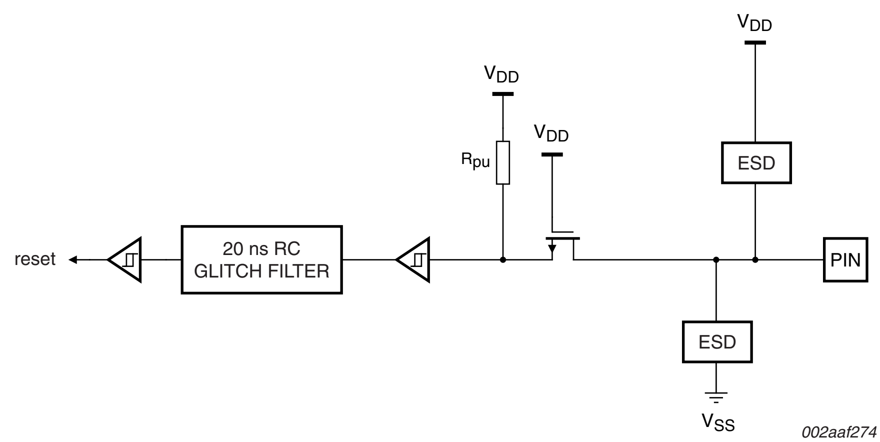
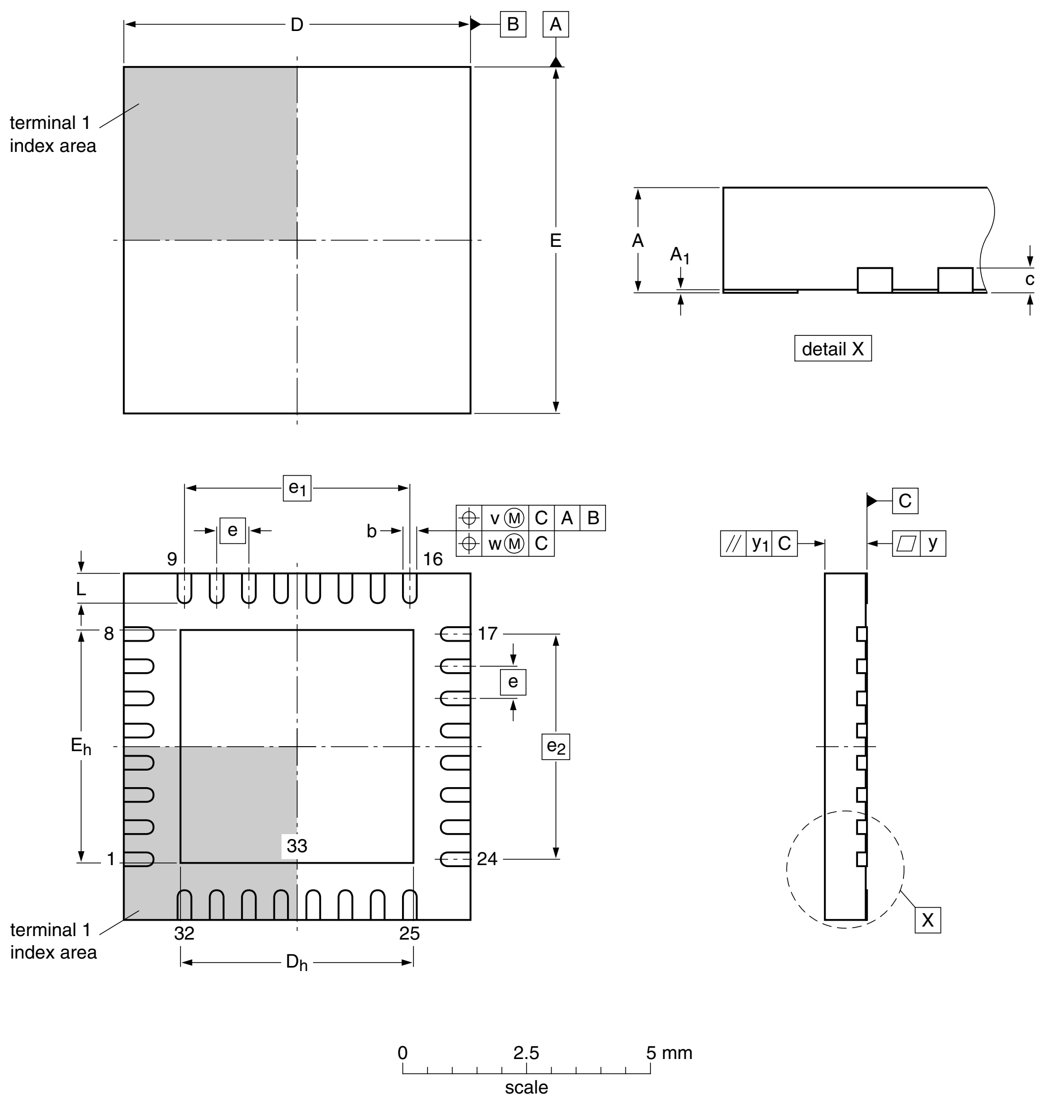


Fig 24. Reset pad configuration

12. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
			- - -			~~09-03-17~~ 09-03-23

Fig 25. Package outline (HVQFN33)

13. Abbreviations

Table 15. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

14. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
EM773 v.1	<tbd>	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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