IBM

IBM13T8644HPB
IBM13T8644HPC

8M x 64 SDRAM SO DIMM

Features

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual-In-line Memory Module
- 8Mx64 Synchronous DRAM SO DIMM
- Low Power
- Performance:

	-360	-10	Units
$\overline{CAS}$ Latency	3	3	
f_{CK} Clock Frequency	100	100	MHz
t_{CK} Clock Cycle	10	10	ns
t_{AC} Clock Access Time	6	7	ns

- Inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have 4 internal banks
- Fully Synchronous to positive Clock Edge

- Programmable Operation:
  - CAS Latency: 2, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 12/9/2 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size:
  - 2.66" x 1.15" x 0.149" (IBM13T8644HPB)
  - 2.66" x 1.05" x 0.149" (IBM13T8644HPC)
- Gold contacts
- SDRAMs in TSOP Type II Package

Description

IBM13T8644HPB and IBM13T8644HPC are 144-pin Synchronous DRAM Small Outline Dual In-line Memory Modules (SO DIMMs) organized as 8Mx64 high-speed memory arrays. These SO DIMMs use eight 8Mx8 SDRAMs in 400mil TSOP II packages. They achieve high speed data transfer rates of up to 100MHz by employing a prefetch/pipe-line hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

The SO DIMM is intended to comply with all JEDEC standards set for 144 pin SDRAM SO DIMMs.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs. All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK1). Internal operating modes are defined by combinations of the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S}0$, DQMB, and CKE0 signals. A command decoder initiates the necessary timings for each operation. A 12 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the SO DIMM by address inputs A0-A9 during the Mode Register Set cycle.

The SO DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.66" long space-saving footprint. Related products are in the EDO DRAM SO DIMM family.

Card Outline

| (Front) | 1 | 59 | 61 | 143 |
| (Back) | 2 | 60 | 62 | 144 |
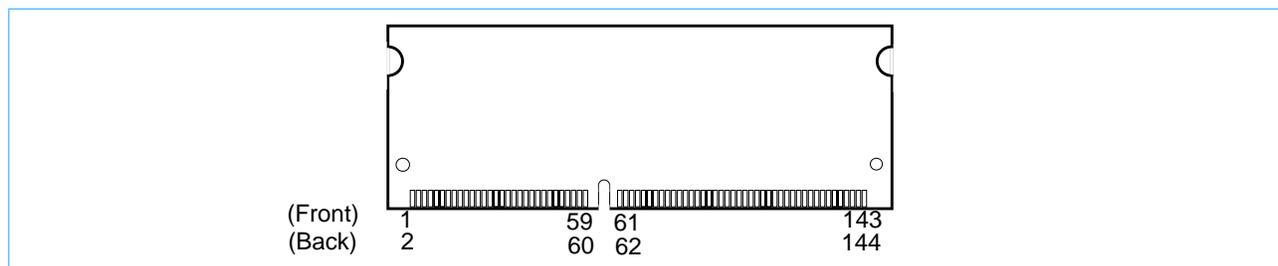
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Pin Description

|				
CK0, CK1	Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0	Clock Enable	DQMB0 - DQMB7	Data Mask
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power (3.3V) 6/8/98
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	NC	No Connect
$\overline{S}0$	Chip Select	SCL	Serial Presence Detect Clock Input
A0 - A9, A11	Address Inputs	SDA	Serial Presence Detect Data Input/Output
A10/AP	Address Input/Autoprecharge	SA0-2	Serial Presence Detect Address Inputs
BA0 - BA1	SDRAM Bank Address		

Pinout

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	2	V_{SS}	37	DQ8	38	DQ40	71	NC	72	NC	107	V_{SS}	108	V_{SS}
3	DQ0	4	DQ32	39	DQ9	40	DQ41	73	DU	74	CK1	109	A9	110	BA1
5	DQ1	6	DQ33	41	DQ10	42	DQ42	75	V_{SS}	76	V_{SS}	111	A10/AP	112	A11
7	DQ2	8	DQ34	43	DQ11	44	DQ43	77	NC	78	NC	113	V_{DD}	114	V_{DD}
9	DQ3	10	DQ35	45	V_{DD}	46	V_{DD}	79	NC	80	NC	115	DQMB2	116	DQMB6
11	V_{DD}	12	V_{DD}	47	DQ12	48	DQ44	81	V_{DD}	82	V_{DD}	117	DQMB3	118	DQMB7
13	DQ4	14	DQ36	49	DQ13	50	DQ45	83	DQ16	84	DQ48	119	V_{SS}	120	V_{SS}
15	DQ5	16	DQ37	51	DQ14	52	DQ46	85	DQ17	86	DQ49	121	DQ24	122	DQ56
17	DQ6	18	DQ38	53	DQ15	54	DQ47	87	DQ18	88	DQ50	123	DQ25	124	DQ57
19	DQ7	20	DQ39	55	V_{SS}	56	V_{SS}	89	DQ19	90	DQ51	125	DQ26	126	DQ58
21	V_{SS}	22	V_{SS}	57	NC	58	NC	91	V_{SS}	92	V_{SS}	127	DQ27	128	DQ59
23	DQMB0	24	DQMB4	59	NC	60	NC	93	DQ20	94	DQ52	129	V_{DD}	130	V_{DD}
25	DQMB1	26	DQMB5		VOLTAGE KEY			95	DQ21	96	DQ53	131	DQ28	132	DQ60
27	V_{DD}	28	V_{DD}	61	CK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
29	A0	30	A3	63	V_{DD}	64	V_{DD}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
31	A1	32	A4	65	$\overline{RAS}$	66	$\overline{CAS}$	101	V_{DD}	102	V_{DD}	137	DQ31	138	DQ63
33	A2	34	A5	67	$\overline{WE}$	68	NC	103	A6	104	A7	139	V_{SS}	140	V_{SS}
35	V_{SS}	36	V_{SS}	69	$\overline{S}0$	70	NC	105	A8	106	BA0	141	SDA	142	SCL
												143	V_{DD}	144	V_{DD}

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13T8644HPB-10T	8Mx64	10ns	gold	2.66" x 1.15" x 0.149"	3.3V
IBM13T8644HPC-10T				2.66" x 1.05" x 0.149"	

8M x 64 SDRAM SO DIMM Block Diagram

* CLOCK WIRING	
CLOCK INPUT	SDRAMs
*CK0	4 SDRAMs
*CK1	4 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

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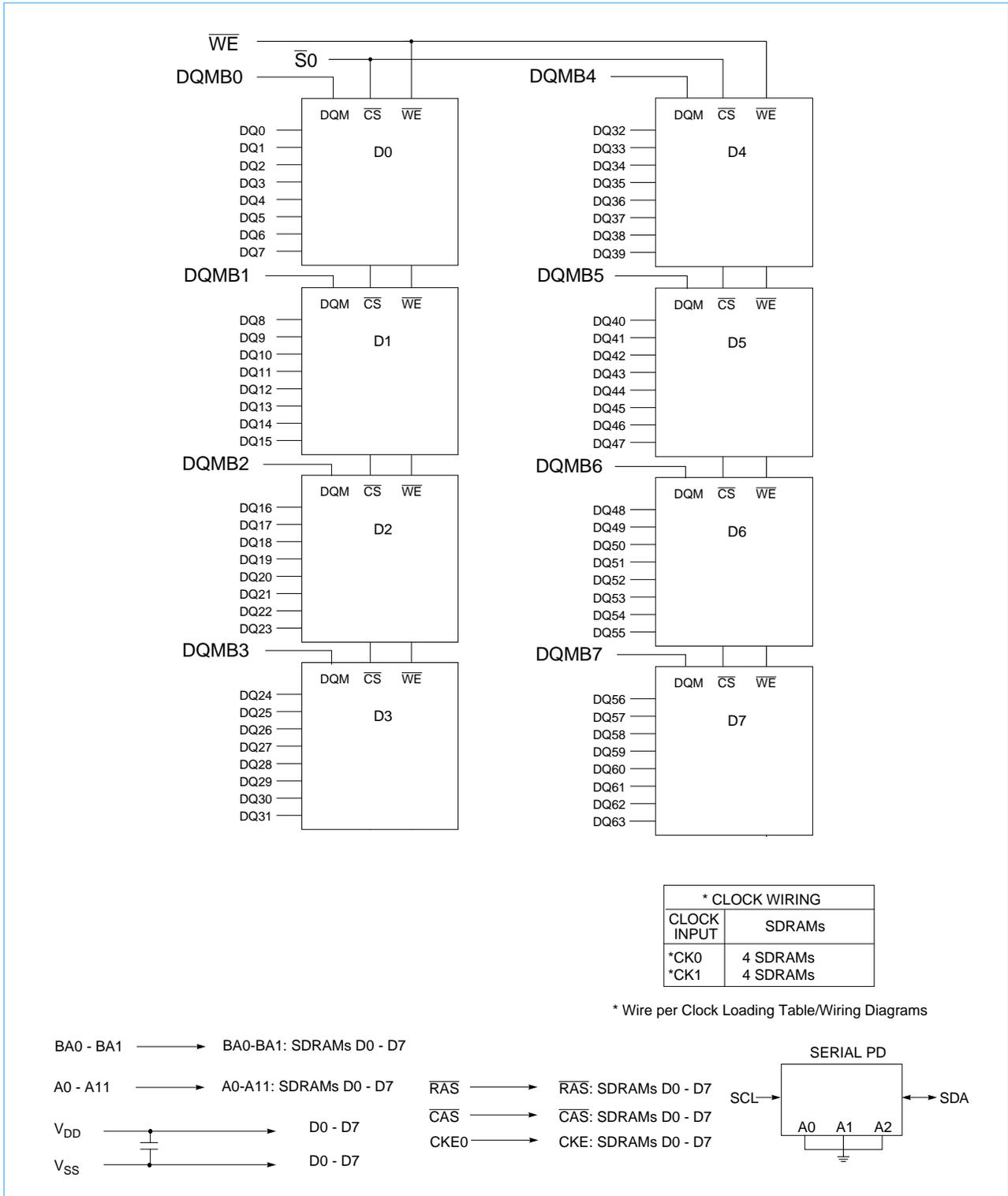
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Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0, CK1	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0, CKE1	Input	Level	Active High	Activates the CK0 and CK1 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S}0$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, BA1	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A9, A11, A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A7 defines the column address (CA0-CA8) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0 defines the bank to be precharged (low=bank A, high=bank B). If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0 to control which bank(s) to precharge. If AP is high, both bank A and bank B will be precharged regardless of the state of BA0. If AP is low, then BA0 is used to define which bank to precharge.
DQ0 - DQ63	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
SDA	Input Output	Level	—	Serial Data. Bidirectional signal used to transfer data into and out of the Serial Presence Detect EEPROM. Since the SDA signal is Open Drain/Open Collector at the EEPROM, a pull-up resistor is required on the system board.
SCL	Input	Pulse	—	Serial Clock. Used to clock all Serial Presence Detect data into and out of the EEPROM. Since the SCL signal is inactive in the "high" state, a pull-up resistor is recommended on the system board.
V_{DD}, V_{SS}	Supply			Power and ground for the module.

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Serial Presence Detect (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	9	09	
5	Number of DIMM Banks	1	01	
6 - 7	Data Width of Assembly	x64	4000	
8	Voltage Interface Level of this Assembly	LVTTL	01	
9	SDRAM Device Cycle Time at CL=3	10.0ns	A0	
10	SDRAM Device Access Time from Clock at CL=3	7.0ns	70	
11	DIMM Configuration Type	Non-Parity	00	
12	Refresh Rate/Type	SR/1x(15.625µs)	80	
13	Primary SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	N/A	00	
15	SDRAM Device Attr: Min CK Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	2, 3	06	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	
21	SDRAM Module Attributes	Unbuffered	00	
22	SDRAM Device Attributes: General	Wr-1/Rd Burst, Precharge All, Auto-Precharge, $V_{DD} \pm 10\%$	0E	
23	Minimum Clock Cycle at CL=2	15.0ns	F0	
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2	8.0ns	80	
25	Minimum Clock Cycle Time at CL=1	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=1	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	30ns	1E	
28	Minimum Row Active to Row Active delay (t_{RRD})	20ns	14	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	30ns	1E	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	60ns	3C	
31	Module Bank Density	64MB	10	
32	Address and Command Setup Time Before Clock	3.0	30	
33	Address and Command Hold Time After Clock	1.0	10	
34	Data Input Setup Time Before Clock	3.0	30	
35	Data Input Hold Time After Clock	1.0	10	
36 - 61	Reserved	Undefined	00	
62	SPD Revision	2	02	
63	Checksum for bytes 0 - 62	Checksum Data	cc	1
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) '00-63 (Hex)
5. ww = Binary coded decimal week code, 01-53 (Decimal) '01-35 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

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Serial Presence Detect (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Module Part Number	ASCII '13T8644HP"R"-10T'	313354383634344850 rr2D31305420202020	2, 3
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	4, 5
95 - 98	Module Serial Number	Serial Number	ssssssss	6
99 - 125	Reserved	Undefined	00	
126	Module Supports this Clock Frequency	66 MHz	66	
127	Attributes for Clock Frequency defined in byte 126	2, 3	C6	
128 - 255	Open for Customer Use	Undefined	00	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) '00-63 (Hex)
5. ww = Binary coded decimal week code, 01-53 (Decimal) '01-35 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{DD}	Power Supply Voltage		−0.3 to + 4.6		
V_{IN}	Input Voltage	SDRAM Devices	−0.3 to + V_{DD} + 0.3	V	1
		Serial PD Device	−0.3 to + 6.5		
V_{OUT}	Output Voltage	SDRAM Devices	−0.3to + V_{DD} + 0.3		
		Serial PD Device	−0.3 to + 6.5		
T_{OPR}	Operating Temperature		0 to + 70	°C	1
T_{STG}	Storage Temperature		−55 to + 125	°C	1
P_D	Power Dissipation		1.6	W	1, 2
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Power is calculated using I_{DD5} @ 3.6Volt and −360 speed.

Recommended DC Operating Conditions (T_A= 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	3.0	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	−0.3	0.0	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Organization 8Mx64 Max	Units
C_{I1}	Input Capacitance (A0 - A9, A10/AP, A11, BA0,BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	53	pF
C_{I2}	Input Capacitance (CKE, CKE0)	49	pF
C_{I3}	Input Capacitance ($\overline{S}$0)	50	pF
C_{I4}	Input Capacitance (CK0, CK1)	38	pF
C_{I5}	Input Capacitance (DQMB0 - DQMB7)	9	pF
C_{I6}	Input Capacitance (SCL)	12	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63)	11	pF
C_{IO2}	Input/Output Capacitance (SDA)	15	pF

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DC Output Load Circuit

3.3 V

1200

Output

V_{OH} (DC) = 2.4V, I_{OH} = −2mA
V_{OL} (DC) = 0.4V, I_{OL} = 2mA

870

50pF
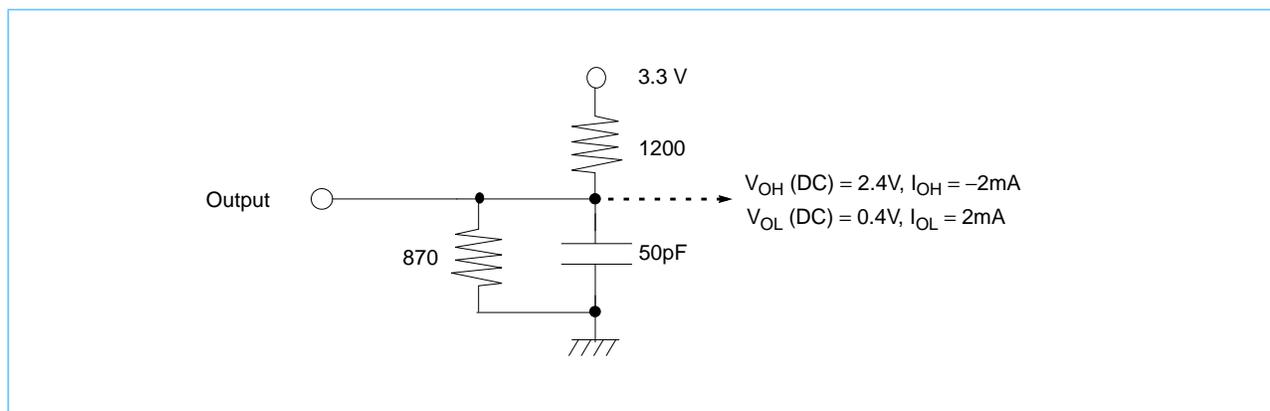
Output Characteristics $(T_A$= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter		8x64		Units	Notes
			Min.	Max.		
$I_{I(L)}$	Input Leakage Current, any input $(0.0V \leq V_{IN} \leq V_{DD})$, All Other Pins Not Under Test = 0V	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0, CK0, A0-A9, A10/AP, A11, BA0, BA1	−16	+16	µA	
		$\overline{S0}$	−16	+16		
		DQMB0-7	−2	+2		
		DQ0 - 63	−2	+2		
		SCL, SDA	−2	+2		
$I_{O(L)}$	Output Leakage Current $(D_{OUT}$ is disabled, $0.0V \leq V_{OUT} \leq V_{DD})$	DQ0 - 63, SDA	−2	+2	µA	
V_{OH}	Output Level (LVTTL) Output "H" Level Voltage $(I_{OUT} = -2.0mA)$		2.4	—	V	1
V_{OL}	Output Level (LVTTL) Output "L" Level Voltage $(I_{OUT} = +2.0mA)$		—	0.4		

1. See DC output load circuit.

Operating, Standby and Refresh Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Parameter	Symbol	Test Condition		Units	Notes
Operating Current t_{RC} = t_{RC}(min), t_{CK} = min Active-Precharge command cycling without Burst operation	I_{DD1}	1 bank operation	440	mA	1, 2
Precharge Standby Current in Power Down Mode	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{S}0$, $\overline{S}1$ =V_{IH}(min)	8	mA	
	I_{DD2Ps}	CKE ≤ V_{IL}(max), t_{CK} = Infinity, $\overline{S}0$, $\overline{S}1$ =V_{IH}(min)	8	mA	
Precharge Standby Current in Non-Power Down Mode	I_{DD2N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{S}0$, $\overline{S}1$ =V_{IH} (min)	200	mA	3
	I_{DD2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity, $\overline{S}0$, $\overline{S}1$ =V_{IH} (min)	40	mA	4
No Operating Current (Active state: 4 bank)	I_{DD3N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{S}0$, $\overline{S}1$ =V_{IH} (min)	240	mA	3
	I_{DD3P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{S}0$, $\overline{S}1$ =V_{IH} (min) (Power Down Mode)	56	mA	5
Burst Operating Current	I_{DD4}	t_{CK} = min, Read/ Write command cycling	720	mA	2, 6
Auto (CBR) Refresh Current	I_{DD5}	t_{CK} = min, CBR command cycling	880	mA	
Self Refresh Current	I_{DD6}	CKE0 ≤ 0.2V	3.2	mA	
Serial PD Device Standby Current	I_{SB5}	V_{IN} = GND or V_{DD}	30	μA	7
Serial PD Device Active Power Supply Current	I_{CCA}	SCL Clock Frequency = 100KHz	1	mA	8

1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
2. The specified values are obtained with the output open.
3. Input signals are changed once during three clock cycles.
4. Input signals are stable.
5. Active Standby current will be higher if Clock Suspend is entered during a Burst Read cycle (add 1mA per DQ).
6. Input signals are changed once during t_{CK}(min).
7. V_{DD} = 3.3V.
8. Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9, input rise and fall times 10ns, input and output timing levels V_{DD} x 0.5, output load 1 TTL gate and CL = 100pf.

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AC Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 200µs, with DQMB0-7 and CKE0 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
3. In addition to meeting the transition rate specification, the CK0, CK2, and CKE0 signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. Load Circuit A: AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.40V crossover point.
5. Load Circuit A: AC measurements assume t_T=1.0 ns.
6. Load Circuit B: AC timing tests have V_{IL} = 0.8 V and V_{IH} = 2.0 V with the timing referenced to the 1.40V crossover point.
7. Load Circuit B: AC measurements assume t_T=1.2 ns.

AC Characteristics Diagrams

AC Output Load Circuit (A)

AC Output Load Circuit (B)
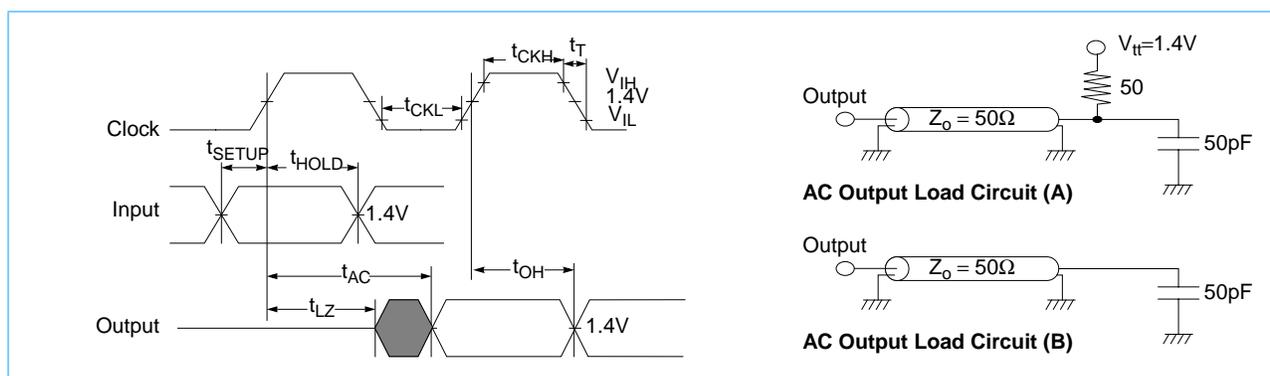
Clock and Clock Enable Parameters

Symbol	Parameter	−10		Units	Notes
		Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	10	1000	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	15	1000	ns	
$t_{AC3 (A)}$	Clock Access Time, $\overline{CAS}$ Latency = 3	—	7	ns	1
$t_{AC2 (A)}$	Clock Access Time, $\overline{CAS}$ Latency = 2	—	8	ns	1
$t_{AC3 (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 3	—	9	ns	2
$t_{AC2 (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 2	—	9	ns	2
t_{CKH}	Clock High Pulse Width	3	—	ns	3
t_{CKL}	Clock Low Pulse Width	3	—	ns	3
t_{CES}	Clock Enable Setup Time	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	ns	
t_{SB}	Power down mode Entry Time	0	10	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	ns	

1. Access time is measured at 1.4V. In AC Characteristics section, see notes 1, 2, 3, 4, and 5, and load circuit A.
2. Access time is measured at 1.4V. In AC Characteristics section, see notes 1, 2, 3, 6, and 7, and load circuit B.
3. t_{CKH} is the pulse width of CK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Common Parameters

Symbol	Parameter	−10		Units	Notes
		Min.	Max.		
t_{CS}	Command Setup Time	3	—	ns	
t_{CH}	Command Hold Time	1	—	ns	
t_{AS}	Address and Bank Select Setup Time	3	—	ns	
t_{AH}	Address and Bank Select Hold Time	1	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	ns	1
t_{RC}	Bank Cycle Time	90		ns	1
t_{RAS}	Active Command Period	60	100000	ns	1
t_{RP}	Precharge Time	30	—	ns	1
t_{RRD}	Bank to Bank Delay Time	20	—	ns	1
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	—	CK	

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	−10		Units	Notes
		Min.	Max.		
t_{RSC}	Mode Register Set Cycle Time	20	—	ns	1

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	−10		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0	—	ns	
t_{HZ3}	Data Out to High Impedance Time	3	7	ns	1
t_{HZ2}	Data Out to High Impedance Time	3	8	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	CK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

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Refresh Cycle

Symbol	Parameter	Units	Notes
t_{REF}	Refresh Period	ms	1
t_{SREX}	Self Refresh Exit Time	ns	

1. 4096 cycles.

Write Cycle

Symbol	Parameter	−10		Units
		Min.	Max.	
t_{DS}	Data In Setup Time	3	—	ns
t_{DH}	Data In Hold Time	1	—	ns
t_{DPL3}	Data input to Precharge, CL=3	10	—	ns
t_{DPL2}	Data input to Precharge, CL=2	15	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	CK

Presence Detect Read and Write Cycle

Symbol	Parameter	Min.	Max.	Units	Notes
f_{SCL}	SCL Clock Frequency		100	kHz	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs	
t_{LOW}	Clock Low Period	4.7		µs	
t_{HIGH}	Clock High Period	4.0		µs	
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_r	SDA and SCL Rise Time		1	µs	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

1. The Write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal Erase/Program cycle. During the Write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

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Clock Frequency and Latency

Symbol	Parameter	\-10		Units
f_{CK}	Clock Frequency	100	66	MHz
t_{CK}	Clock Cycle Time	10	15	ns
t_{AA}	$\overline{CAS}$ Latency	3	2	CK
t_{RP}	Precharge Time	3	2	CK
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	3	2	CK
t_{RC}	Bank Cycle Time	9	6	CK
t_{RAS}	Minimum Bank Active Time	6	4	CK
t_{DPL}	Data In to Precharge	1	1	CK
t_{DAL}	Data In to Active/Refresh	4	3	CK
t_{RRD}	Bank to Bank Delay Time	2	2	CK
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	1	CK
t_{WL}	Write Latency	0	0	CK
t_{DQW}	DQM Write Mask Latency	0	0	CK
t_{DQZ}	DQM Data Disable Latency	2	2	CK
t_{CSL}	Clock Suspend Latency	1	1	CK

Functional Description and Timing Diagrams

Refer to the IBM 64Mb Synchronous DRAM data sheet, document 19L3264.E35855A, for the functional description and timing diagrams for SDRAM operation.

Refer to the IBM Application Notes: *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

All AC timing information refers to the timings at the SDRAM devices.

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Layout Drawing (IBM13T8644HPB)
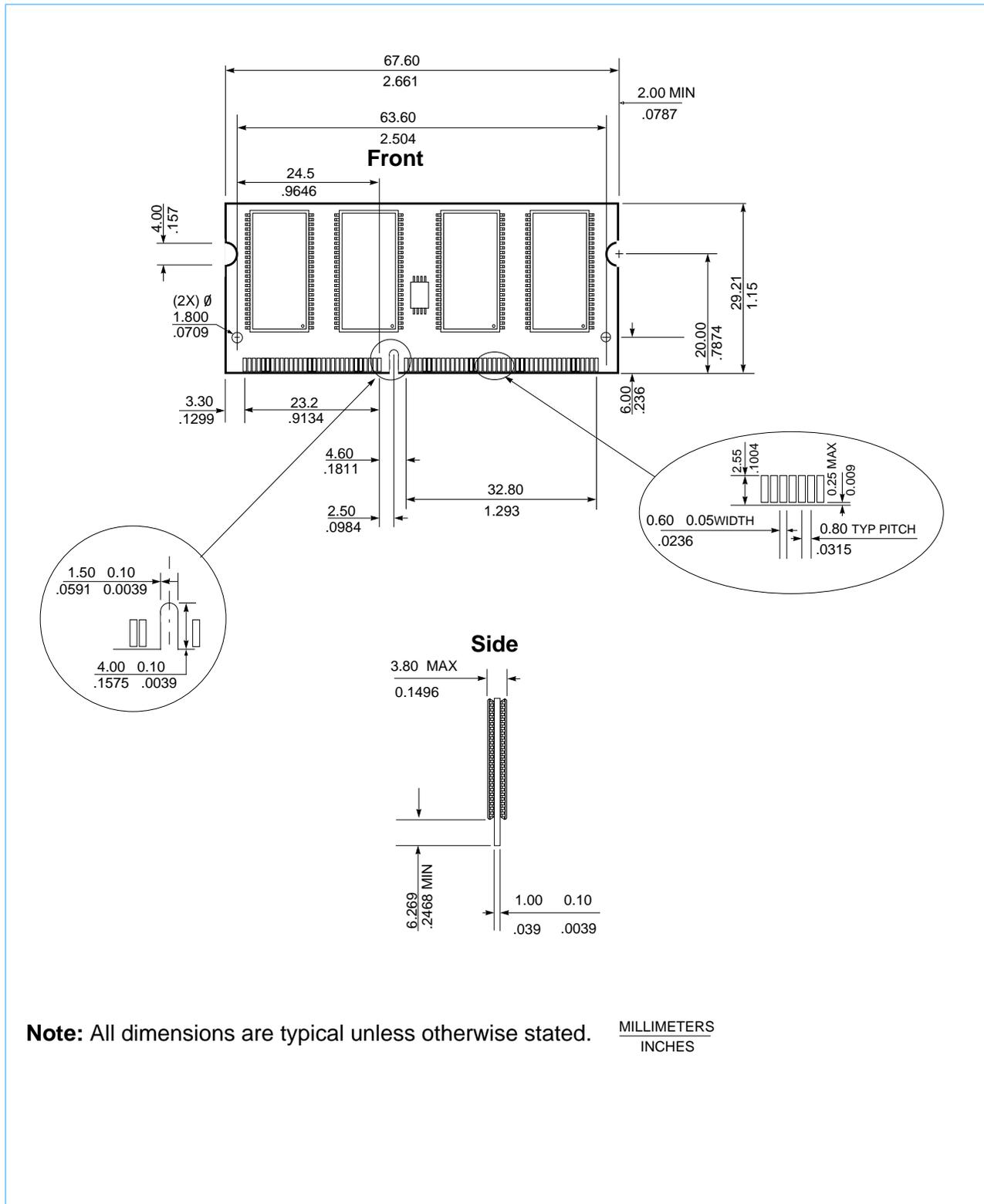
Note: All dimensions are typical unless otherwise stated.

$$\frac{\text{MILLIMETERS}}{\text{INCHES}}$$

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Layout Drawing (IBM13T8644HPC)

Front

Side

Note: All dimensions are typical unless otherwise stated.

$$\frac{MILLIMETERS}{INCHES}$$
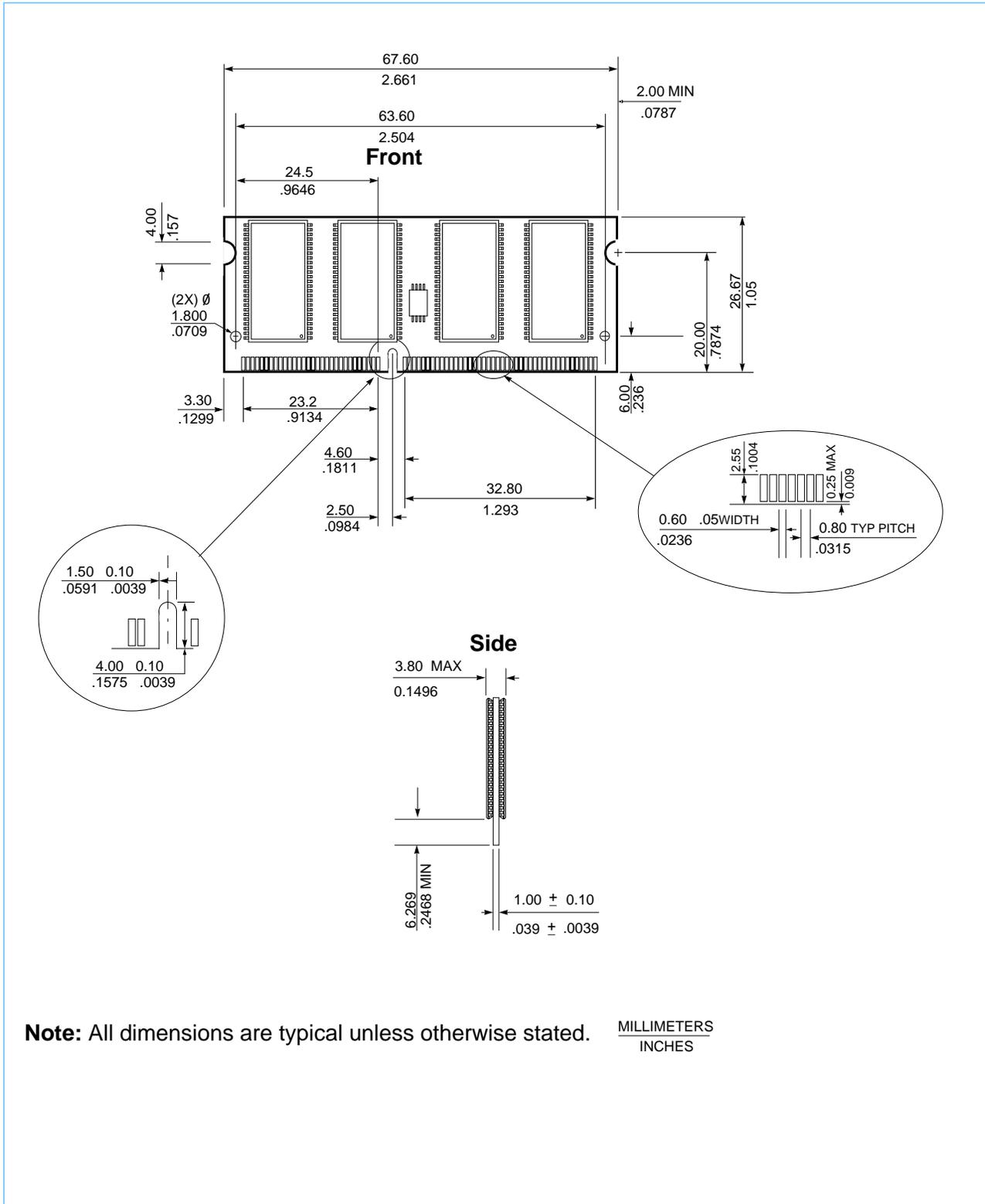
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Revision Log

Rev	Contents of Modification
4/98	Initial release.
6/98	Changes to leakage current, IDD3P, clock access to reflect changes to SDRAM specification. Updated Serial Presence Detect table with SPD rev2 data.
8/98	Add -360 speed, change DQ capacitance to 9pf, add clock frequency and latency table. Remove IBM13T8644HC Standard Power SO DIMM.
9/98	Add IBM13T8644HPC - 1.05" card height; fix typo on page 7; byte #32 added −360/−10 designation. Corrected typo's in Operating, Standby and Refresh Current notes & numbering.
3/99	Change I_{CC2P}, I_{CC2PS}, I_{CC3P}, I_{CC5}; Change DQ Capacitance.
5/99	Changed line 127 in Serial Presence Detect Table.

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