Am29LV640MT/B

Data Sheet

RETIRED PRODUCT

This product has been retired and is not available for designs. For new and current designs, S29GL064A supersedes Am29LV640MT/B and is the factory-recommended migration path. Please refer to the S29GL064A datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

Publication Number **26190** Revision **C** Amendment **8** Issue Date **February 1, 2007**

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DATA SHEET

Am29LV640MT/B

64 Megabit (4 M x 16-Bit/8 M x 8-Bit) MirrorBit™ 3.0 Volt-only Boot Sector Flash Memory

This product has been retired and is not available for designs. For new and current designs, S29GL064A supersedes Am29LV640M T/B and is the factory-recommended migration path. Please refer to the S29GL064A datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 3 V for read, erase, and program operations
- **Manufactured on 0.23 µm MirrorBit process technology**
- **Secured Silicon Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - Can be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - One hundred twenty-seven 32 Kword/64-Kbyte sectors
  - Eight 4 Kword/8 Kbyte boot sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - 90 ns access time
  - 25 ns page read times
  - 0.5 s typical sector erase time
  - 22 µs typical effective write buffer word programming time: 16-word/32-byte write buffer reduces overall programming time for multiple-word/byte updates
  - 4-word/8-byte page read buffer
  - 16-word/32-byte write buffer
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 30 mA typical active read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- **Package options**
  - 48-pin TSOP
  - 63-ball Fine-pitch BGA
  - 64-ball Fortified BGA

SOFTWARE & HARDWARE FEATURES

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Sector Group Protection: hardware-level method of preventing write operations within a sector group
  - Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
  - WP#/ACC input:
    Write Protect input (WP#) protects top or bottom two sectors regardless of sector protection settings
    ACC (high voltage) accelerates programming time for higher throughput during system production
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) indicates program or erase cycle completion

Publication# **26190** Rev: **C** Amendment/**8**
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GENERAL DESCRIPTION

The Am29LV640M is a 64 Mbit, 3.0 volt single power supply flash memory device organized as 4,194,304 words or 8,388,608 bytes. The device has an 8-bit/16-bit bus and can be programmed either in the host system or in standard EPROM programmers.

An access time of 90, 100, 110, or 120 ns is available. Note that each access time has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in Product Selector Guide on page 6 and Ordering Information on page 10. The device is offered in a 48-pin TSOP, 63-ball Fine-pitch BGA or 64-ball Fortified BGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** function provides shorter programming times through increased current on the WP#/ACC input. This feature is intended to facilitate factory throughput during system production, but can also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This is achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin can be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **Write Protect (WP#)** feature protects the top or bottom two sectors by asserting a logic low on the WP#/ACC pin. The protected sector is still protected even during accelerated programming.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

MIRRORBIT 64 MBIT DEVICE FAMILY

Device	Bus	Sector Architecture	Packages	V_{IO}	RY/BY#	WP#, ACC	WP# Protection
LV065MU	x8	Uniform (64 Kbyte)	48-pin TSOP (std. & rev. pinout), 63-ball FBGA	Yes	Yes	ACC only	No WP#
LV640MT/B	x8/x16	Boot (8 x 8 Kbyte at top & bottom)	48-pin TSOP, 63-ball Fine-pitch BGA, 64-ball Fortified BGA	No	Yes	WP#/ACC pin	2 x 8 Kbyte top or bottom
LV640MH/L	x8/x16	Uniform (64 Kbyte)	56-pin TSOP (std. & rev. pinout), 64-ball Fortified BGA	Yes	Yes	WP#/ACC pin	1 x 64 Kbyte high or low
LV641MH/L	x16	Uniform (32 Kword)	48-pin TSOP (std. & rev. pinout)	Yes	No	Separate WP# and ACC pins	1 x 32 Kword top or bottom
LV640MU	x16	Uniform (32 Kword)	64-ball Fortified BGA, 63-ball Fine-pitch BGA	Yes	Yes	ACC only	No WP#

RELATED DOCUMENTS

To download related documents, click on the following links or go to www.amd.com→Flash Memory→Product Information→MirrorBit→Flash Information→Technical Documentation.

MirrorBit™ Flash Memory Write Buffer Programming and Page Buffer Read

Implementing a Common Layout for AMD MirrorBit and Intel StrataFlash Memory Devices

Migrating from Single-byte to Three-byte Device IDs

AMD MirrorBit™ White Paper

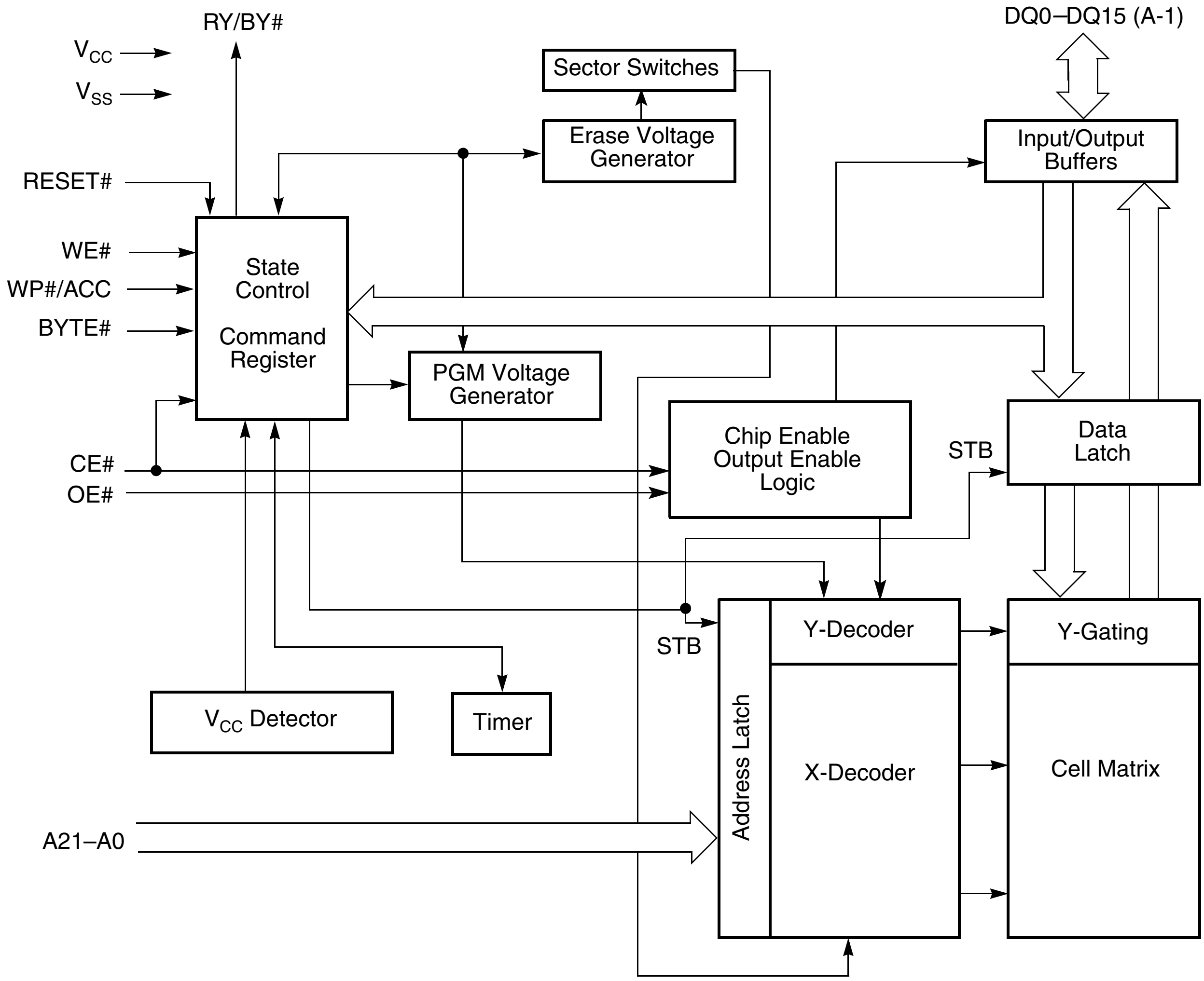
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

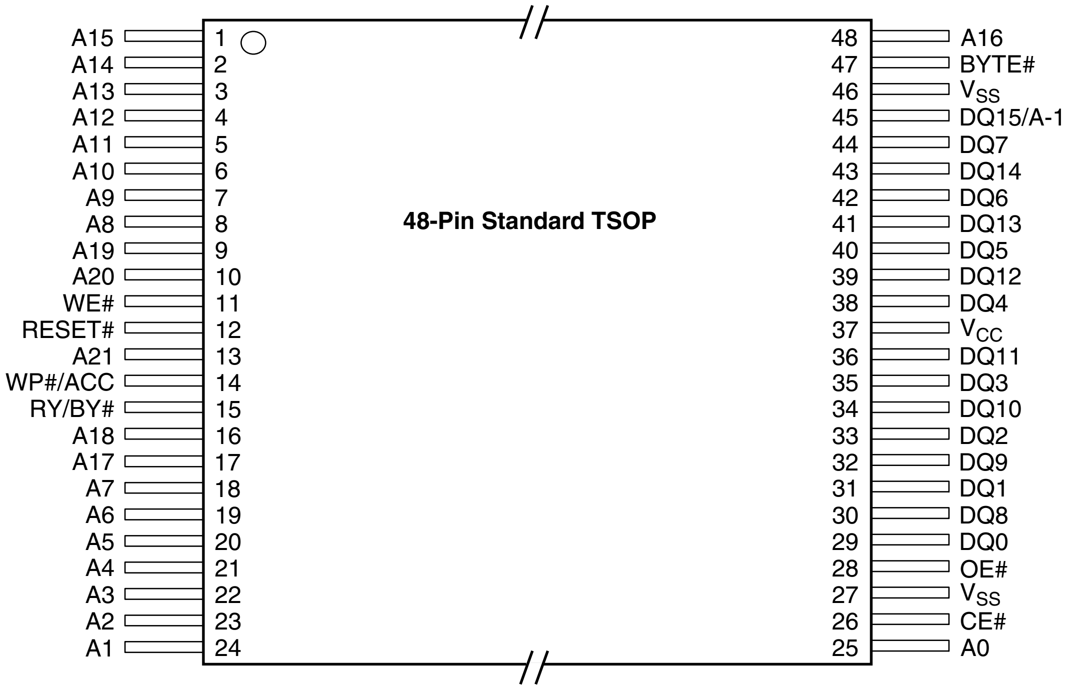
Part Number		Am29LV640M					
Speed Option	V_{CC} = 3.0–3.6 V	**90R**	**100R**	**110R**		**120R**	
	V_{CC} = 2.7–3.6 V		**100**		**110**		**120**
Max. Access Time (ns)		90	100	110		120	
Max. CE# Access Time (ns)		90	100	110		120	
Max. Page access time (t_{PACC})		25	30	30	40	30	40
Max. OE# Access Time (ns)		25	30	30	40	30	40

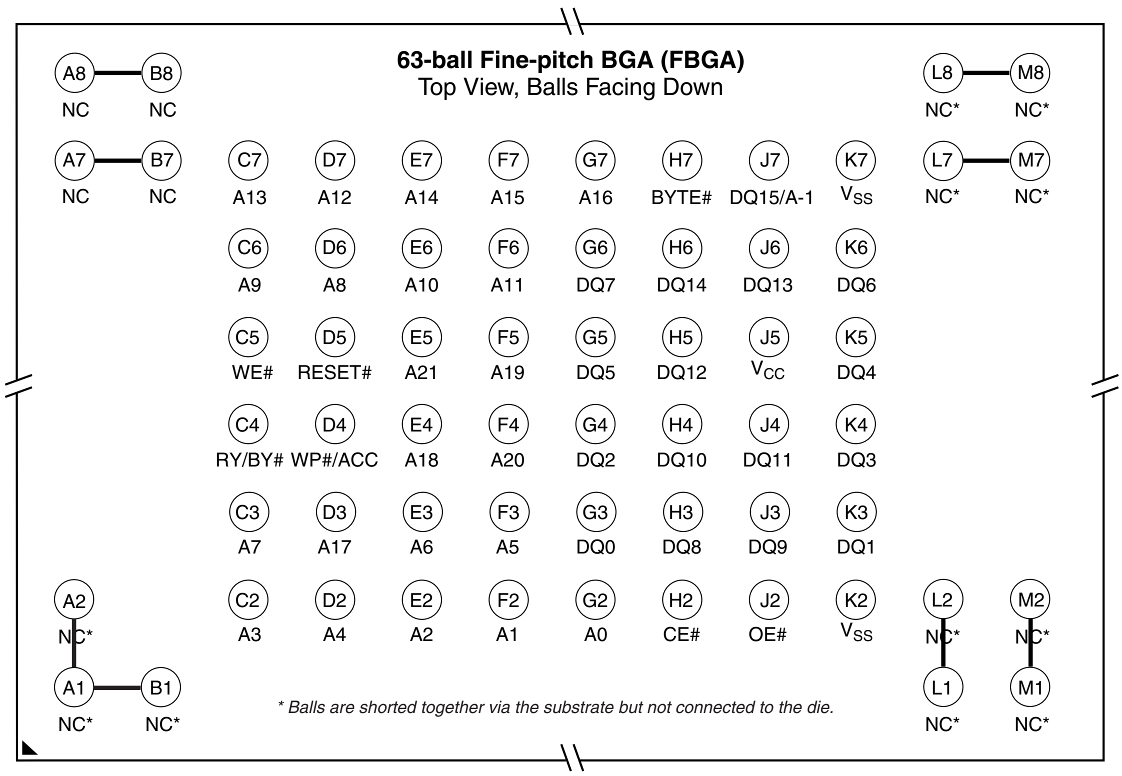
Note:
See AC Characteristics on page 45 for full specifications.

BLOCK DIAGRAM



CONNECTION DIAGRAMS





CONNECTION DIAGRAMS

64-Ball Fortified BGA (fBGA)
Top View, Balls Facing Down

A8 NC	B8 NC	C8 NC	D8 NC	E8 V_{SS}	F8 NC	G8 NC	H8 NC
A7 A13	B7 A12	C7 A14	D7 A15	E7 A16	F7 BYTE#	G7 DQ15/A-1	H7 V_{SS}
A6 A9	B6 A8	C6 A10	D6 A11	E6 DQ7	F6 DQ14	G6 DQ13	H6 DQ6
A5 WE#	B5 RESET#	C5 A21	D5 A19	E5 DQ5	F5 DQ12	G5 V_{CC}	H5 DQ4
A4 RY/BY#	B4 WP#/ACC	C4 A18	D4 A20	E4 DQ2	F4 DQ10	G4 DQ11	H4 DQ3
A3 A7	B3 A17	C3 A6	D3 A5	E3 DQ0	F3 DQ8	G3 DQ9	H3 DQ1
A2 A3	B2 A4	C2 A2	D2 A1	E2 A0	F2 CE#	G2 OE#	H2 V_{SS}
A1 NC	B1 NC	C1 NC	D1 NC	E1 NC	F1 NC	G1 NC	H1 NC

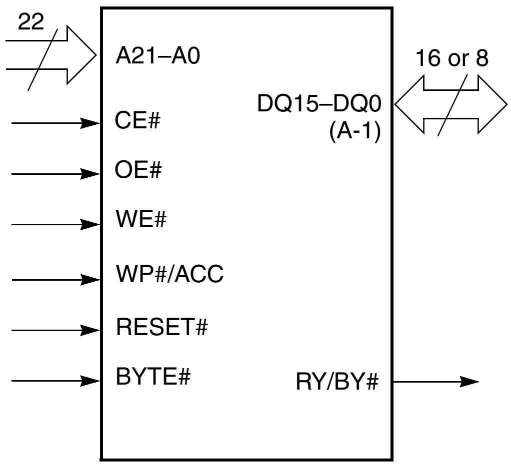
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP and BGA). The package and/or data integrity can be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A21–A0	=	22 Address inputs
DQ14–DQ0	=	15 Data inputs/outputs
DQ15/A-1	=	DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
WP#/ACC	=	Hardware Write Protect input/Programming Acceleration input
RESET#	=	Hardware Reset Pin input
RY/BY#	=	Ready/Busy output
BYTE#	=	Selects 8-bit or 16-bit mode
V_{CC}	=	3.0 volt-only single power supply (See Product Selector Guide on page 6 for speed options and voltage supply tolerances.)
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29LV640M T 120R PC I

TEMPERATURE RANGE
F = Industrial (-40°C to +85°C) with Pb-free Package
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
PC = 64-Ball Fortified Ball Grid Array
1.0 mm pitch, 13 x 11 mm package (LAA064)
WH = 63-Ball Fine Pitch Ball Grid Array
0.80 mm pitch, 12 x 11 mm package (FBE063)

SPEED OPTION
See Product Selector Guide and Valid Combinations

SECTOR ARCHITECTURE AND WP# PROTECTION (WP# = V_{IL})
T = Top boot sector device, top two address sectors protected
B = Bottom boot sector device, bottom two address sectors protected

DEVICE NUMBER/DESCRIPTION
Am29LV640M
64 Megabit (4 M x 16-Bit/8 M x 8-Bit) MirrorBit™ Boot Sector Flash Memory
3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP Package		Speed (ns)	V_{CC} Range
Am29LV640MT90R, Am29LV640MB90R	EI EF	90	3.0–3.6 V
Am29LV640MT100, Am29LV640MB100		100	2.7–3.6 V
Am29LV640MT110, Am29LV640MB110		110	
Am29LV640MT120, Am29LV640MB120		120	
Am29LV640MT100R, Am29LV640MB100R		100	3.0–3.6 V
Am29LV640MT110R, Am29LV640MB110R		110	
Am29LV640MT120R, Am29LV640MB120R		120	

Valid Combinations for BGA Packages						Speed (ns)	V_{CC} Range
Order Number		Package Marking	Order Number		Package Marking		
Am29LV640MT90R	WHI	L640MT90RI	Am29LV640MT90R	WHF	L640MT90RF	90	3.0–3.6 V
	PCI	L640MT90NI		PCF	L640MT90NF		
Am29LV640MB90R	WHI	L640MB90RI	Am29LV640MB90R	WHF	L640MB90RF		
	PCI	L640MB90NI		PCF	L640MB90NF		
Am29LV640MT100	WHI	L640MT10VI	Am29LV640MT100	WHF	L640MT10VF	100	2.7–3.6 V
	PCI	L640MT10PI		PCF	L640MT10PF		
Am29LV640MB100	WHI	L640MB10VI	Am29LV640MB100	WHF	L640MB10VF		
	PCI	L640MB10PI		PCF	L640MB10PF		
Am29LV640MT110	WHI	L640MT11VI	Am29LV640MT110	WHF	L640MT11VF	110	
	PCI	L640MT11PI		PCF	L640MT11PF		
Am29LV640MB110	WHI	L640MB11VI	Am29LV640MB110	WHF	L640MB11VF		
	PCI	L640MB11PI		PCF	L640MB11PF		
Am29LV640MT120	WHI	L640MT12VI	Am29LV640MT120	WHF	L640MT12VF	120	
	PCI	L640MT12PI		PCF	L640MT12PF		
Am29LV640MB120	WHI	L640MB12VI	Am29LV640MB120	WHF	L640MB12VF		
	PCI	L640MB12PI		PCF	L640MB12PF		
Am29LV640MT100R	WHI	L640MT10RI	Am29LV640MT100R	WHF	L640MT10RF	100	3.0–3.6 V
	PCI	L640MT10NI		PCF	L640MT10NF		
Am29LV640MB100R	WHI	L640MB10RI	Am29LV640MB100R	WHF	L640MB10RF		
	PCI	L640MB10NI		PCF	L640MB10NF		
Am29LV640MT110R	WHI	L640MT11RI	Am29LV640MT110R	WHF	L640MT11RF	110	
	PCI	L640MT11NI		PCF	L640MT11NF		
Am29LV640MB110R	WHI	L640MB11RI	Am29LV640MB110R	WHF	L640MB11RF		
	PCI	L640MB11NI		PCF	L640MB11NF		
Am29LV640MT120R	WHI	L640MT12RI	Am29LV640MT120R	WHF	L640MT12RF	120	
	PCI	L640MT12NI		PCF	L640MT12NF		
Am29LV640MB120R	WHI	L640MB12RI	Am29LV640MB120R	WHF	L640MB12RF		
	PCI	L640MB12NI		PCF	L640MB12NF		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	ACC	Addresses (Note 2)	DQ0–DQ7	DQ8–DQ15	
									BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	(Note 3)	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6 =L, A3=L, A2=L, A1=H, A0=L	(Note 4)	X	X
Sector Group Unprotect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 4)	X	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	X	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A21:A0 in word mode; A21:A-1 in byte mode. Sector addresses are A21:A12 in both modes.*
2. *The sector protect and sector unprotect functions can also be implemented via programming equipment. See the See Sector Group Protection and Unprotection on page 20.*
3. *If WP# = V_{IL}, the first or last sector remains protected. If WP# = V_{IH}, the top two or bottom two sectors are protected or unprotected as determined by the method described in Sector Group Protection and Unprotection. All sectors are unprotected when shipped from the factory (The Secured Silicon Sector can be factory protected depending on version ordered.)*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0–DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See See Reading Array Data on page 27 for more information. See the table, Read-Only Operations on page 45 for timing specifications and to Figure 14 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8 bytes. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 in word mode (A1–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The Word/Byte Program Command Sequence on page 29 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 and Table 3 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. AC Characteristics on page 45 contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system to write a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See Write Buffer on page 12 for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage can result. In addition, no external pullup is necessary since the WP#/ACC pin has internal pullup to V_{CC}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. See Autoselect Mode on page 19 and Autoselect Command Sequence on page 28 for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

See the table in DC Characteristics on page 43 for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the DC Characteristics table for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. To ensure data integrity, reinitiate the operation that was interrupted, once the device is ready to accept another command sequence.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current is greater.

The RESET# pin can be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 16 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29LV640MT Top Boot Sector Architecture

Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	0000000xxx	64/32	000000h–00FFFFh	00000h–07FFFh
SA1	0000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh
SA2	0000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh
SA3	0000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
SA4	0000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh
SA5	0000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
SA6	0000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh
SA7	0000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
SA8	0001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
SA9	0001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh
SA10	0001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
SA11	0001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
SA12	0001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
SA13	0001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
SA14	0001101xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
SA15	0001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh
SA16	0010000xxx	64/32	100000h–00FFFFh	80000h–87FFFh
SA17	0010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh
SA18	0010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh
SA19	0010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
SA20	0010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
SA21	0010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
SA22	0010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
SA23	0010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
SA24	0011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
SA25	0011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
SA26	0011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh

Table 2. Am29LV640MT Top Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA27	0011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
SA28	0011000xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
SA29	0011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
SA30	0011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
SA31	0011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
SA32	0100000xxx	64/32	200000h–20FFFFh	F9000h–107FFFh
SA33	0100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	0100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	0101011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA36	0100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	0100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA41	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA43	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	0101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	0110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	0110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	0100100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA53	0110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	0110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	0110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	0111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	0111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	0111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	0111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	0111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	0111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	0111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	0111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh
SA64	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh
SA65	1000001xxx	64/32	410000h–41FFFFh	208000h–20FFFFh
SA66	1000010xxx	64/32	420000h–42FFFFh	210000h–217FFFh
SA67	1000011xxx	64/32	430000h–43FFFFh	218000h–21FFFFh
SA68	1000100xxx	64/32	440000h–44FFFFh	220000h–227FFFh
SA69	1000101xxx	64/32	450000h–45FFFFh	228000h–22FFFFh
SA70	1000110xxx	64/32	460000h–46FFFFh	230000h–237FFFh
SA71	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh
SA72	1001000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
SA73	1001001xxx	64/32	490000h–49FFFFh	248000h–24FFFFh
SA74	1001010xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
SA75	1001011xxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
SA76	1001100xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
SA77	1001101xxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
SA78	1001110xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
SA79	1001111xxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
SA80	1010000xxx	64/32	500000h–50FFFFh	280000h–28FFFFh
SA81	1010001xxx	64/32	510000h–51FFFFh	288000h–28FFFFh

Table 2. Am29LV640MT Top Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA82	1010010xxx	64/32	520000h–52FFFFh	290000h–297FFFh
SA83	1010011xxx	64/32	530000h–53FFFFh	298000h–29FFFFh
SA84	1010100xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
SA85	1010101xxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
SA86	1010110xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
SA87	1010111xxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
SA88	1011000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
SA89	1011001xxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
SA90	1011010xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
SA91	1011011xxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
SA92	1011100xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
SA93	1011101xxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
SA94	1011110xxx	64/32	5E0000h–5EFFFFh	2F0000h–2FFFFFh
SA95	1011111xxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
SA96	1100000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
SA97	1100001xxx	64/32	610000h–61FFFFh	308000h–30FFFFh
SA98	1100010xxx	64/32	620000h–62FFFFh	310000h–317FFFh
SA99	1100011xxx	64/32	630000h–63FFFFh	318000h–31FFFFh
SA100	1100100xxx	64/32	640000h–64FFFFh	320000h–327FFFh
SA101	1100101xxx	64/32	650000h–65FFFFh	328000h–32FFFFh
SA102	1100110xxx	64/32	660000h–66FFFFh	330000h–337FFFh
SA103	1100111xxx	64/32	670000h–67FFFFh	338000h–33FFFFh
SA104	1101000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
SA105	1101001xxx	64/32	690000h–69FFFFh	348000h–34FFFFh
SA106	1101010xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh
SA107	1101011xxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh
SA108	1101100xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh
SA109	1101101xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
SA110	1101110xxx	64/32	6E0000h–6EFFFFh	370000h–377FFFh
SA111	1101111xxx	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
SA112	1110000xxx	64/32	700000h–70FFFFh	380000h–387FFFh
SA113	1110001xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
SA114	1110010xxx	64/32	720000h–72FFFFh	390000h–397FFFh
SA115	1110011xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
SA116	1110100xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
SA117	1110101xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
SA118	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA119	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA120	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA121	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA122	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA123	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA124	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA125	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA126	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA127	1111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
SA128	1111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
SA129	1111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
SA130	1111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
SA131	1111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
SA132	1111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
SA133	1111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
SA134	1111111111	8/4	7FE000h–7FFFFFh	3FF000h–3FFFFFh

Table 3. Am29LV640MB Bottom Boot Sector Architecture

Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	0000000000	8/4	000000h–001FFFh	00000h–00FFFh
SA1	0000000001	8/4	002000h–003FFFh	01000h–01FFFh
SA2	0000000010	8/4	004000h–005FFFh	02000h–02FFFh
SA3	0000000011	8/4	006000h–007FFFh	03000h–03FFFh
SA4	0000000100	8/4	008000h–009FFFh	04000h–04FFFh
SA5	0000000101	8/4	00A000h–00BFFFh	05000h–05FFFh
SA6	0000000110	8/4	00C000h–00DFFFh	06000h–06FFFh
SA7	0000000111	8/4	00E000h–00FFFFFh	07000h–07FFFh
SA8	0000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh
SA9	0000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh
SA10	0000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
SA11	0000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh
SA12	0000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
SA13	0000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh
SA14	0000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
SA15	0001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
SA16	0001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh
SA17	0001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
SA18	0001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
SA19	0001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
SA20	0001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
SA21	0001101xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
SA22	0001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh
SA23	0010000xxx	64/32	100000h–00FFFFh	80000h–87FFFh
SA24	0010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh
SA25	0010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh
SA26	0010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
SA27	0010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
SA28	0010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
SA29	0010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
SA30	0010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
SA31	0011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
SA32	0011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
SA33	0011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh
SA34	0011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
SA35	0011000xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
SA36	0011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
SA37	0011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
SA38	0011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
SA39	0100000xxx	64/32	200000h–20FFFFh	F9000h–107FFFh
SA40	0100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA41	0100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA42	0101011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA43	0100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA44	0100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA45	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA46	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA47	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA48	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA49	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA50	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA51	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA52	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA53	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh

Table 3. Am29LV640MB Bottom Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA54	0101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA55	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA56	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA57	0110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA58	0110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA59	0100100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA60	0110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA61	0110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA62	0110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA63	0111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA64	0111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA65	0111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA66	0111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA67	0111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA68	0111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA69	0111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA70	0111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh
SA71	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh
SA72	1000001xxx	64/32	410000h–41FFFFh	208000h–20FFFFh
SA73	1000010xxx	64/32	420000h–42FFFFh	210000h–217FFFh
SA74	1000011xxx	64/32	430000h–43FFFFh	218000h–21FFFFh
SA75	1000100xxx	64/32	440000h–44FFFFh	220000h–227FFFh
SA76	1000101xxx	64/32	450000h–45FFFFh	228000h–22FFFFh
SA77	1000110xxx	64/32	460000h–46FFFFh	230000h–237FFFh
SA78	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh
SA79	1001000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
SA80	1001001xxx	64/32	490000h–49FFFFh	248000h–24FFFFh
SA81	1001010xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
SA82	1001011xxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
SA83	1001100xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
SA84	1001101xxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
SA85	1001110xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
SA86	1001111xxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
SA87	1010000xxx	64/32	500000h–50FFFFh	280000h–28FFFFh
SA88	1010001xxx	64/32	510000h–51FFFFh	288000h–28FFFFh
SA89	1010010xxx	64/32	520000h–52FFFFh	290000h–297FFFh
SA90	1010011xxx	64/32	530000h–53FFFFh	298000h–29FFFFh
SA91	1010100xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
SA92	1010101xxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
SA93	1010110xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
SA94	1010111xxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
SA95	1011000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
SA96	1011001xxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
SA97	1011010xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
SA98	1011011xxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
SA99	1011100xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
SA100	1011101xxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
SA101	1011110xxx	64/32	5E0000h–5EFFFFh	2F0000h–2FFFFFh
SA102	1011111xxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
SA103	1100000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
SA104	1100001xxx	64/32	610000h–61FFFFh	308000h–30FFFFh
SA105	1100010xxx	64/32	620000h–62FFFFh	310000h–317FFFh
SA106	1100011xxx	64/32	630000h–63FFFFh	318000h–31FFFFh
SA107	1100100xxx	64/32	640000h–64FFFFh	320000h–327FFFh
SA108	1100101xxx	64/32	650000h–65FFFFh	328000h–32FFFFh

Table 3. Am29LV640MB Bottom Boot Sector Architecture (Continued)

Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA109	1100110xxx	64/32	660000h–66FFFFh	330000h–337FFFh
SA110	1100111xxx	64/32	670000h–67FFFFh	338000h–33FFFFh
SA111	1101000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
SA112	1101001xxx	64/32	690000h–69FFFFh	348000h–34FFFFh
SA113	1101010xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh
SA114	1101011xxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh
SA115	1101100xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh
SA116	1101101xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
SA117	1101110xxx	64/32	6E0000h–6EFFFFh	370000h–377FFFh
SA118	1101111xxx	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
SA119	1110000xxx	64/32	700000h–70FFFFh	380000h–387FFFh
SA120	1110001xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
SA121	1110010xxx	64/32	720000h–72FFFFh	390000h–397FFFh
SA122	1110011xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
SA123	1110100xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
SA124	1110101xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
SA125	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA126	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA127	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA128	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA129	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA130	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA131	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA132	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA133	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA134	1111111000	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Note: *The address range is A21:A-1 in byte mode (BYTE# = V_{IL}) or A21:A0 in word mode (BYTE# = V_{IH})*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device programmed with its corresponding programming algorithm. However, the autoselect codes can be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A3, A2, A1, and A0 must be set as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 2 and 3). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment can then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12 and Table 13. This method does not require V_{ID}. See Autoselect Command Sequence on page 28 for more information.

Table 4. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A21 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15 BYTE# = V_{IH}	DQ8 to DQ15 BYTE# = V_{IL}	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h
Device ID	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	10h
	Cycle 3										H	H	H	22	X	00 (bottom boot) 01h (top boot)
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects top two address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	98h (factory locked), 18h (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects bottom two address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	88h (factory locked), 08h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Tables 5 and 6). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See Autoselect Mode on page 19

Table 5. Am29LV640MT Top Boot Sector Protection

Sector	A21–A12	Sector/ Sector Block Size
SA0-SA3	00000XXXXX	256 (4x64) Kbytes
SA4-SA7	00001XXXXX	256 (4x64) Kbytes
SA8-SA11	00010XXXXX	256 (4x64) Kbytes
SA12-SA15	00011XXXXX	256 (4x64) Kbytes
SA16-SA19	00100XXXXX	256 (4x64) Kbytes
SA20-SA23	00101XXXXX	256 (4x64) Kbytes
SA24-SA27	00110XXXXX	256 (4x64) Kbytes
SA28-SA31	00111XXXXX	256 (4x64) Kbytes
SA32-SA35	01000XXXXX	256 (4x64) Kbytes
SA36-SA39	01001XXXXX	256 (4x64) Kbytes
SA40-SA43	01010XXXXX	256 (4x64) Kbytes
SA44-SA47	01011XXXXX	256 (4x64) Kbytes
SA48-SA51	01100XXXXX	256 (4x64) Kbytes
SA52-SA55	01101XXXXX	256 (4x64) Kbytes
SA56-SA59	01110XXXXX	256 (4x64) Kbytes
SA60-SA63	01111XXXXX	256 (4x64) Kbytes
SA64-SA67	10000XXXXX	256 (4x64) Kbytes
SA68-SA71	10001XXXXX	256 (4x64) Kbytes
SA72-SA75	10010XXXXX	256 (4x64) Kbytes
SA76-SA79	10011XXXXX	256 (4x64) Kbytes
SA80-SA83	10100XXXXX	256 (4x64) Kbytes
SA84-SA87	10101XXXXX	256 (4x64) Kbytes
SA88-SA91	10110XXXXX	256 (4x64) Kbytes
SA92-SA95	10111XXXXX	256 (4x64) Kbytes
SA96-SA99	11000XXXXX	256 (4x64) Kbytes
SA100-SA103	11001XXXXX	256 (4x64) Kbytes
SA104-SA107	11010XXXXX	256 (4x64) Kbytes
SA108-SA111	11011XXXXX	256 (4x64) Kbytes
SA112-SA115	11100XXXXX	256 (4x64) Kbytes
SA116-SA119	11101XXXXX	256 (4x64) Kbytes
SA120-SA123	11110XXXXX	256 (4x64) Kbytes
SA124-SA126	1111100XXX 1111101XXX 1111110XXX	192 (3x64) Kbytes
SA127	1111111000	8 Kbytes
SA128	1111111001	8 Kbytes
SA129	1111111010	8 Kbytes
SA130	1111111011	8 Kbytes
SA131	1111111100	8 Kbytes
SA132	1111111101	8 Kbytes
SA133	1111111110	8 Kbytes
SA134	1111111111	8 Kbytes

Table 6. Am29LV640MB Bottom Boot Sector Protection

Sector	A21–A12	Sector/ Sector Block Size
SA0	0000000000	8 Kbytes
SA1	0000000001	8 Kbytes
SA2	0000000010	8 Kbytes
SA3	0000000011	8 Kbytes
SA4	0000000100	8 Kbytes
SA5	0000000101	8 Kbytes
SA6	0000000110	8 Kbytes
SA7	0000000111	8 Kbytes
SA8–SA10	0000001XXX, 0000010XXX, 0000011XXX,	192 (3x64) Kbytes
SA11–SA14	00001XXXXX	256 (4x64) Kbytes
SA15–SA18	00010XXXXX	256 (4x64) Kbytes
SA19–SA22	00011XXXXX	256 (4x64) Kbytes
SA23–SA26	00100XXXXX	256 (4x64) Kbytes
SA27-SA30	00101XXXXX	256 (4x64) Kbytes
SA31-SA34	00110XXXXX	256 (4x64) Kbytes
SA35-SA38	00111XXXXX	256 (4x64) Kbytes
SA39-SA42	01000XXXXX	256 (4x64) Kbytes
SA43-SA46	01001XXXXX	256 (4x64) Kbytes
SA47-SA50	01010XXXXX	256 (4x64) Kbytes
SA51-SA54	01011XXXXX	256 (4x64) Kbytes

Table 6. Am29LV640MB Bottom Boot Sector Protection (Continued)

Sector	A21–A12	Sector/ Sector Block Size
SA55–SA58	01100XXXXX	256 (4x64) Kbytes
SA59–SA62	01101XXXXX	256 (4x64) Kbytes
SA63–SA66	01110XXXXX	256 (4x64) Kbytes
SA67–SA70	01111XXXXX	256 (4x64) Kbytes
SA71–SA74	10000XXXXX	256 (4x64) Kbytes
SA75–SA78	10001XXXXX	256 (4x64) Kbytes
SA79–SA82	10010XXXXX	256 (4x64) Kbytes
SA83–SA86	10011XXXXX	256 (4x64) Kbytes
SA87–SA90	10100XXXXX	256 (4x64) Kbytes
SA91–SA94	10101XXXXX	256 (4x64) Kbytes
SA95–SA98	10110XXXXX	256 (4x64) Kbytes
SA99–SA102	10111XXXXX	256 (4x64) Kbytes
SA103–SA106	11000XXXXX	256 (4x64) Kbytes
SA107–SA110	11001XXXXX	256 (4x64) Kbytes
SA111–SA114	11010XXXXX	256 (4x64) Kbytes
SA115–SA118	11011XXXXX	256 (4x64) Kbytes
SA119–SA122	11100XXXXX	256 (4x64) Kbytes
SA123–SA126	11101XXXXX	256 (4x64) Kbytes
SA127–SA130	11110XXXXX	256 (4x64) Kbytes
SA131–SA134	11111XXXXX	256 (4x64) Kbytes

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the top two or bottom two sectors without using V_{ID}. WP# is one of two functions provided by the WP#/ACC input.

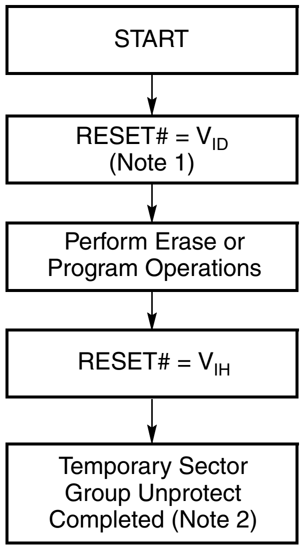
If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector independently of whether those sectors were protected or unprotected using the method described in Sector Group Protection and Unprotection. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in DC Characteristics.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the top or bottom two sectors were previously set to be protected or unprotected using the method described in Sector Group Protection and Unprotection. *Note: No external pullup is necessary since the WP#/ACC pin has internal pullup to* V_{CC}

Temporary Sector Group Unprotect

*(**Note:** In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 6).*

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sector groups unprotected (If WP# = V_{IL}, the first or last sector remain protected).*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

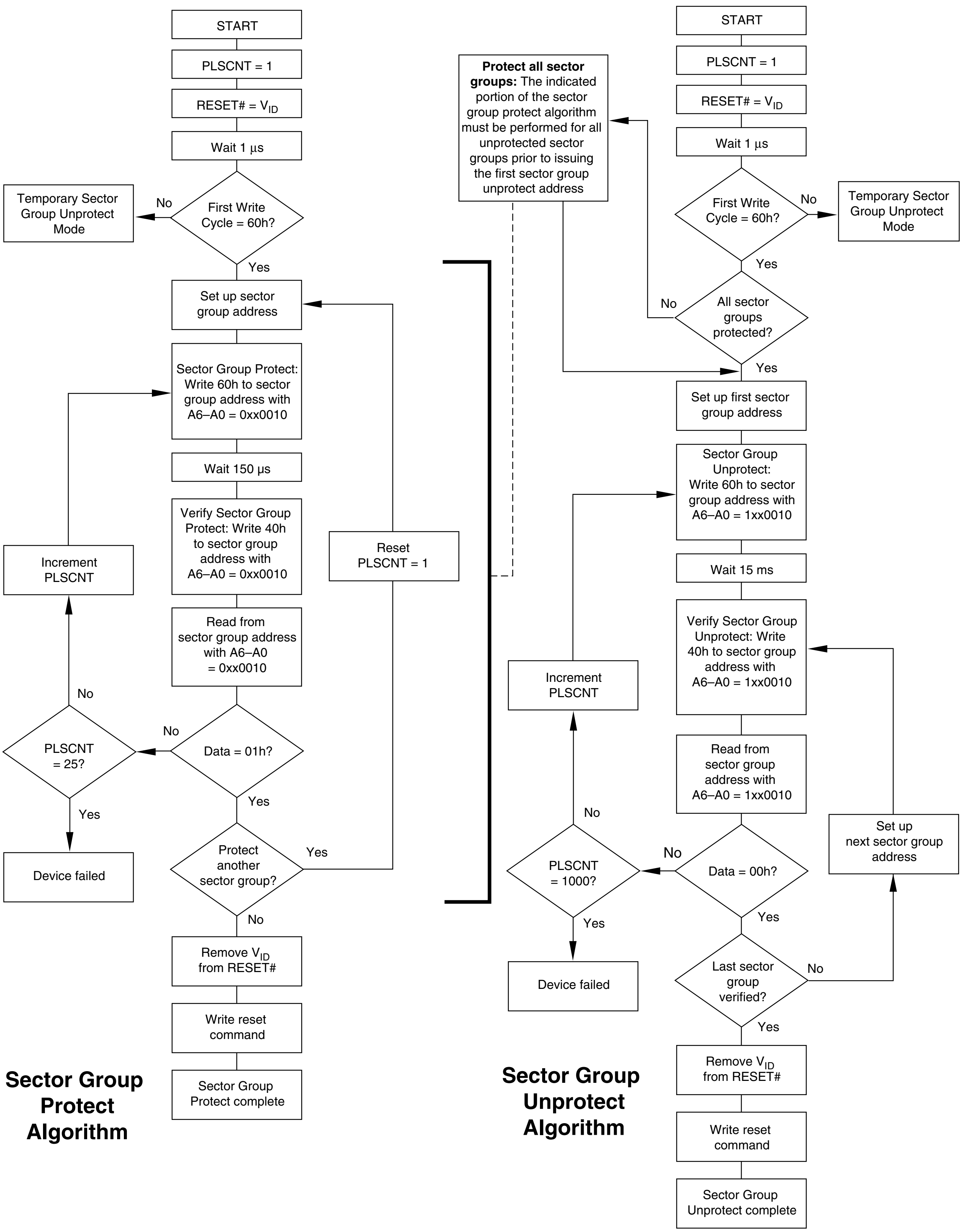


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 128 words/256 bytes in length, and uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the Secured Silicon Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a “1.” The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the Secured Silicon Sector Indicator Bit permanently set to a “0.” Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The Secured Silicon sector address space in this device is allocated as follows:

Table 7. Secured Silicon Sector Contents

Secured Silicon Sector Address Range		Standard Factory Locked	ExpressFlash Factory Locked	Customer Lockable
x16	x8			
000000h–000007h	000000h–00000Fh	ESN	ESN or determined by customer	Determined by customer
000008h–00007Fh	000010h–0000FFh	Unavailable	Determined by customer	

The system accesses the Secured Silicon Sector through a command sequence. See Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence on page 28 After the system has written the Enter Secured Silicon Sector command sequence, it can read the Secured Silicon Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

Factory Locked: Secured Silicon Sector Programmed and Protected At the Factory

In devices with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. See Table 7 for Secured Silicon Sector addressing.

Customers can opt to have their code programmed by AMD through the AMD ExpressFlash service. The devices are then shipped from AMD’s factory with the Secured Silicon Sector permanently locked. Contact an AMD representative for details on using AMD’s ExpressFlash service.

Customer Lockable: Secured Silicon Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device can be ordered such that the customer can program and protect the 128-word/256 bytes Secured Silicon sector.

The system can program the Secured Silicon Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions on page 27

Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# can be at either V_{IH} or V_{ID}.* This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 3.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing within the remainder of the array.

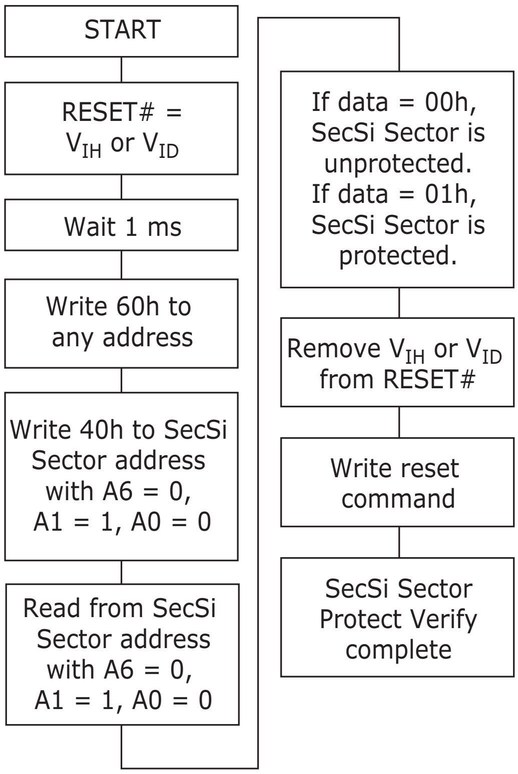


Figure 3. Secured Silicon Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 12 and 13 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8–11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8–11. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 8. CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9. System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0007h	Typical timeout per single byte/word write 2^N µs
20h	40h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0001h	Max. timeout for byte/word write 2^N times typical
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 10. Device Geometry Definition

Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	0017h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	007Fh 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	007Eh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 11. Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0008h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0010b = 0.23 µm MirrorBit
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	0002h/ 0003h	Top/Bottom Boot Sector Flag 00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Tables 12 and 13 define the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence can place the device in an unknown state. A reset command is then required to return the device to reading array data.*

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. See AC Characteristics on page 45 for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system can once again read array data with the same exception. See Erase Suspend/Erase Resume Commands on page 35 for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data on page 11 in Device Bus Operations for more information. See the table, Read-Only Operations on page 45 for the read parameters, and Figure 14 for the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command can be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command can be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command can be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to read several identifier codes at specific addresses:

Identifier Code	A7:A0 (x16)	A6:A-1 (x8)
Manufacturer ID	00h	00h
Device ID, Cycle 1	01h	02h
Device ID, Cycle 2	0Eh	1Ch
Device ID, Cycle 3	0Fh	1Eh
Secured Silicon Sector Factory Protect	03h	06h
Sector Protect Verify	(SA)02h	(SA)04h

Note: *The device ID is read over three cycles. SA = Sector Address*

Tables 12 and 13 show the address and data requirements. This method is an alternative to that shown in Table 4, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence can be written to an address that is either in the read or erase-suspend-read mode. The autoselect command cannot be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system can read at any address any number of times without initiating another autoselect command sequence.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Tables 12 and 13 show the address and data requirements for both command sequences. See also Secured Silicon Sector Flash Memory Region for further information.

Word/Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Tables 12 and 13 show the address and data requirements for the word program command sequence. *Note that the autoselect and CFI functions are unavailable when a program operation is in progress.*

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See Write Operation Status on page 38 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so can cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 12 and 13 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system programs six unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations can be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation aborts.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter is decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Also note, if an address location is loaded more than once into the buffer, the final data loaded for that address is programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

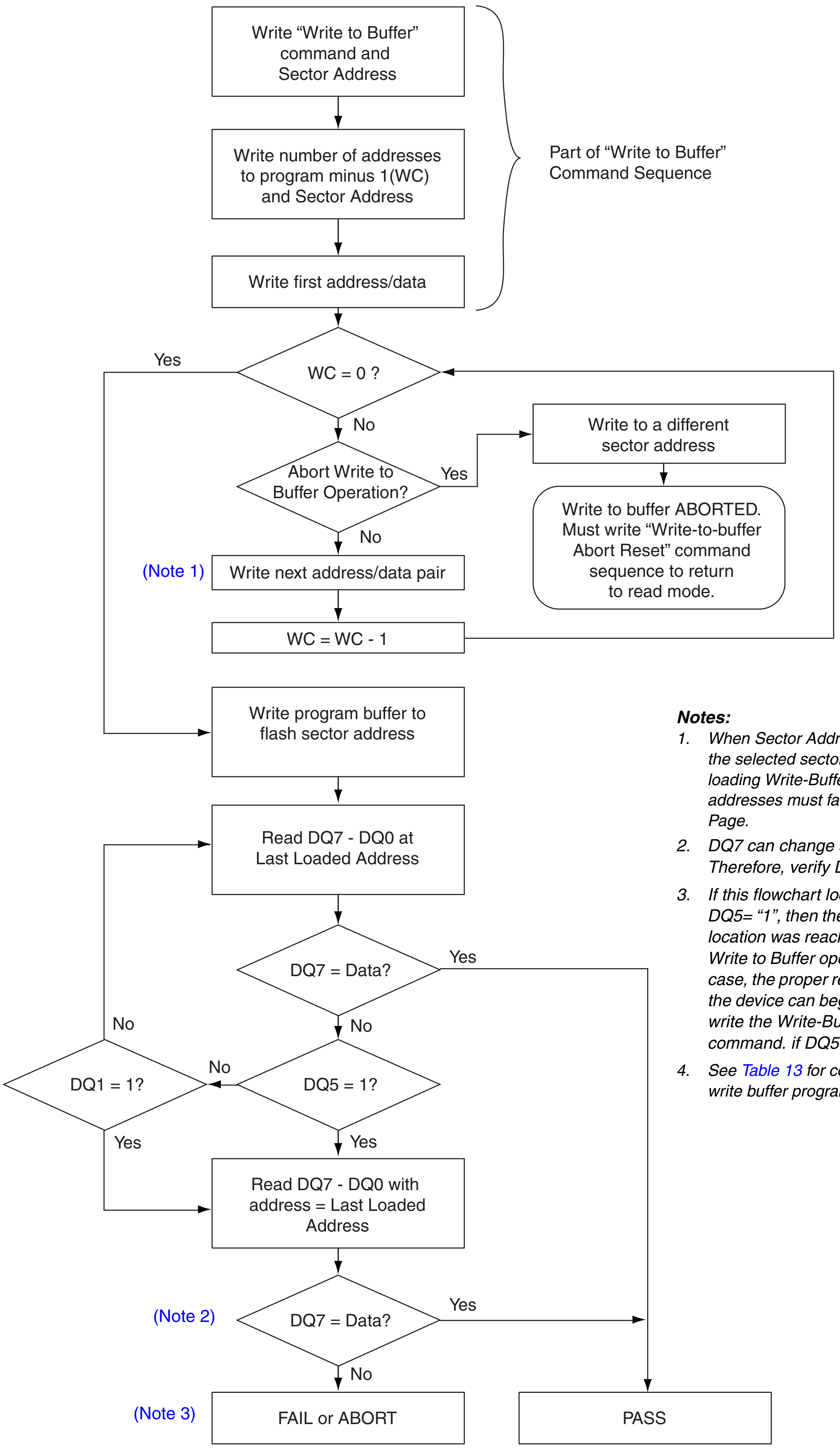
- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system can then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage can result. In addition, no external pullup is necessary since the WP#/ACC pin has internal pullup to V_{CC}.*

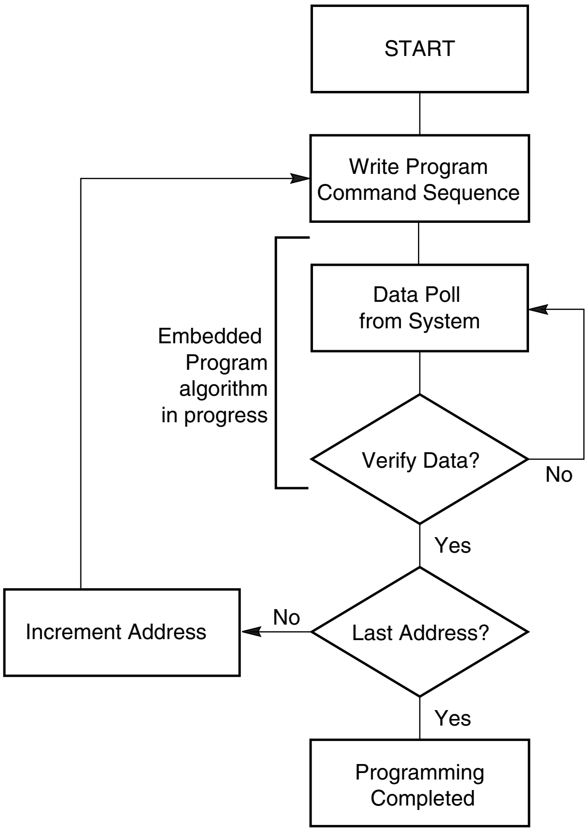
Figure 5 illustrates the algorithm for the program operation. See the table, Erase and Program Operations on page 48 in AC Characteristics for parameters, and Figure 17 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 can change simultaneously with DQ5. Therefore, verify DQ7 .*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must write before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Table 13 for command sequences required for write buffer programming.*

Figure 4. Write Buffer Programming Operation



Note: *See Table 13 for program command sequence.*

Figure 5. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command can also be issued during a programming operation while an erase is suspended. In this case, data can be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system can also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence on page 28 for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status on page 38 for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

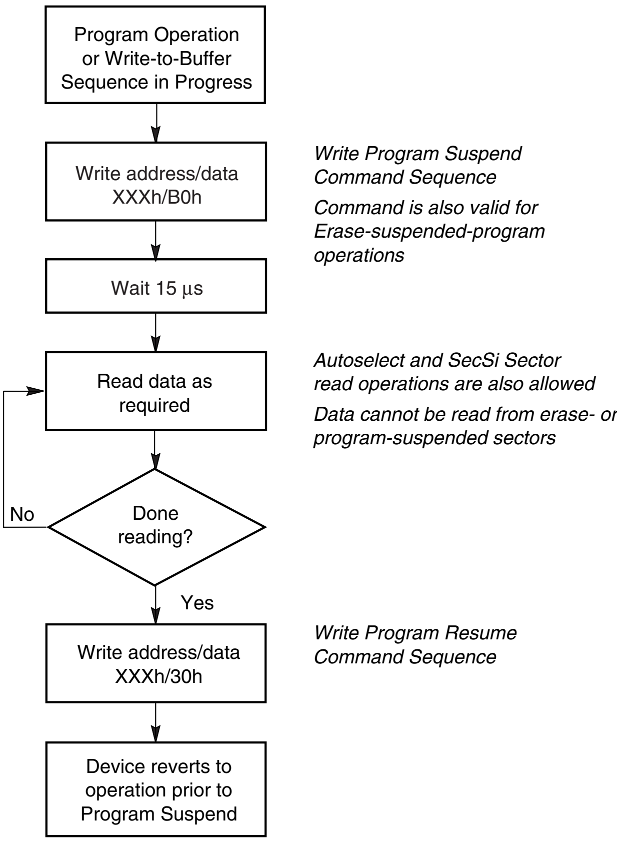


Figure 6. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Tables 12 and 13 shows the address and data requirements for the chip erase command sequence. *Note that the autoselect and CFI functions are unavailable when an erase operation is in progress.*

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See Write Operation Status on page 38 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 7 illustrates the algorithm for the erase operation. See the table, Erase and Program Operations on page 48 in AC Characteristics for parameters, and Figure 19 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Tables 12 and 13 shows the address and data requirements for the sector erase command sequence. *Note that the autoselect and CFI functions are unavailable when an erase operation is in progress.*

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

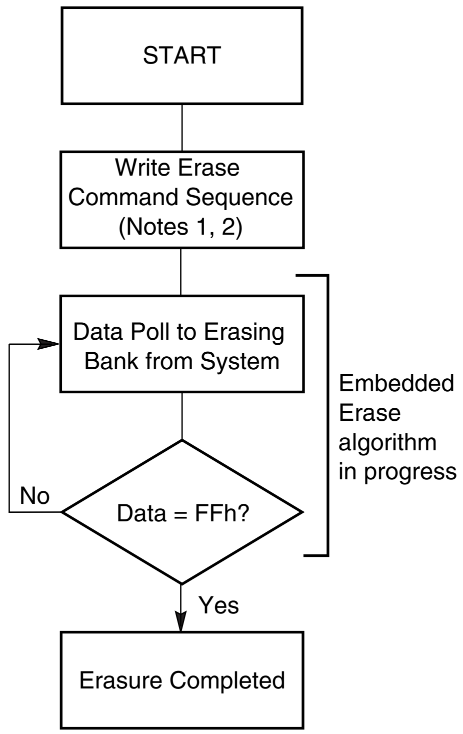
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands can be written. Loading the sector erase buffer can be done in any sequence, and the number of sectors can be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure can begin. Any sector erase address and command following the exceeded time-out might or might not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. See DQ3: Sector Erase Timer on page 41. The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. See Write Operation Status on page 38 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 7 illustrates the algorithm for the erase operation. See the table, Erase and Program Operations on page 48 in AC Characteristics for parameters, and Figure 19 for timing diagrams.



Notes:

1. *See Table 12 and Table 13 for erase command sequence.*
2. *See DQ3: Sector Erase Timer on page 41 for information on the sector erase timer.*

Figure 7. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See Write Operation Status on page 38 for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. See Write Operation Status on page 38 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. See Autoselect Mode on page 19 and Autoselect Command Sequence on page 28 for details.

To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Note: During an erase operation, this flash device performs multiple internal operations which are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if this flash device is continually issued suspend/resume commands in rapid succession, erase progress is impeded as a function of the number of suspends. The result is a longer cumulative erase time than without suspends. Note that the additional suspends do not affect device reliability or future performance. In most systems rapid erase/suspend activity occurs only briefly. In such cases, erase performance is not significantly impacted.

Command Definitions

Table 12. Command Definitions (x16 Mode, BYTE# = V_{IH})

	Command Sequence (Notes)	Cycles	Bus Cycles (Notes 1–4) First Addr	First Data	Second Addr	Second Data	Third Addr	Third Data	Fourth Addr	Fourth Data	Fifth Addr	Fifth Data	Sixth Addr	Sixth Data
	Read (Note 5)	1	RA	RD										
	Reset (Note 6)	1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
Autoselect (Note 7)	Device ID (Note 8)	6	555	AA	2AA	55	555	90	X01	227E	X0E	2210	X0F	2200/ 2201
Autoselect (Note 7)	Secured Silicon Sector Factory Protect (Note 9)	4	555	AA	2AA	55	555	90	X03	(Note 9)				
Autoselect (Note 7)	Sector Group Protect Verify (Note 10)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
	Enter Secured Silicon Sector Region	3	555	AA	2AA	55	555	88						
	Exit Secured Silicon Sector Region	4	555	AA	2AA	55	555	90	XXX	00				
	Program	4	555	AA	2AA	55	555	A0	PA	PD				
	Write to Buffer (Note 11)	6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
	Program Buffer to Flash	1	SA	29										
	Write to Buffer Abort Reset (Note 12)	3	555	AA	2AA	55	555	F0						
	Unlock Bypass	3	555	AA	2AA	55	555	20						
	Unlock Bypass Program (Note 13)	2	XXX	A0	PA	PD								
	Unlock Bypass Reset (Note 14)	2	XXX	90	XXX	00								
	Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Program/Erase Suspend (Note 15)	1	XXX	B0										
	Program/Erase Resume (Note 16)	1	XXX	30										
	CFI Query (Note 17)	1	55	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *During unlock cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when device is in read mode.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.*
7. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. Except RD, PD and WC. See Autoselect Command Sequence on page 28 for more information.*
8. *The device ID must be read in three cycles. The data is 2201h for top boot and 2200h for bottom boot.*
9. *If WP# protects the top two address sectors, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the bottom two address sectors, the data is 88h for factory locked and 08h for not factor locked.*
10. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
11. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21, including "Program Buffer to Flash" command.*
12. *Command sequence resets device for next command after aborted write-to-buffer operation.*
13. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
14. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
15. *The system can read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume command is valid only during the Erase Suspend mode.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

Table 13. Command Definitions (x8 Mode, BYTE# = V_{IL})

Command Sequence (Notes)	Cycles	Bus Cycles (Notes 1–4) First Addr	First Data	Second Addr	Second Data	Third Addr	Third Data	Fourth Addr	Fourth Data	Fifth Addr	Fifth Data	Sixth Addr	Sixth Data
Read (Note 5)	1	RA	RD										
Reset (Note 6)	1	XXX	F0										
Autoselect (Note 7): Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
Autoselect (Note 7): Device ID (Note 8)	6	AAA	AA	555	55	AAA	90	X02	7E	X1C	10	X1E	00/01
Autoselect (Note 7): Secured Silicon Sector Factory Protect (Note 9)	4	AAA	AA	555	55	AAA	90	X06	(Note 9)				
Autoselect (Note 7): Sector Group Protect Verify (Note 10)	4	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
Enter Secured Silicon Sector Region	3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector Region	4	AAA	AA	555	55	AAA	90	XXX	00				
Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (Note 11)	6	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash	1	SA	29										
Write to Buffer Abort Reset (Note 12)	3	AAA	AA	555	55	AAA	F0						
Unlock Bypass	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 13)	2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 14)	2	XXX	90	XXX	00								
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (Note 15)	1	XXX	B0										
Program/Erase Resume (Note 16)	1	XXX	30										
CFI Query (Note 17)	1	AA	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

BC = Byte Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *During unlock cycles, when lower address bits are 555 or AAAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when device is in read mode.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.*
7. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See Autoselect Command Sequence on page 28 for more information.*
8. *The device ID must be read in three cycles. The data is 01h for top boot and 00h for bottom boot*
9. *If WP# protects the top two address sectors, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the bottom two address sectors, the data is 88h for factory locked and 08h for not factor locked.*
10. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
11. *The total number of cycles in the command sequence is determined by the number of bytes written to the write buffer. The maximum number of cycles in the command sequence is 37, including "Program Buffer to Flash" command.*
12. *Command sequence resets device for next command after aborted write-to-buffer operation.*
13. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
14. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
15. *The system can read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume command is valid only during the Erase Suspend mode.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 14 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

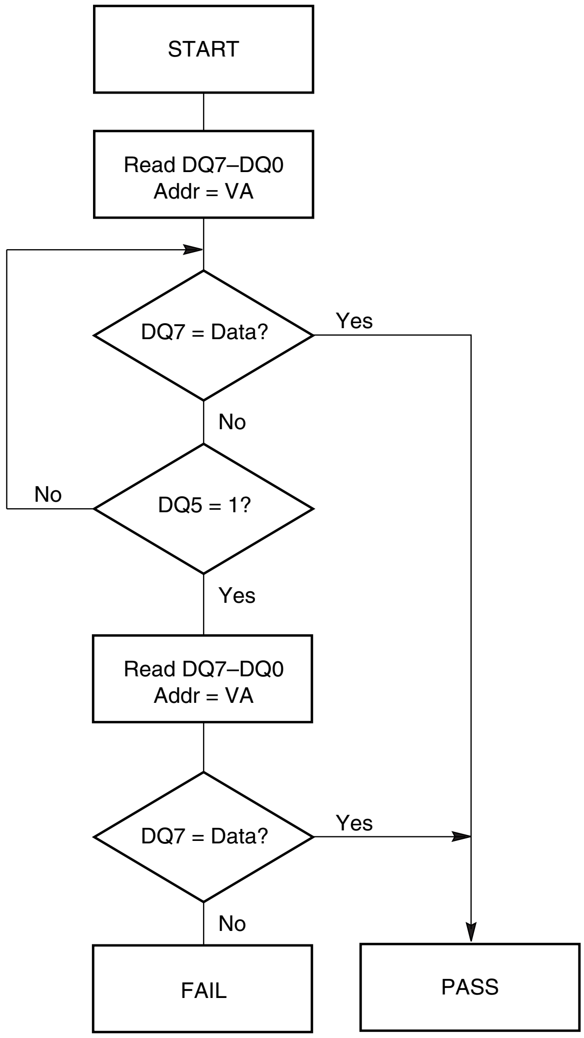
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status might not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 can change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device can change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it can read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 might be still invalid. Valid data on DQ0–DQ7 appears on successive read cycles.

Table 14 shows the outputs for Data# Polling on DQ7. Figure 8 shows the Data# Polling algorithm. Figure 20 in AC Characteristics shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *Recheck DQ7 even if DQ5 = “1” because DQ7 can change simultaneously with DQ5.*

Figure 8. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 14 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I can be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system can use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

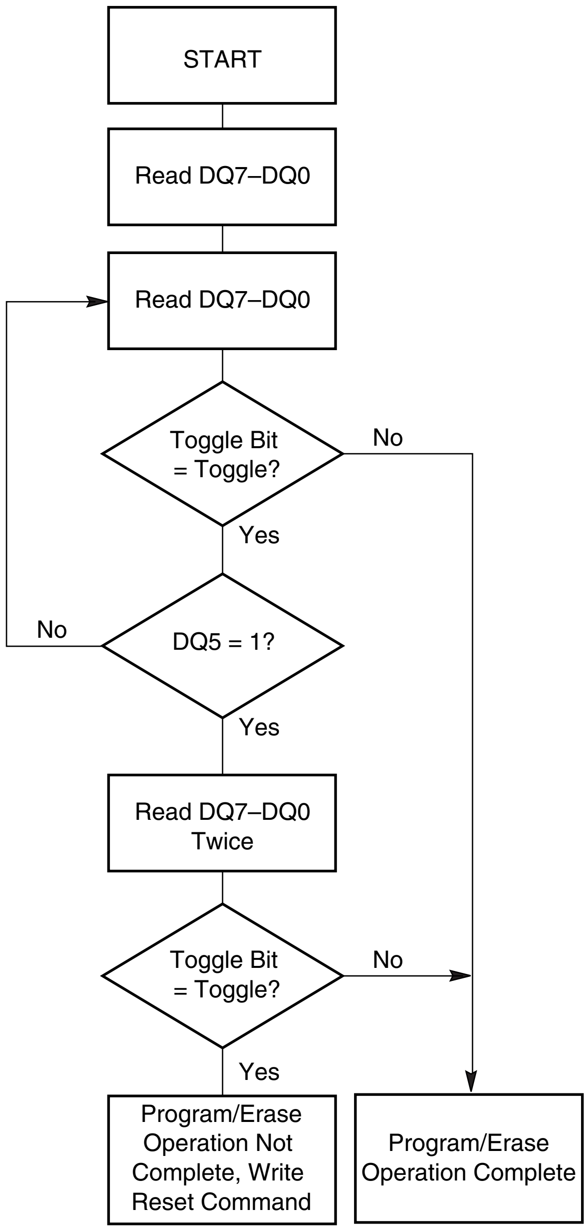
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7. See DQ7: Data# Polling on page 38).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 14 shows the outputs for Toggle Bit I on DQ6. Figure 9 shows the toggle bit algorithm. Figure 21 in AC Characteristics shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also DQ2: Toggle Bit II on page 40.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit can stop toggling as DQ5 changes to "1." See DQ6: Toggle Bit I and DQ2: Toggle Bit II for more information.*

Figure 9. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system can use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 14 to compare outputs for DQ2 and DQ6.

Figure 9 shows the toggle bit algorithm in flowchart form, and DQ2: Toggle Bit II on page 40 explains the algorithm. See also RY/BY#: Ready/Busy# on page 39. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 9 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high. (See DQ2: Toggle Bit II on page 40.) If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit might have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system can continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it can choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 9).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device might output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system can read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also Sector Erase Command Sequence on page 33 .

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device accepts additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 14 shows the status of DQ3 relative to the other status bits.

DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer Programming on page 29 for more details.

Table 14. Write Operation Status

<table>
<tr><th colspan="3">Status</th><th>DQ7 (Note 2)</th><th>DQ6</th><th>DQ5 (Note 1)</th><th>DQ3</th><th>DQ2 (Note 2)</th><th>DQ1</th><th>RY/BY#</th></tr>
<tr><td rowspan="2">Standard Mode</td><td colspan="2">Embedded Program Algorithm</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>No toggle</td><td>0</td><td>0</td></tr>
<tr><td colspan="2">Embedded Erase Algorithm</td><td>0</td><td>Toggle</td><td>0</td><td>1</td><td>Toggle</td><td>N/A</td><td>0</td></tr>
<tr><td rowspan="2">Program Suspend Mode</td><td rowspan="2">Program-Suspend Read</td><td>Program-Suspended Sector</td><td colspan="6">Invalid (not allowed)</td><td>1</td></tr>
<tr><td>Non-Program Suspended Sector</td><td colspan="6">Data</td><td>1</td></tr>
<tr><td rowspan="3">Erase Suspend Mode</td><td rowspan="2">Erase-Suspend Read</td><td>Erase-Suspended Sector</td><td>1</td><td>No toggle</td><td>0</td><td>N/A</td><td>Toggle</td><td>N/A</td><td>1</td></tr>
<tr><td>Non-Erase Suspended Sector</td><td colspan="6">Data</td><td>1</td></tr>
<tr><td colspan="2">Erase-Suspend-Program (Embedded Program)</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>N/A</td><td>N/A</td><td>0</td></tr>
<tr><td rowspan="2">Write-to-Buffer</td><td colspan="2">Busy (Note 3)</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>N/A</td><td>0</td><td>0</td></tr>
<tr><td colspan="2">Abort (Note 4)</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>N/A</td><td>1</td><td>0</td></tr>
</table>

Notes:

1. *DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to '1' when the device has aborted the write-to-buffer operation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . .–0.5 V to +4.0 V

V_{IO}. . . . .–0.5 V to +4.0 V

A9, OE#, ACC, and RESET#
(Note 2). . . . .–0.5 V to +12.5 V

All other pins (Note 1) . . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins can overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 10. During voltage transitions, input or I/O pins can overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 11.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# can overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 10. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which can overshoot to +14.0 V for periods up to 20 ns.*
3. *No more than one output can be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods can affect device reliability.

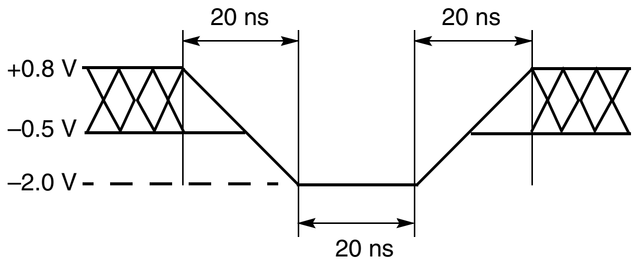


Figure 10. Maximum Negative Overshoot Waveform

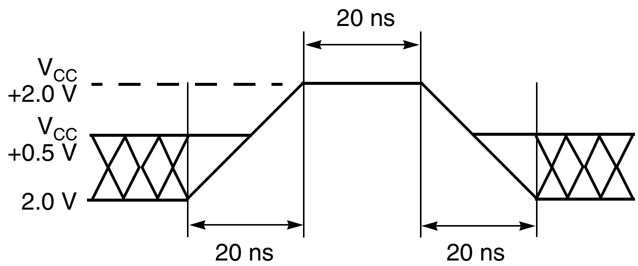


Figure 11. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Supply Voltages

V_{CC} for full voltage range . . . . 2.7–3.6 V

V_{CC} for regulated voltage range . . . . 3.0–3.6 V

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

DC CHARACTERISTICS

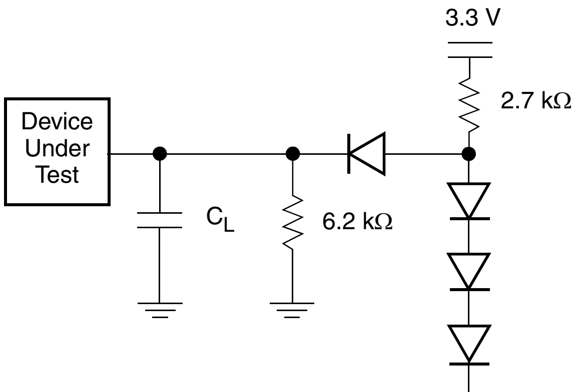
CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET= 12.5 V				35	µA
I_{CC1}	V_{CC} Active Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH},	5 MHz		15	20	mA
			1 MHz		15	20	
I_{CC2}	V_{CC} Initial Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}			30	50	mA
I_{CC3}	V_{CC} Intra-Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}			10	20	mA
I_{CC4}	V_{CC} Active Write Current (3, 4)	CE# = V_{IL}, OE# = V_{IH}			50	60	mA
I_{CC5}	V_{CC} Standby Current (3)	CE#, RESET# = $V_{CC} \pm 0.3$ V, WP# = V_{IH}			1	5	µA
I_{CC6}	V_{CC} Reset Current (3)	RESET# = $V_{SS} \pm 0.3$ V, WP# = V_{IH}			1	5	µA
I_{CC7}	Automatic Sleep Mode (3, 5)	$V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V, WP# = V_{IH}			1	5	µA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			1.9		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.15 x V_{CC}	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (6)			2.3		2.5	V

Notes:

1. *On the WP#/ACC pin only, the maximum input load current when WP# = V_{IL} is ± 5.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}max$.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
6. *Not 100% tested.*
7. *Includes RY/BY#*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

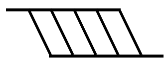
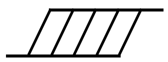
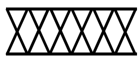
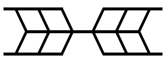
Figure 12. Test Setup

Table 15. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels (See Note)	1.5	V
Output timing measurement reference levels	0.5 V_{IO}	V

Note: *If $V_{IO} < V_{CC}$, the reference level is 0.5 V_{IO}.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Note: *If $V_{IO} < V_{CC}$, the input measurement reference level is 0.5 V_{IO}.*

Figure 13. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations

Parameter						Speed Options							
JEDEC	Std.	Description		Test Setup		90R	100R	100	110R	110,	120R	120	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	100		110		120		ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	90	100		110		120		ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	90	100		110		120		ns
	t_{PACC}	Page Access Time			Max	25	30		30	40	30	40	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	30		30	40	30	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16							ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16							ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0							ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0							ns
			Toggle and Data# Polling		Min	10							ns

Notes:

1. *Not 100% tested.*
2. *See Figure 12 and Table 15 for test specifications.*

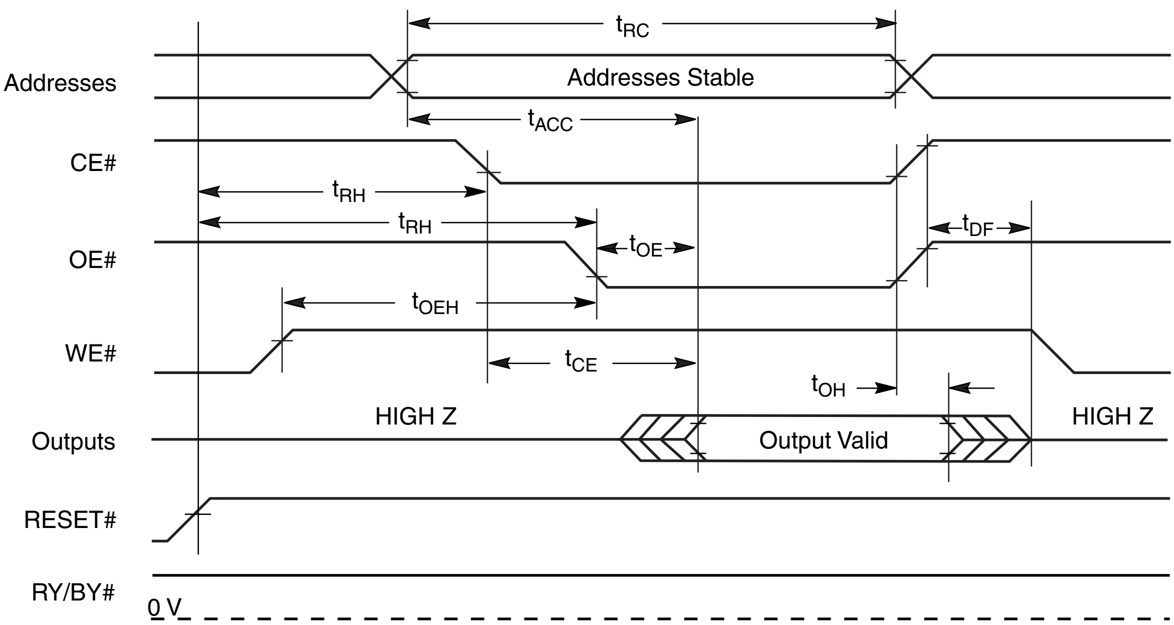
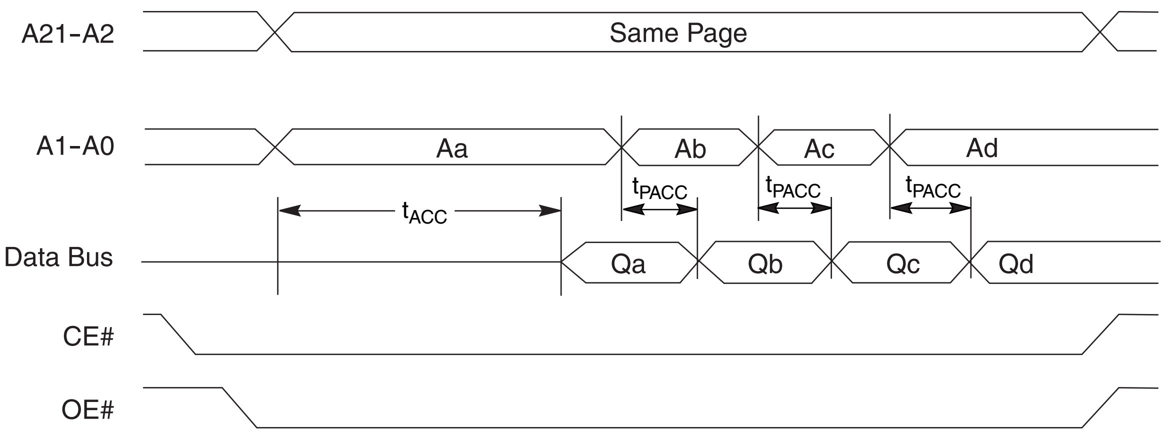


Figure 14. Read Operation Timings

AC CHARACTERISTICS



** Figure shows word mode. Addresses are A1–A-1 for byte mode.*

Figure 15. Page Read Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

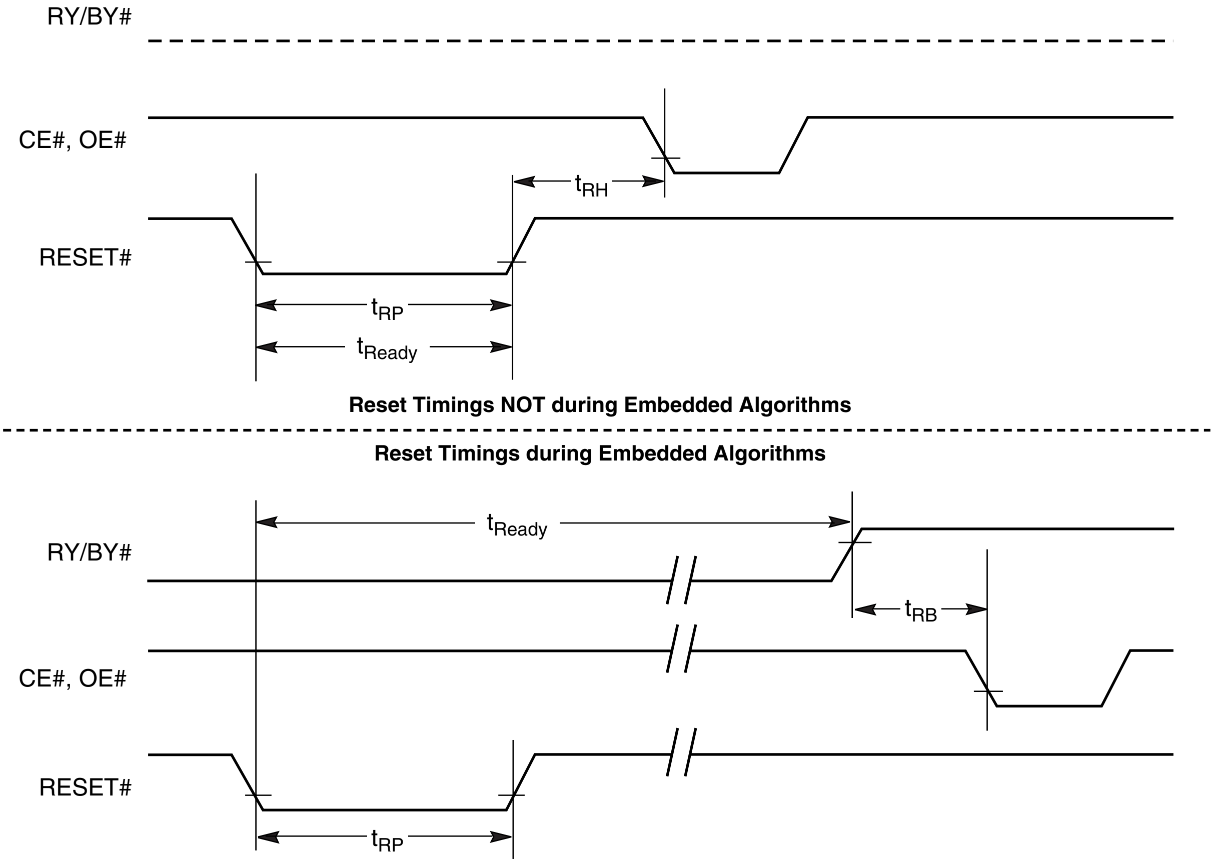


Figure 16. Reset Timings

AC CHARACTERISTICS

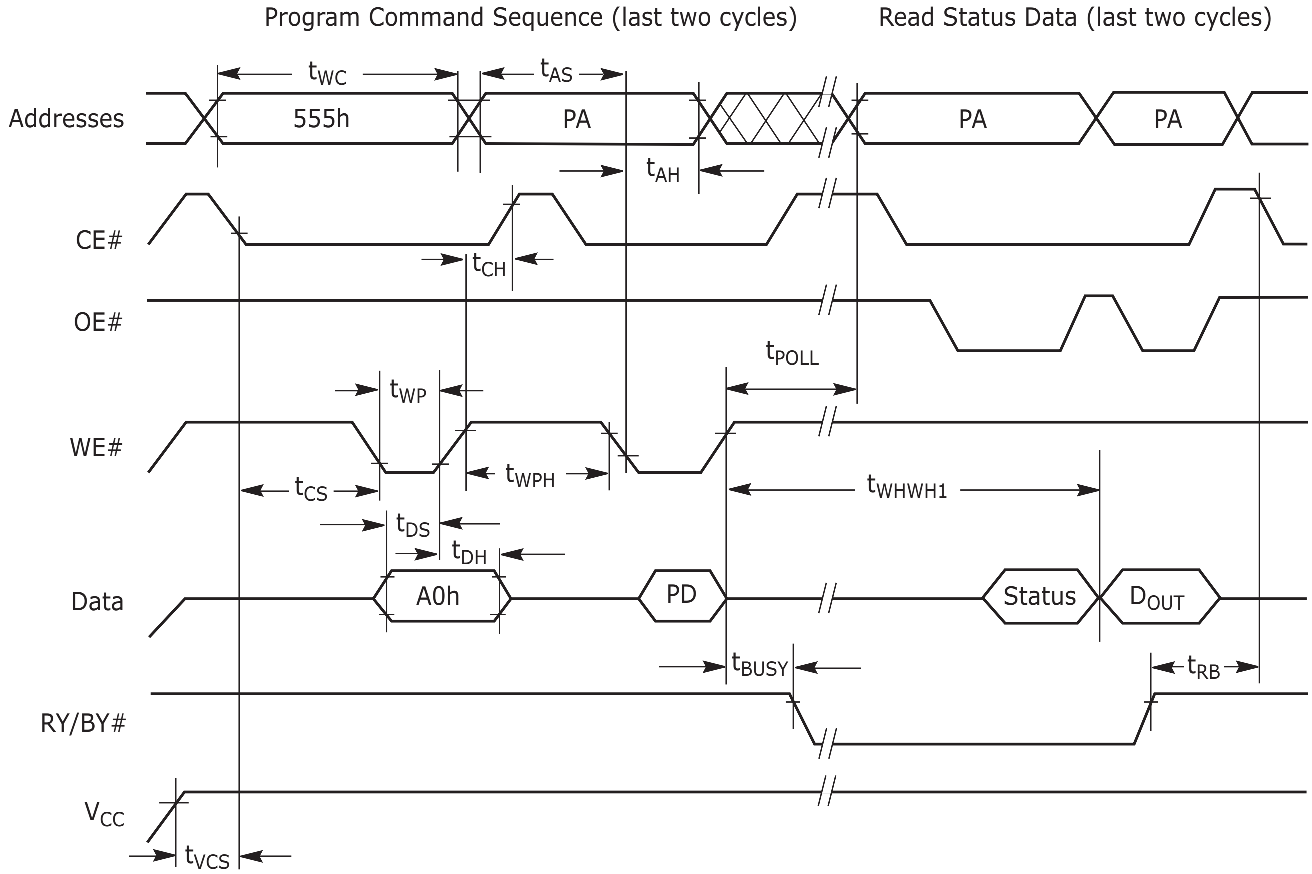
Erase and Program Operations

Parameter					Speed Options				
JEDEC	Std.	Description			90R	100, 100R	112, 112R	120, 120R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45				ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	352				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ	11				µs
			Per Word	Typ	22				µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ	8.8				µs
			Per Word	Typ	17.6				µs
		Single Word/Byte Program Operation (Note 2, 5)	Byte	Typ	100				µs
			Word		100				
		Accelerated Single Word/Byte Programming Operation (Note 2, 5)	Byte	Typ	90				µs
			Word		90				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5				sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250				ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				µs
	t_{BUSY}	WE# High to RY/BY# Low		Max	90	100	110	120	ns
	t_{POLL}	Program Valid Before Status Polling (Note 6)		Max	4				µs

Notes:

1. *Not 100% tested.*
2. *See Erase And Programming Performance on page 57 for more information.*
3. *For 1–16 words/ 1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/ 32-byte write buffer operation.*
5. *Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.*
6. *When using the program suspend/resume feature, if the suspend command is issued within t_{POLL}, t_{POLL} must be fully re-applied upon resuming the programming operation. If the suspend command is issued after t_{POLL}, t_{POLL} is not required again prior to reading the status bits upon resuming.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

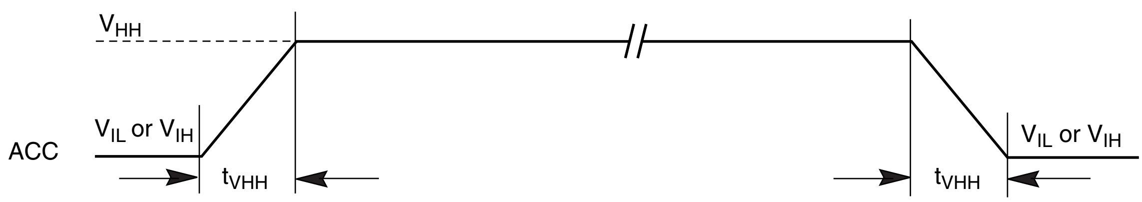
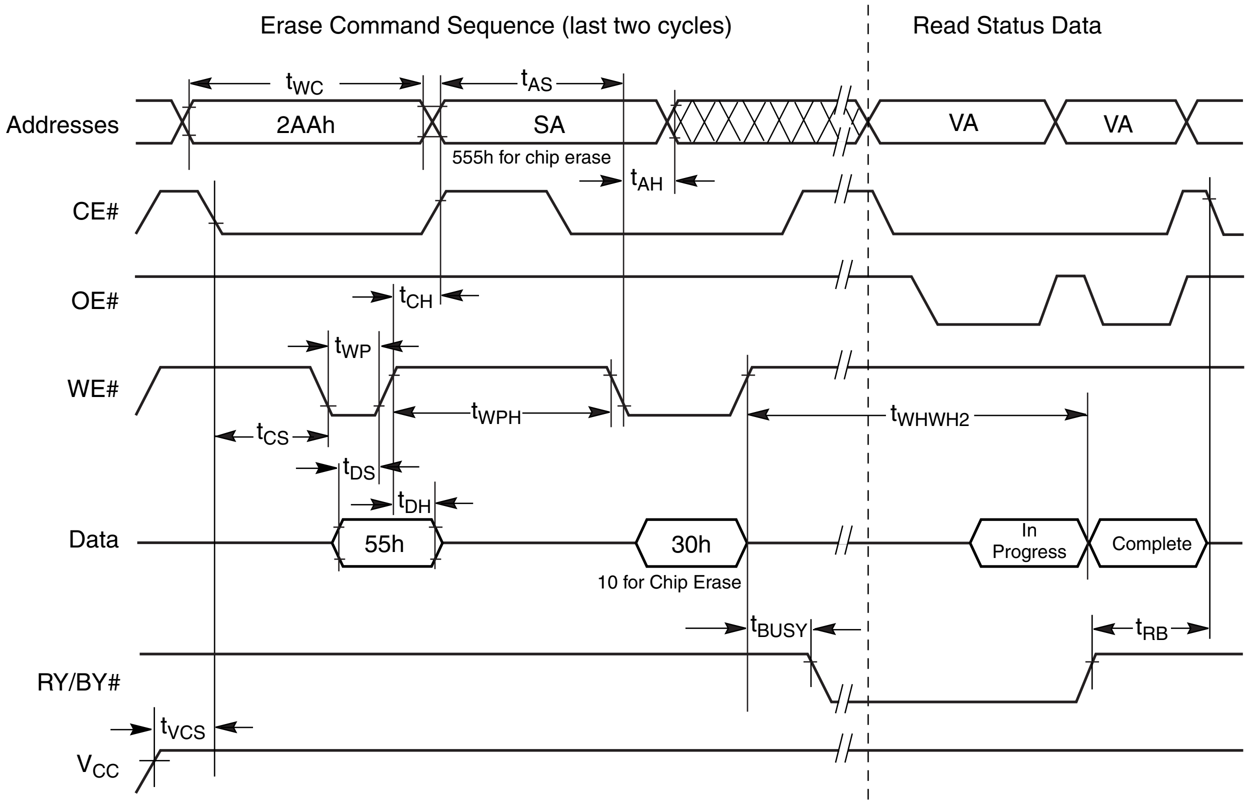


Figure 18. Accelerated Program Timing Diagram

AC CHARACTERISTICS

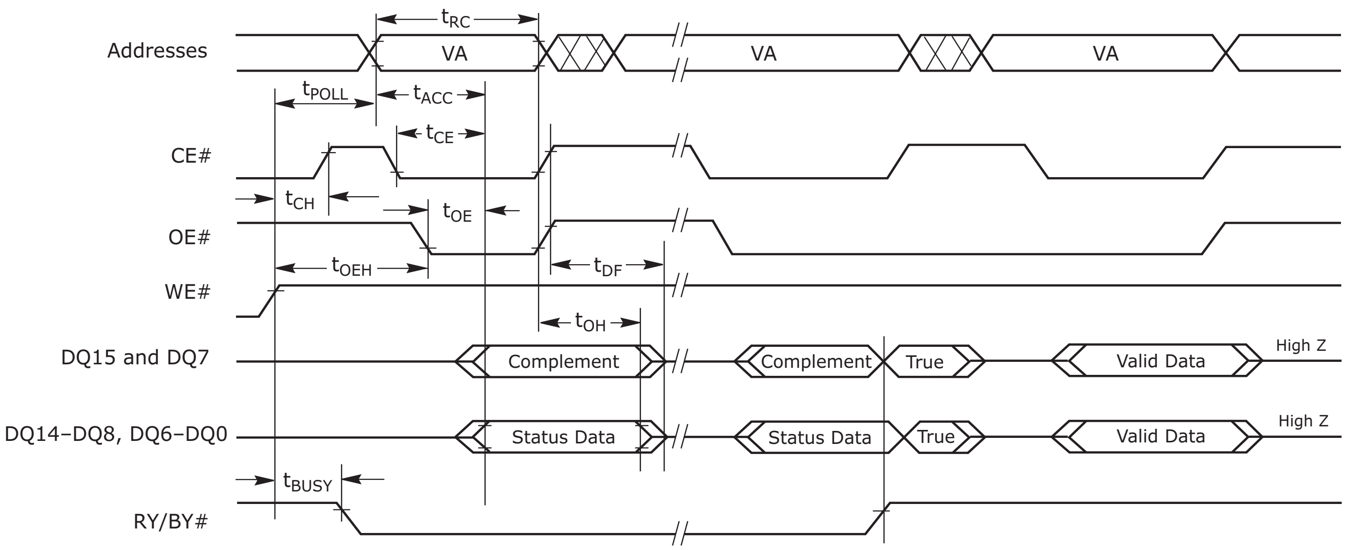


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data. See Write Operation Status on page 38.*
2. *These waveforms are for the word mode.*

Figure 19. Chip/Sector Erase Operation Timings

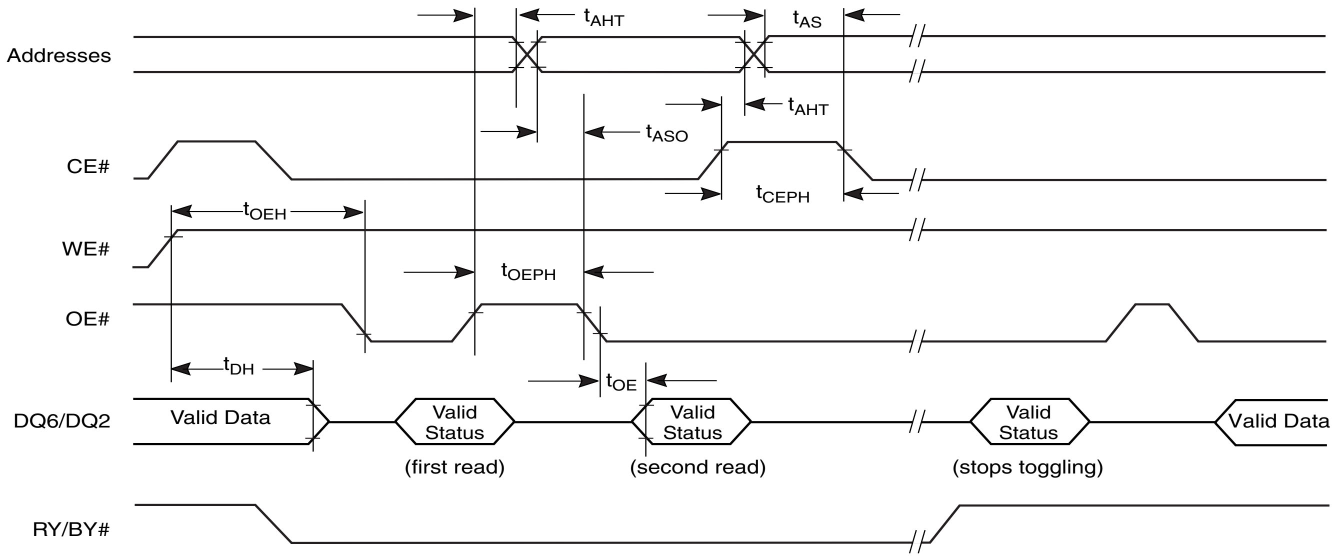
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

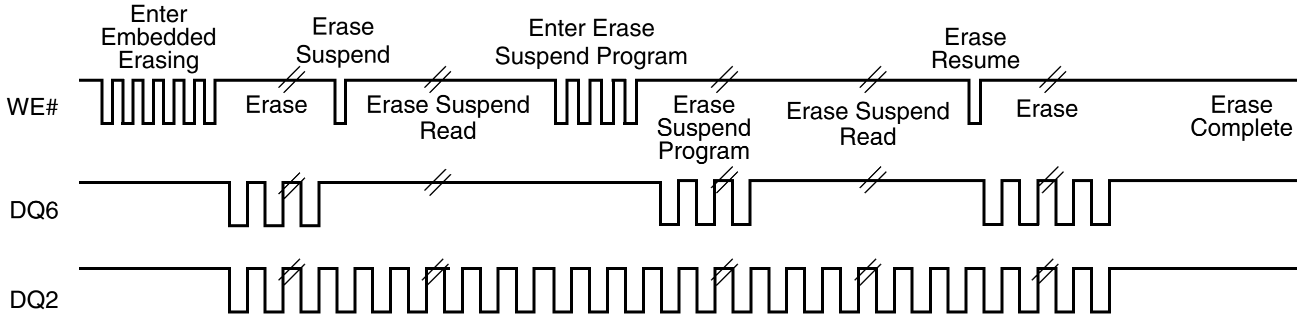
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system can use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

***Note:** Not 100% tested.*

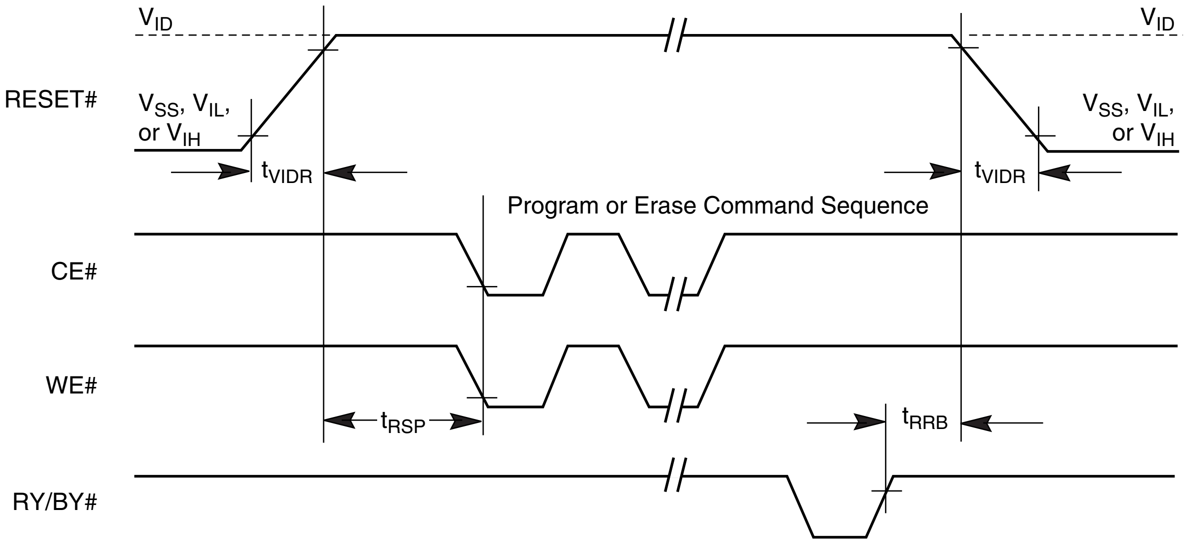
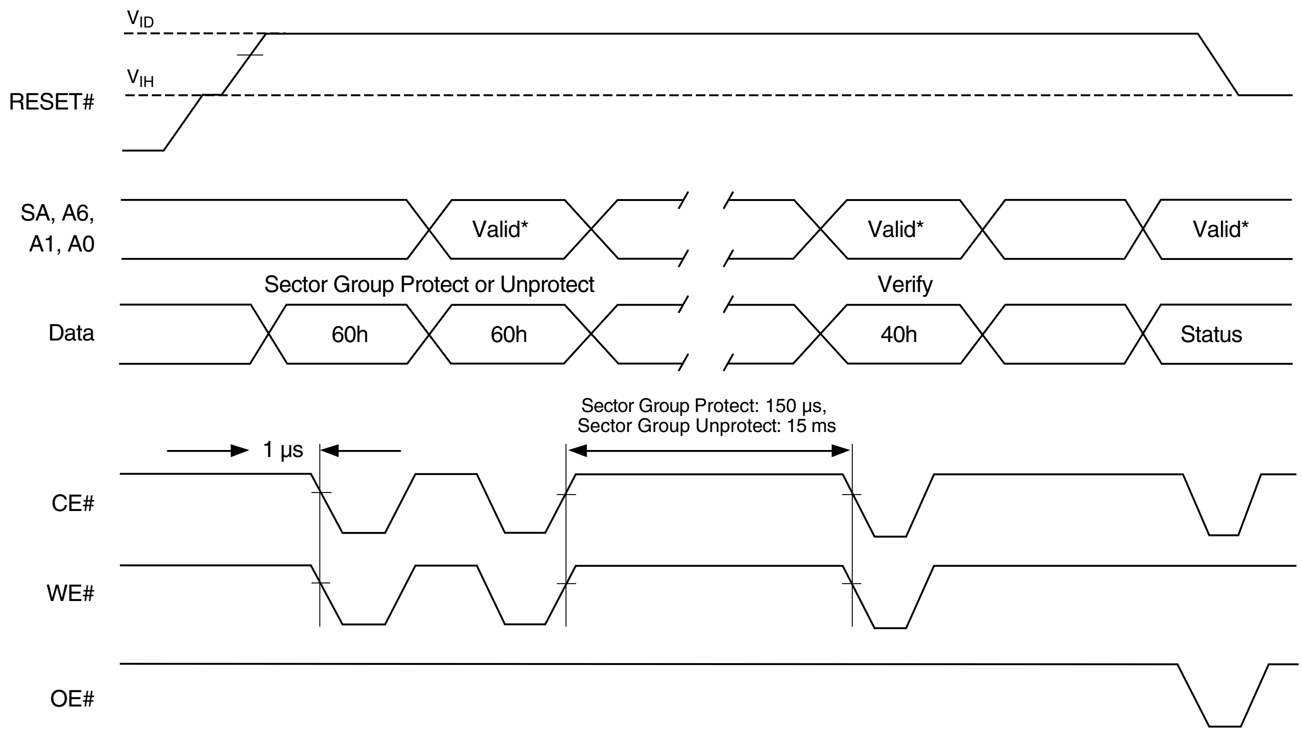


Figure 23. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS



** For sector group protect, A6–A0 = 0xx0010. For sector group unprotect, A6–A0 = 1xx0010.*

Figure 24. Sector Group Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

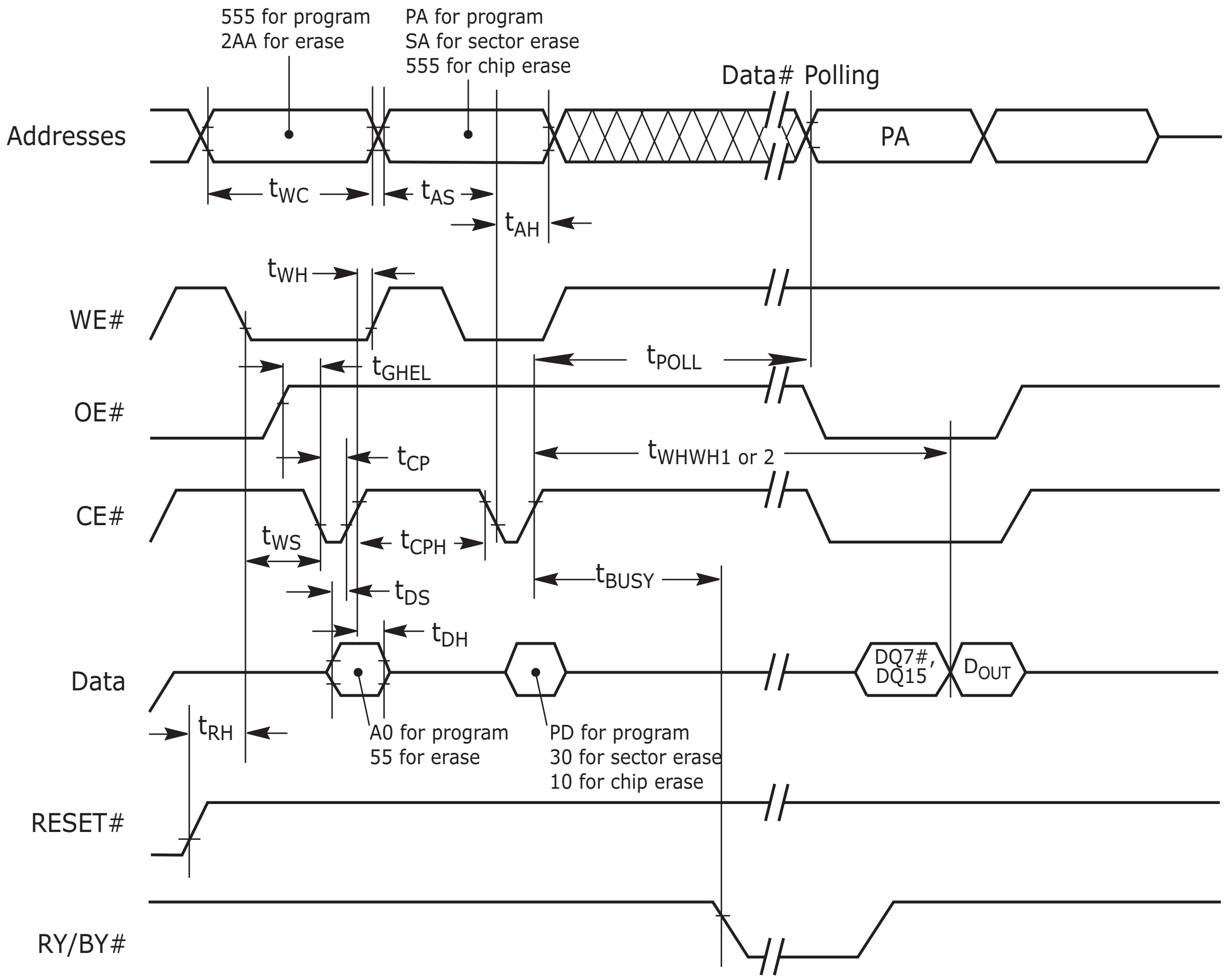
Alternate CE# Controlled Erase and Program Operations

Parameter					Speed Options				
JEDEC	Std.	Description			90R	100, 100R	112, 112R	120, 120R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45				ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45				ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	352				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ	11				µs
			Per Word	Typ	22				µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ	8.8				µs
			Per Word	Typ	17.6				µs
		Single Word/Byte Program Operation (Note 2)	Byte	Typ	100				µs
			Word		100				
		Accelerated Single Word/Byte Programming Operation (Note 2)	Byte	Typ	90				µs
			Word		90				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5				sec
	t_{RH}	RESET High Time Before Write (Note 1)		Min	50				ns
	t_{POLL}	Program Valid Before Status Polling (Note 6)		Max	4				µs

Notes:

1. *Not 100% tested.*
2. *See Erase And Programming Performance on page 57 for more information.*
3. *For 1–16 words programmed/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.*
6. *When using the program suspend/resume feature, if the suspend command is issued within t_{POLL}, t_{POLL} must be fully re-applied upon resuming the programming operation. If the suspend command is issued after t_{POLL}, t_{POLL} is not required again prior to reading the status bits upon resuming.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	15	sec	Excludes 00h programming prior to erasure (Note 6)
Chip Erase Time		64	128	sec	
Single Word/Byte Program Time (Note 3)	Byte	100	800	µs	Excludes system level overhead (Note 7)
	Word	100	800	µs	
Accelerated Single Word/Byte Program Time (Note 3)	Byte	90	720	µs	
	Word	90	720	µs	
Total Write Buffer Program Time (Note 4)		352	1800	µs	
Effective Write Buffer Program Time (Note 5)	Per Byte	11	57	µs	
	Per Word	22	113	µs	
Total Accelerated Write Buffer Program Time (Note 4)		282	1560	µs	
Effective Accelerated Write Buffer Program Time (Note 4)	Per Byte	8.8	49	µs	
	Per Word	17.6	98	µs	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}. Programming specifications assume that all bits are programmed to 00h.*
2. *Maximum values are measured at V_{CC} = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.*
3. *Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.*
4. *For 1-16 words or 1-32 bytes programmed in a single write buffer programming operation.*
5. *Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.*
6. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
7. *System-level overhead is the time required to execute the command sequence(s) for the program command. See Tables 12 and 13 for further information on command definitions.*
8. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note:

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP PIN AND BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	TSOP	6	7.5	pF
			Fine-pitch BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	TSOP	8.5	12	pF
			Fine-pitch BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	TSOP	7.5	9	pF
			Fine-pitch BGA	3.9	4.7	pF

Notes:

1. Sampled, not 100% tested.

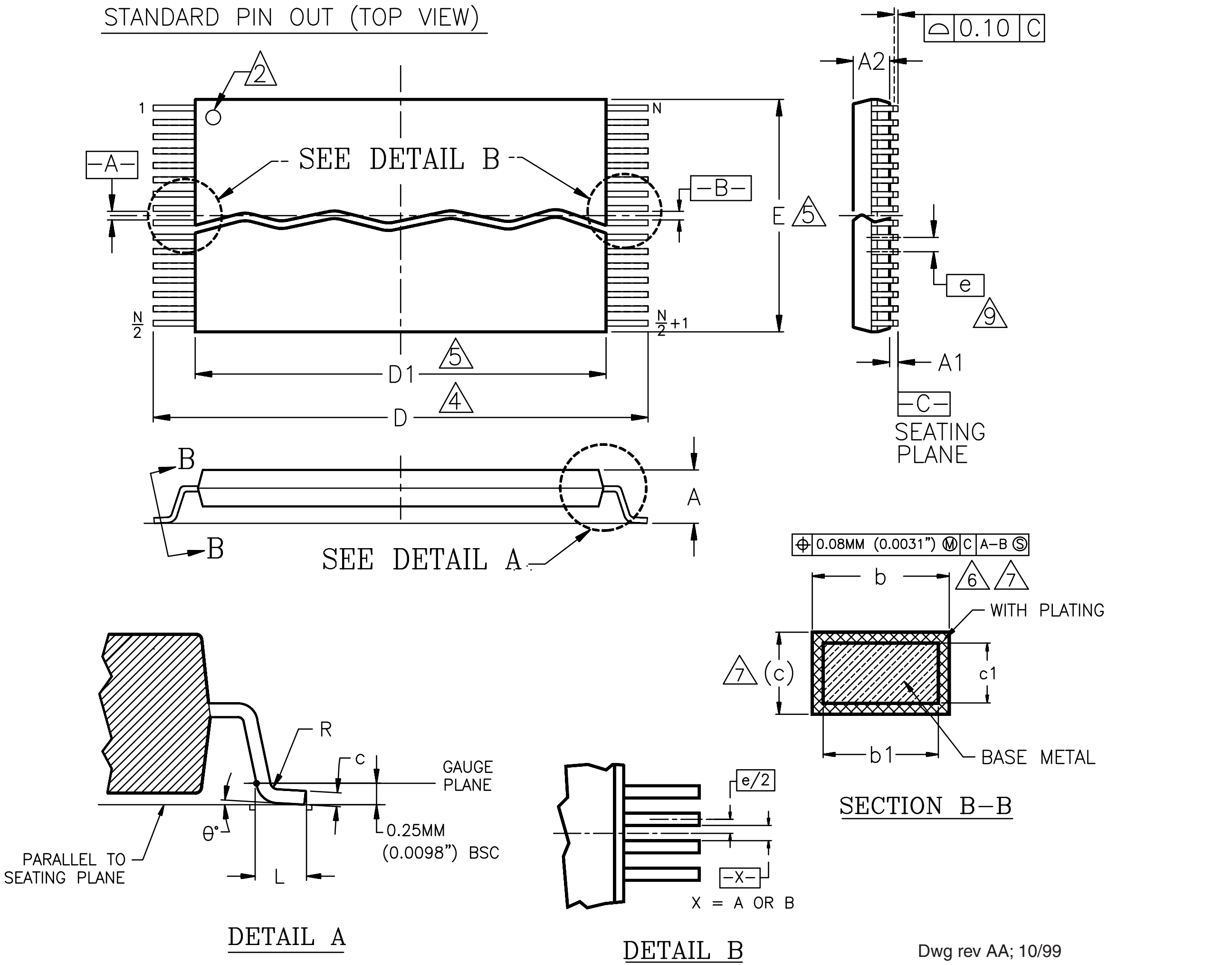
2. Test conditions $T_A = 25°C$, $f = 1.0$ MHz.

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

TS 048—48-Pin Standard Pinout Thin Small Outline Package (TSOP)



Dwg rev AA; 10/99

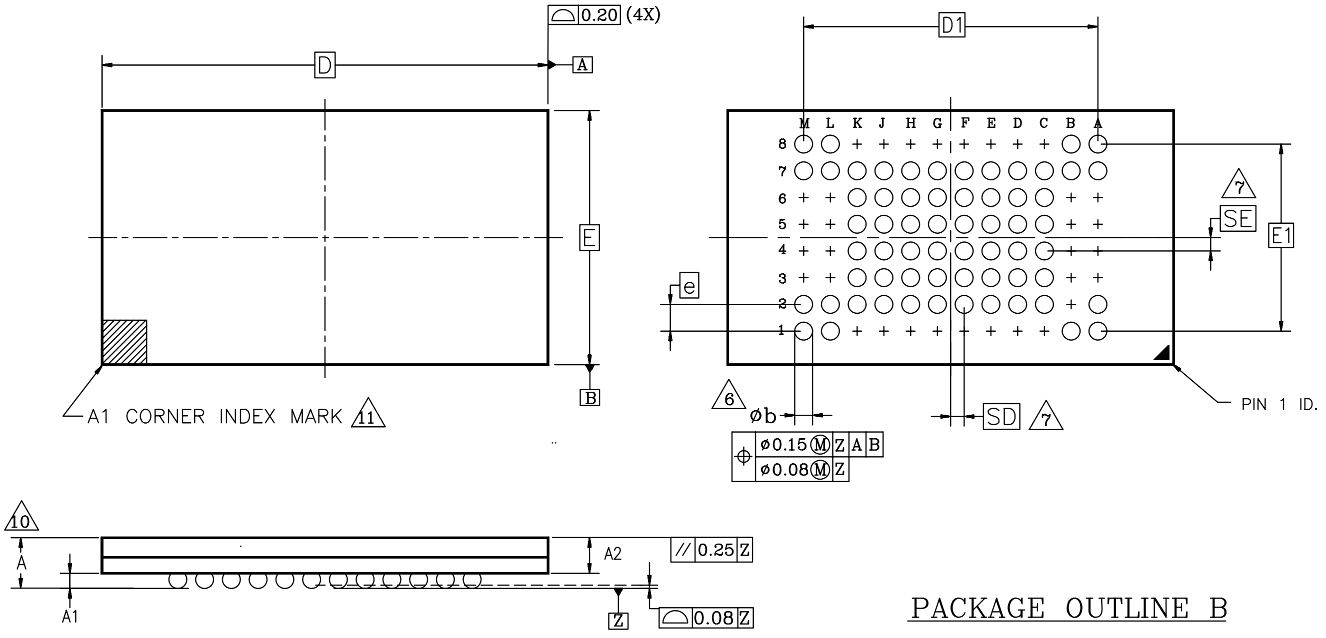
Package	TS 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS

FBE063—63-Ball Fine-pitch Ball Grid Array (FBGA) 12 x 11 mm Package



Dwg rev AF; 10/99

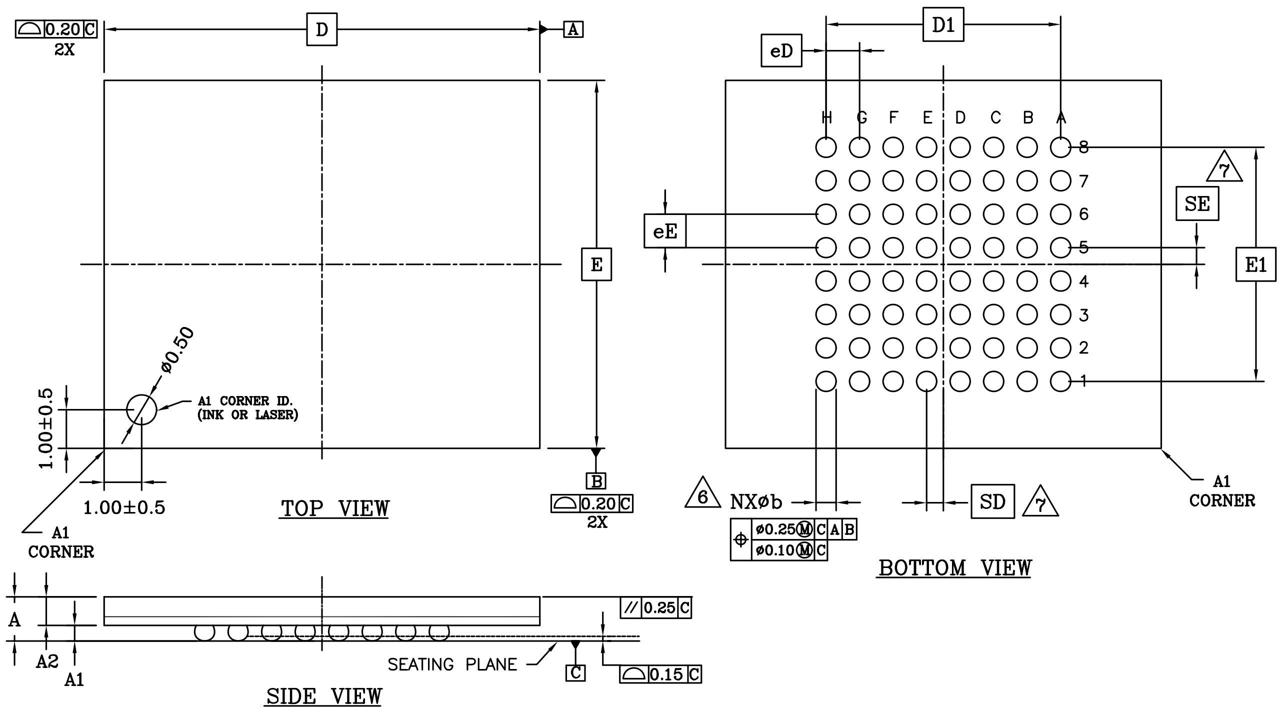
PACKAGE	xFBE 063			
JEDEC	N/A			
	12.00mmx11.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	12.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	8.80 BSC			BALL FOOTPRINT
E1	5.60 BSC			BALL FOOTPRINT
MD	12			ROW MATRIX SIZE D DIRECTION
ME	8			ROW MATRIX SIZE E DIRECTION
N	63			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A3–A6,B2–B6 L3–L6, M3–M6 C1–K1,C8–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.
11. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

PHYSICAL DIMENSIONS

LAA064—64-Ball Fortified Ball Grid Array (FBGA) 13 x 11 mm Package



PACKAGE	LAA 064			
JEDEC	N/A			
	13.00x11.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.40	PROFILE HEIGHT
A1	0.40	–	–	STANDOFF
A2	0.60	–	–	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
øb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH – D DIRECTION
eE	1.00 BSC.			BALL PITCH – E DIRECTION
SD/SE	0.50 BSC.			SOLDER BALL PLACEMENT
	A1–A8, K1–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 (EXCEPT AS NOTED).
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

REVISION SUMMARY

Revision A (April 26, 2002)

Initial release.

Revision B (May 23, 2002)

Changed packaging from 64-ball FBGA to 64-ball Fortified BGA.

Changed Block Diagram: Moved V_{IO} from RY/BY# to Input/Output Buffers.

Changed Note about WP#/ACC pin to indicate internal pullup to V_{CC}.

Revision B+1 (July 31, 2002)

MIRRORBIT 64 MBIT Device Family

Added 64 Fortified BGA to LV640MU device.

Alternate CE# Controlled Erase and Program Operations

Added t_{RH} parameter to table.

Erase and Program Operations

Added t_{BUSY} parameter to table.

Figure 16. Program Operation Timings

Added RY/BY# to waveform.

TSOP and BGA PIN Capacitance

Added the FBGA package.

Program Suspend/Program Resume Command Sequence

Changed 15 µs typical to maximum and added 5 µs typical.

Erase Suspend/Erase Resume Commands

Changed typical from 20 µs to 5 µs and added a maximum of 20 µs.

Revision B+2 (August 9, 2002)

Valid Combinations for TSOP Package

Added 100R, 110R, and 120R OPNs.

Valid Combinations for BGA Package

Added 100R, 110R, and 120R OPNs.

CMOS Compatible

Added Note 8.

Special package handling instructions

Modified the special handling wording.

DC Characteristics table

Deleted the I_{ACC} specification row.

CFI

Changed text in the third paragraph of CFI to read "reading array data."

Revision B+3 (September 19, 2002)

Ordering Information

Deleted FI from Valid Combinations Table.

Revision B+4 (October 15, 2002)

Connection Diagrams

Changed from 56-Pin Standard TSOP to 48-Pin Standard TSOP.

Product Selector Guide

Added regulated OPNs.

Revision C (December 5, 2002)

Secured Silicon Sector Flash Memory Region, and Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

Noted that the A_{CC} function and unlock bypass modes are not available when the Secured Silicon sector is enabled.

Byte/Word Program Command Sequence, Sector Erase Command Sequence, and Chip Erase Command Sequence

Noted that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program or erase operation is in progress.

Common Flash Memory Interface (CFI)

Changed CFI website address.

Command Definitions

Changed wording in last sentence of first paragraph from, "...resets the device to reading array data." to ..."may place the device to an unknown state. A reset command is then required to return the device to reading array data."

CMOS Compatible

Added I_{LR} parameter to table.

Removed V_{IL}, V_{IH}, V_{OL}, and V_{OH} from table and added V_{IL1}, V_{IH1}, V_{IL2}, V_{IH2}, V_{OL}, V_{OH1}, and V_{OH2} from the CMOS table in the Am29LV640MH/L datasheet.

Changed V_{IH1} and V_{IH2} minimum to 1.9.

Removed typos in notes.

AC Characteristics and Read-Only Operations

Changed the Chip Enable to Output High Z and Output Enable to Output High Z Speed Options from 30 ns to 16 ns.

Word/Byte Configuration

Changed BYTE# Switching Low to Output High Z Speed Options from 30 ns to 16 ns.

Customer Lockable: Secured Silicon Sector NOT Programmed or Protected at the factory.

Added second bullet, Secured Silicon sector-protect.

Revision C+1 (February 16, 2003)

Distinctive Characteristics

Corrected performance characteristics.

Product Selector Guide

Added note 2.

Connection Diagrams

Changed pin F1 to NC.

Ordering Information

Corrected Valid Combinations table.

Added Note.

AC Characteristics

Removed 93, 93R speed option.

Added Note

Input values in the $t_{WHWH}1$ and $t_{WHWH}2$ parameters in the Erase and Program Options table that were previously TBD. Also, added note 5.

Input values in the $t_{WHWH}1$ and $t_{WHWH}2$ parameters in the Alternate CE# Controlled Erase and Program Options table that were previously TBD. Also, added note 5.

Erase and Programming Performance

Input values into table that were previously TBD.

Added note 3 and 4

Revision C+2 (June 12, 2003)

Ordering Information

Added 90R speed grade.

Erase and Programming Performance

Modified table and notes, inserted values for Typical.

Revision C+3 (February 12, 2004)

Erase Suspend/Erase Resume Commands

Added note reference to erase operation.

Table 12 & Table 13: Command Definitions

Modified the Addr information for both Program/Erase Suspend and Program/Erase Resume from BA to XXX.

AC Characteristics - Erase and Program Operations, and Alternate CE# Controlled Erase and Program Operations

Added t_{POLL} information.

AC Characteristics Figures - Program Operation Timings, Data# Polling Timings (During Embedded Algorithms, and Alternate CE# Controlled Write (Erase/Program) Operation Timings

Updated figures with t_{POLL} information.

Revision C+4 (August 19, 2004)

Added Max programming specifications.

Cover sheet and Title page

Added notation referencing superseding documentation.

Revision C+5 (November5, 2004)

Ordering Information and Valid Combinations

Added Pb-Free options

Revision C+6 (December 7, 2004)

Coversheet and Title page

Added notation referencing superseding documentation.

Revision C+7 (December 13, 2005)

Global

This product has been retired and is not available for designs. For new and current designs, S29GL064A supersedes Am29LV640MT/B and is the factory-recommended migration path. Please refer to the S29GL064A datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

Revision C8 (February 1, 2007)

Global

Changed SecSi Sector to Secured Silicon Sector.

AC Characteristics

Erase and Program Operations table: Changed t_{BUSY} to a maximum specification.

Colophon

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